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Mixed-phase Ni–Al as barrier layer against perovskite oxides to react with Cu for ferroelectric memory with Cu metallization

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ABSTRACT

The microstructures, interfaces, and physics properties of the devices with multifunctional barrier materials are investigated to achieve integration of perovskite oxide films with Cu film on Si for the application in nonvolatile Si-based ferroelectric random access memories (FeRAMs) with the on-chip copper metallization of advanced microelectronic devices. $La_{0.5}Sr_{0.5}CoO_3/Pb(Zr_{0.4}Ti_{0.6})O_3/La_{0.5}Sr_{0.5}CoO_3$ (LSCO/PZT/LSCO) capacitors have been successfully fabricated on the Cu/Ni–Al/SiO_2/Si stack structure for Cu interconnects using an amorphous Ni–Al (a-Ni–Al) film as the barrier layer for the Cu/SiO_2 interface and a mixed-phase nanocrystalline Ni–Al (n-Ni–Al)/a-Ni–Al ((n+a)-Ni–Al) bi-layer-like film as the oxygen diffusion barrier layer for the LSCO/Cu interface, respectively. The perfect structure compatibility and clear interfaces between thin films are achieved. Excellent physical properties of the capacitor, such as high remnant polarization (~26 μC/cm^2), good reliability and dielectricity, powerfully confirm that Ni–Al film can be used as the barrier layer between Cu and SiO_2 or LSCO. The barrier properties of the (n+a)-Ni–Al can be understood as two aspects: n-Ni–Al component can level up the roughness of Cu/barrier/SiO_2/Si surface and relax stresses in the multilayer stack heterostructure, and a-Ni–Al can inhibit oxygen penetration. Compared to the (n+a)-Ni–Al, only n-Ni–Al film without a-Ni–Al layer couldn't prevent Cu oxidation due to oxygen penetration leading to the failure of devices, whose failure mechanism can be ascribed to the reactions between Cu and complex oxides. The results fully illustrate the viability of the lead-based ferroelectric capacitors grown on Cu/Barrier/SiO_2/Si stack structure with Ni–Al barrier for the future ferroelectric capacitor based devices with Cu metallization.

1. Introduction

Perovskite materials such as Pb(Zr,Ti)O_3 (PZT), as one of the most commonly used ferroelectric materials, has been intensively studied due to its potential applications in piezoelectric sensors and actuators, pyroelectric infrared detector, nonlinear optical devices, and nonvolatile Si-based ferroelectric random access memories (FeRAMs) [1–5]. The electrical properties of ferroelectric thin films are strongly influenced by their electrode materials [6,7]. Perovskite electrodes being similar to PZT in structure, like $La_{0.5}Sr_{0.5}CoO_3$ (LSCO), $SrRuO_3$ (SRO) and $LaNiO_3$ (LNO), can provide a famous reliability of ferroelectric thin films [8,9]. On the other hand, with the shrink of the feature sizes in ultralarge scale integration microelectronic devices, Cu has been a viable dominant material for backend interconnects in Si semiconductor processing due to its superior electrical resistivity and resistance to electromigration [10–12]. The development of the next high density FeRAMs will provoke a motivation to integrate ferroelectric capacitors with Cu metallization in order to take advantage of their own strengths and complete the multiplication together. Firstly, the low cost, high conductivity, and relatively easier reactive etching of Cu film, compared to Pt widely used as the electrode material in ferroelectric and complex oxide thin film devices, make it an appealing candidate to replace Pt as a basic metal material for the application

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in high-density FeRAMs [13]. Secondly, Cu has been introduced as an interconnect material for ultra-large scale integration (ULSI) due to its good conductivity and high electromigration resistance, which are superior to those of the prior interconnect materials, such as Al, showing its industrialized application in the high density Si-based devices [14,15]. Last but not least, a new ferroelectric capacitor with Cu metallization on Si substrate must arouse some new good properties, such as low series resistance (*i. e.* low RC decay) and high density, which paves the way for the integration of functional oxide films with the on-chip copper metallization of advanced microelectronic devices.

However, this is a challenging and frustrating work due to the critical issues related to Cu film itself and the interfaces of Cu/Si and Cu/perovskite oxide film. It is well known that Cu severely diffuses into Si or SiO_2, shows poor adhesion to dielectric layers, and is readily oxidized at relatively low temperatures with a significant rate, especially when it is exposed to high temperature and oxygen or oxygen plasma [16]. In this case Cu oxide will become more incident, but the synthesis of those oxide films, for example, PZT and LSCO, always require these unfulfilling conditions above. Even so, there is still a little work done regarding integrating ferroelectric film with Cu, for example, PZT films with very good physical properties have been directly integrated on metal copper foil using sol–gel method and annealed at high vacuum [13]. Fan et al. integrated complex oxide $(Ba_xSr_{1-x})TiO_3$ (BST) film with Cu using Ta layer as diffusion barrier layer to inhibit deleterious Cu diffusion into the Si substrate and using amorphous Ti–Al as a reliable protection layer to prevent Cu to react with oxide thin film-based capacitors [16,17].

A feasible solution to solve some above-mentioned issues in integrating ferroelectric capacitors with Cu metallization is two barrier schemes, *i. e.* oxygen diffusion barrier layer between Cu and perovskite oxide films, and diffusion barrier layer between Cu and Si or SiO_2. In fact, a host of research works about the latter have been published with good physical properties unless the thermal stability greater than 800 °C or ultrathin thickness less than 5 nm [11,12]. This work is relatively easy to benefit from inexistence of oxygen environment and complex layer structure. Nonetheless for the former, it will completely be different because the oxygen diffusion barrier layer necessarily exposed to a high deposition temperature and oxygen atmosphere. The situation makes the integration of perovskite oxides with Cu metallization significantly more difficult due to (i) an initial stage of rough copper film grown at silicon substrate with diffusion barrier layer, (ii) oxygen penetration when barrier materials has to be exposed to oxygen atmosphere, (iii) Cu/barrier/oxide electrode interface roughening and (iv) Cu recrystallization observed during the annealing of oxide thin films at a high temperature [18]. An oxygen diffusion barrier layer should possess a nature of strong oxidation resistance and chemical stability in order to prevent Cu oxidation and interdiffusion/reaction during the growth of oxide films in an oxygen atmosphere. In addition, this oxygen diffusion barrier layer must also be a good conductor and form ohmic contact to its adjacent layer, such as Cu and oxide electrode, for a direct electrical contact between the drain of transistor and bottom electrode of the ferroelectric capacitor via Cu wiring [19].

In this work, Ni–Al, an intermetallic compound, has been employed as diffusion barrier layer and oxygen diffusion barrier layer simultaneously to realize integrating ferroelectric capacitor with copper film based on the following reasons. To begin with, Ni–Al was chosen as oxygen diffusion barrier based on our previous work that revealed its excellent barrier properties against oxygen penetration at elevated temperature of 550 °C for integration of $Pb(Zr_{0.4}Ti_{0.6})O_3$ films with Si for the fabrication of ferroelectric random access memories [20]. What's more, the superiorities of Ni–Al itself, such as low density, high melting point, low cost, easily being patterned by conventional etching techniques and oxidation resistance at elevated temperatures, make it to be a good choice among several candidates in barrier material systems [21–23]. As shown in Table 1, a general comparison table for the performance of the Ni–Al and other similar binary and ternary materials is provided. It is found that the Ni–Al possesses high thermal and chemical stability, and good conductivity. Thirdly, a multifunctional barrier layer, *i.e.* diffusion barrier for Cu/Si and oxygen barrier for Cu/perovskite oxides with the same material, can simplify process and lower cost.

The physical and chemical properties of intermetallic compounds as barrier layer materials often correlate with their crystallinity, and the amorphous should be preferred to prevent the fast diffusion of oxygen at high temperatures because of no grain boundaries. For instance, a distinct chemical reaction with the oxide electrode happens for the crystalline Ti–Al intermetallic material thus preventing ohmic contact between ferroelectric capacitor and Si transistor, corresponding to the failure of device performance. In contrast, when the amorphous material is used as a barrier layer, the intact interfaces in the electrode/barrier layer/Si layer structure are presented and an ohmic contact to oxide is formed while the device exhibits good ferroelectric behavior [19]. Our previous work also found similar results that an amorphous Ni–Al (a-Ni–Al) film possesses much stronger oxidation resistance than the polycrystalline Ni–Al (c-Ni–Al) film, and the crystallinity of the Ni–Al film impacts the interfaces and microstructure of LSCO, which can further influence the physical properties of the PZT capacitors in LSCO/PZT/LSCO/Ni–Al/Si heterostructure [31]. It was reported that the reason for the formation of amorphous phases of binary metallic alloys has been shown to be due to large differences in the atomic radii of the components, deep eutectics in the phase diagram, a strong affinity between the components of the alloy, and the presence of a predominantly covalently bonded species such as Al favoring the formation of these phases [18,19]. In our experiments, we have found that the crystallinity of the Ni–Al film can be well tailored by the deposition power of magnetron sputtering, *i. e.* an amorphous pure phase Ni–Al film can be yielded at low rf powers of 6–12 W, a nanocrystalline Ni–Al (n-Ni–Al) film with ~5 nm grains formed at medium rf powers of 18–27 W, and a c-Ni–Al film prepared at high rf powers of 50–70 W. This subtle technological control for the crystallinity of Ni–Al film facilitates this work.

Based on the reasons above, a-Ni–Al thin film has been used as diffusion barrier layer between Cu and SiO_2. It is found that 4.5-nm-thick a-Ni–Al film can act as an effective diffusion barrier to remain the stable Cu-coated Si substrate. This pure amorphous Ni–Al achieved by low rf power (7 W) only has a rate of 0.15 nm/min, which is competent to ultrathin diffusion barrier layer. On the basis of Cu/a-Ni–Al/SiO_2 stack structure above with a robust a-Ni–Al barrier layer, Ni–Al film has also been introduced again as the oxygen diffusion barrier layer between LSCO and Cu for integrating LSCO/PZT/LSCO capacitor on Cu/a-Ni–Al/SiO_2 substrate. In this step, it is found that the initial stage of thin films, *i.e.* the surface of Cu/a-Ni–Al/SiO_2 stack structure, is not smooth like that of Si, but shows undulations with the root mean square (RMS) roughness of ~20 nm. This requires thicker barrier layer and makes us to give up the pure amorphous phase of Ni–Al prepared by the rf powers of 6–12 W owing to its very low deposition rate. The rf power was changed from 7 W to 25 W corresponding to the deposition rate from 0.15 nm/min to 2.7 nm/min, in which the nonlinear change of the rate vs power accompanies the phase change of Ni–Al film. The 25 W Ni–Al is still amorphous from XRD measurement, but nanoscale grains have been observed by HRTEM, indicating that the Ni–Al film possesses a nanocrystalline state. But in our

Table 1
A general comparison for the performance of the Ni–Al and other materials.

Material	Function	Thermal stability (Thickness)	Chemical states	Resistivity (μΩ cm)
Ni–Al [24,25]	Diffusion barrier	750 °C (5 nm)	$Al2p_{1/2}$, $Ni2p_{1/2}$,$Ni2p_{3/2}$	24–54
Ni–Ti [26,27]	Diffusion barrier	700 °C (5 nm)	$Ni2p_{1/2}$,$Ni2p_{3/2}$	~370
Ti–Al [19]	Oxidation barrier	>700 °C (50 nm)	$Ti2p_{1/2}$,$Ti2p_{3/2}$, $TiO_2 2p_{1/2}$,$TiO_2 2p_{3/2}$	300
Ta–Ni [28]	Diffusion barrier	650 °C (20 nm)	–	170
Ti–Al–N [29]	Diffusion barrier	1000 °C (100 nm)	–	216
Ta–Si–C [30]	Diffusion barrier	750 °C (5 nm)	–	–

experiments, we have found that 200 nm n-Ni–Al could not act as an effective oxygen barrier layer to suppress chemical reactions between Cu and perovskite oxides. Therefore, a novel mixed-phase Ni–Al scheme, i.e. n-Ni–Al with the grains of a few nanometers in size surrounded by an amorphous matrix (80% of total thickness) plus pure amorphous phase (20% of total thickness), (n+a)-Ni–Al for short, has been implemented as oxygen diffusion barrier layer between LSCO/PZT/LSCO capacitor and Cu/a-Ni–Al/SiO_2 stack structure. The interfaces, microstructures and physical properties of the LSCO/PZT/LSCO/(n+a)-Ni–Al/Cu/a-Ni–Al/SiO_2 heterostructure are evaluated. In addition, to understand the barrier mechanism of (n+a)-Ni–Al, the heterostructure only with n-Ni–Al barrier layer, is also analyzed as the comparison. Lastly, the understanding for barrier properties of (n+a)-Ni–Al and the failure mechanism of n-Ni–Al as oxygen diffusion barrier layer are discussed.

2. Experimental

All the films in the Pt/LSCO/PZT/LSCO/Ni–Al/Cu/Ni–Al/SiO_2/Si heterostructure were prepared by sputtering except for PZT film prepared by sol–gel method. The integration was completed by a multistep procedure. (1) The p-type (001) Si wafer with thermally oxidized 300-nm-thick SiO_2 layer was transferred into the sputtering chamber right after ultrasonically rinsed in acetone, 2-propanol, and washed with de-ionized water successively, and finally dried with high-purity N_2. 4.5-nm-thick Ni–Al film was deposited on the Si wafers using rf magnetron sputtering from a Ni_3Al target at a power of 7 W in a 3 Pa atm of Ar. Inductively coupled plasma (ICP) analysis indicated that the atomic ratio of Ni:Al in Ni–Al film was very close to 3:1 of the Ni_3Al target. The base pressure was maintained at 2×10^{-4} Pa and the flow of high-purity Ar is 50 sccm. Before the Ni–Al deposition on Si wafers, a 10 min pre-deposition was performed in order to remove the target contamination due to the exposure of air. Cu film of 100 nm in thickness was then *in situ* deposited on Ni–Al/SiO_2/Si heterostructure without opening the chamber at a power of 50 W, the only one deposition parameter changed compared with those of Ni–Al film deposition. (2) Cu/Ni–Al/SiO_2/Si was further used as a substrate to grow oxide ferroelectric capacitor based on the above analysis results. (3) 200-nm-thick Ni–Al film was grown on Cu/Ni–Al/SiO_2/Si substrate in a 3 Pa atm of Ar with a rf power of 25 W first for ~160 nm n-Ni–Al and then being switched to 7 W for ~40 nm a-Ni–Al, accompanying 200-nm-thick n-Ni–Al only with a rf power of 25 W as a comparison analysis. (4) ~40 nm thick LSCO film was *in situ* deposited on Ni–Al/Cu/Ni–Al/SiO_2/Si at the following conditions: temperature = 400 °C, Ar:O_2 = 3:1, and power = 50 W, followed by a rapid thermal annealing (RTA) at 550 °C for 2 min in O_2. (5) 120-nm-thick PZT film was prepared by the spin coating technique using a modified PZT sol–gel solution and then annealed at 550 °C for 5 min using RTA method. Detailed information about preparing the samples can be found elsewhere [20]. (6) Pt (100 nm)/LSCO (40 nm) integrated top electrode was in series deposited on the surface of PZT/LSCO/Ni–Al/Cu/Ni–Al/SiO_2/Si heterostructure through a shadow mask to get 1×10^{-4} cm^2 circular pads, which was then annealed as mentioned in step (4) in order to obtain symmetric top and bottom electrodes.

The interfaces and microstructures of the heterostructures were identified by transmission electron microscopy (TEM) and X-ray diffraction (XRD). The ferroelectric properties of the capacitor were determined using a precision LC unit from Radiant Technologies. The surface morphology of thin films was showed by scan electric microscopy (SEM). The dielectric property and the leakage current of the capacitor were measured by Agilent E4980A LCR Meter and Keithley 2601 Source Meter instruments respectively.

3. Results

TEM and HRTEM are employed to investigate the interfaces of the PZT/LSCO/(n+a)-Ni–Al/Cu/Ni–Al/SiO_2/Si heterostructure, as shown in Fig. 1. We can see that all the interfaces, especially for those of Ni–Al with their adjacent layers, are clear and sharp, and no evident reaction or interdiffusion happens at the interfaces, showing the excellent barrier properties of Ni–Al thin films. The performance of a-Ni–Al as diffusion barrier layer between Cu and SiO_2 is as shown in Fig. 1(b), it can be seen that the a-Ni–Al is indeed pure amorphous phase, and the intact SiO_2/a-Ni–Al and a-

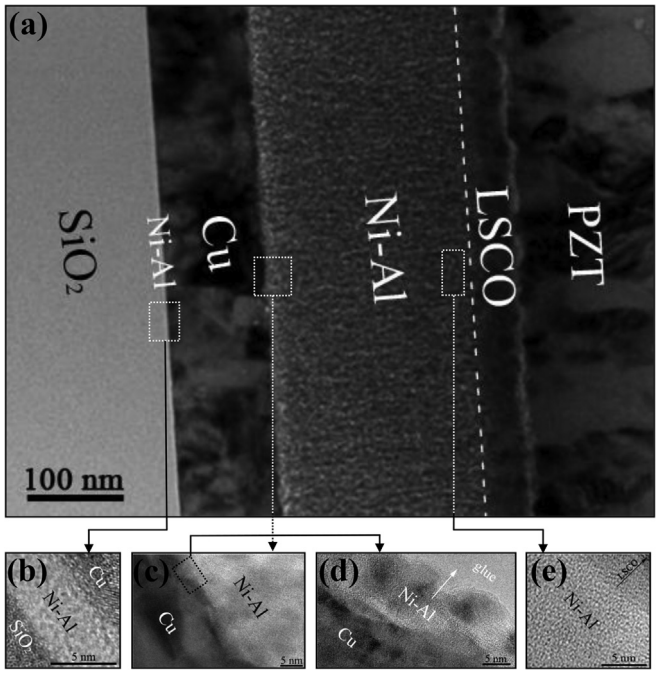

Fig. 1. (a) The cross-sectional TEM image of the PZT/LSCO/(n+a)-Ni–Al/Cu/a-Ni–Al/SiO_2/Si heterostructure. The high resolution TEM image of (b) a-Ni–Al as diffusion barrier layer and interfaces from its adjacent layers, (c) the interface between Cu and (n+a)-Ni–Al as the oxygen conducting diffusion barrier layer, (d) Cu/(n+a)-Ni–Al interface with higher resolution ratio when much of (n+a)-Ni–Al was removed, and (e) a-Ni–Al in (n+a)-Ni–Al bi-layer close to Ni–Al/LSCO interface.

Ni–Al/Cu interfaces imply it as an effective diffusion barrier layer for Cu interconnect. To emphasize (n+a)-Ni–Al as oxygen diffusion barrier layer to avoid Cu oxidation with adjacent perovskite oxides films, the part of Ni–Al close to Cu and LSCO respectively are characterized by HRTEM as shown in Fig. 1(c)–(e). It can be found that Ni–Al close to interface of Cu/Ni–Al is composed of an embedded nanocrystalline grains and amorphous matrix, and that the interface of Cu/Ni–Al lies in undulations and its roughening happens. Fan et al. also observed that interface roughening between Cu and Ti–Al occurred during the growth of BST films at high temperature due to copper grain growth in BST/Ti–Al/Cu/Ta/Si heterostructure, which resulted in large dielectric loss on the fabricated BST capacitors [16]. Here it is comforting to see these undulations have been filled and leveled up by n-Ni–Al thin film in Fig. 1(c). The PZT/LSCO/Ni–Al (much towards LSCO) in the TEM sample was removed for a more clear observation of n-Ni–Al and Cu/n-Ni–Al interface, as shown in Fig. 1(d). The nanocrystalline microstructure of Ni–Al, composed of nanocrystalline grains of ~5 nm and amorphous matrix, are further confirmed. Fig. 1(e) shows the Ni–Al close to interface of Ni–Al/LSCO is pure amorphous phase, no any crystallization, which coincides with Fig. 1(b). From the cross-sectional TEM image of our sample, we can also see that the PZT ferroelectric capacitor can be well integrated with copper film on silicon substrate.

Fig. 2 shows the typical XRD spectrum of the heterostructure, from which we can see that no impurity peaks such as copper silicides or Cu oxides, except the peaks of the PZT and Cu, can be observed. The PZT film is found to be well crystallized with random crystallographic orientation, and the Cu film is (111) highly-oriented. Interestingly, the intensity of Cu (111) peak for the 100-nm-thick Cu film is much higher than those of 120-nm-thick PZT film, meaning that Cu film keeps intact after the thrice 550 °C anneals for PZT, bottom and top LSCO. Here although nanocrystalline Ni–Al was observed in TEM image in Fig. 1(d), no Ni–Al peaks can be found from XRD pattern. This can be attributed to the poor crystallinity of the n-Ni–Al and sensitivity of XRD technique as well as small amount of n-Ni–Al.

Fig. 3(a) demonstrates a polarization hysteresis loop of a typical Pt/LSCO/PZT/LSCO/(n+a)-Ni–Al/Cu/a-Ni–Al/SiO_2/Si heterostructure capacitor, vertically measured at 5 V. The contact between the bottom electrode of ferroelectric capacitor and SiO_2/Si was realized by Ni–Al/Cu/Ni–Al multilayered electrodes. The remnant polarization (P_r) and coercive voltage (V_c) are ~26 μC/cm^2 and ~1.18 V, respectively. The switchable polarization Δ*P*, a parameter that can be directly read from the Radiant ferroelectric tester, is

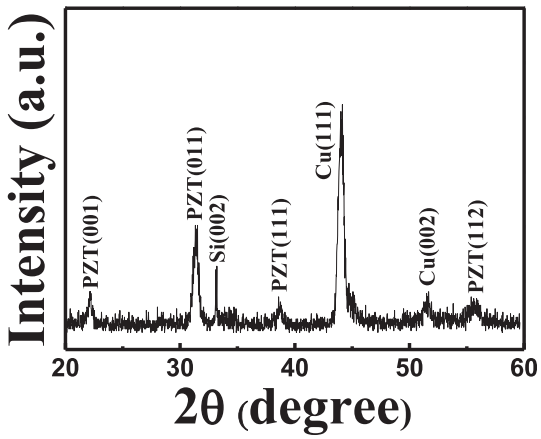

Fig. 2. X-ray diffraction pattern of the PZT/LSCO/(n+a)-Ni–Al/Cu/a-Ni–Al/SiO_2/Si heterostructure.

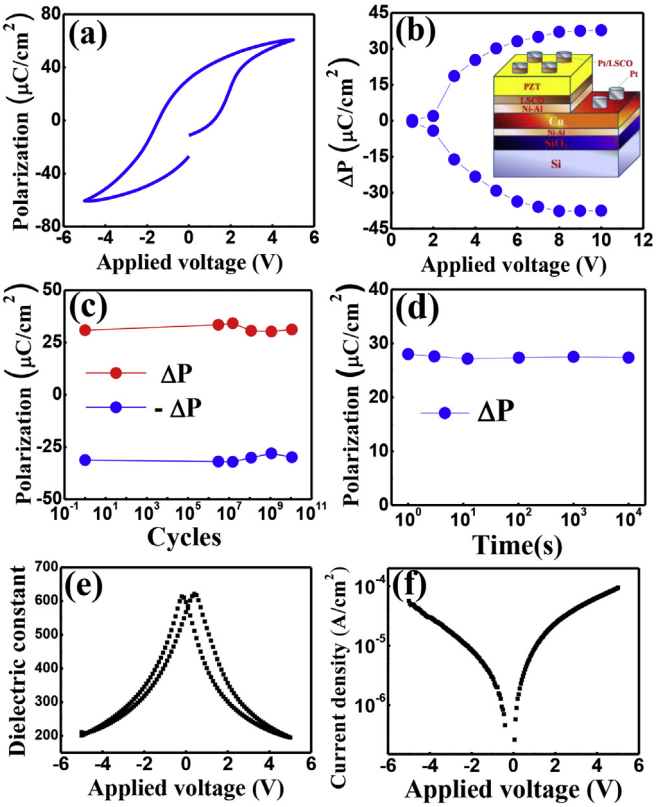

Fig. 3. (a) Ferroelectric hysteresis loop of the heterostructure capacitor measured at 5 V. (b) The switchable polarization of the heterostructure capacitor as a function of applied voltage. The inset at bottom right-hand side presents a simple diagram of the electrical measurement by vertical transport. The switchable polarizations of the heterostructure capacitor as a function of (c) switching cycle and as a function of (d) retention measurement time. (e) Dielectric constant of the heterostructure capacitor as a function of applied voltage curve at 1 kHz. (f) Leakage-current dependence on applied voltage of the heterostructure capacitor.

defined as the difference between the switched and non-switched polarizations. The larger the Δ*P*, the more "ferroelectric". The dependence of the switchable polarization (Δ*P*) on the applied voltage is shown in Fig 3(b), from which we can see that the switchable polarization, measured at 5 V, is about 30 μC/cm^2, indicating that the polarization of our samples is sufficiently high for the application of ferroelectric random access memory (FeRAM).

Reliability is the ability of a device to perform its required functions under stated conditions. Fatigue in ferroelectric capacitor can be simply defined as the loss of switchable polarization due to repeated cycling of the capacitor, and can affect the long-term reliability of ferroelectric memories. In the fatigue test, bipolar-pulsed cycles of 5 V in amplitude and at a frequency of 1.0 MHz were applied on the heterostructure capacitor. The switchable polarization, Δ*P*, was measured through pulsed polarization tests as a function of fatigue cycle, as shown in Fig. 3(c), from which we can see that the test capacitor displays very good fatigue resistance up to 10^{10} switching cycles. Retention is another reliability factor, and can be characterized as the loss of stored data with time after writing. In the retention test, the test capacitor was applied with write pulse of −5 V and read pulse of 4 V. As presented in Fig. 3(d), the switchable polarization is about 27 μC/cm^2 within the whole retention measurement time of 10^4 s without any obvious degradation of the polarization.

The bias-voltage dependences of dielectric constant of this heterostructure capacitor at 1 kHz is shown in Fig. 3(e). The

customary "double peaks" resulting from hysteresis in the permittivity-field response typical of a ferroelectric, are observed, and the peak permittivity is 621, from which dielectric properties and nonlinear nature of the heterostructure capacitor can be inferred. The Leakage current is a very important factor for dielectric materials, and higher leakage will cause resistive loss leading to the dielectric loss. Therefore, low leakage is expected for the ferroelectric capacitor. Fig. 3(f) shows the dependence of leakage current on applied voltage for this heterostructure capacitor. It can be seen that leakage current density of the sample is still below 10^{-4} A/cm^2 at 5 V after thrice 550 °C anneals, which can meet the requirements for the majority of applications. The excellent physical properties of our capacitors further confirm that a successful integration of LSCO/PZT/LSCO capacitor stack with Cu/Ni–Al/SiO_2/Si substrate can be achieved using Ni–Al films as the barriers for the interfaces of Cu/SiO_2 and Cu/LSCO synchronously.

Just as a-Ni–Al between Cu and Si, the absence of grain boundaries makes it to act as an effective barrier material, a-Ni–Al in (n+a)-Ni–Al also plays a fatal role in avoiding the existence of grain boundary in the crystalline Ni–Al (notwithstanding poor crystallization here). Hereinafter, it will be proved that n-Ni–Al without the amorphous layer does not possess barrier ability for the interface of Cu/oxide films. Although the multilayer capacitor is structurally intact, it exhibits very poor electric properties. Comparison of the physical properties of the LSCO/PZT/LSCO capacitors grown on the two types of diffusion barrier layers is further evaluated. Fig. 4(a) presents the comparison analysis of ferroelectric hysteresis loops of the heterostructure capacitors using (n+a)-Ni–Al and n-Ni–Al as oxygen diffusion barrier layer, we can see that the later is leaky, indicating that n-Ni–Al cannot be used as an effective barrier layer for integrating ferroelectric capacitor stack on Cu/Ni–Al/SiO_2/Si. Fig. 4(b) shows that the heterostructure capacitor using n-Ni–Al as oxygen barrier layer, unlike (n+a)-Ni–Al barrier layer, has lost the dielectric properties of a typical ferroelectric material. It is also found that the standard "γ"-shape *J–V* curve of the ferroelectric capacitor is given by the heterostructure capacitor with (n+a)-Ni–Al, but the one with n-Ni–Al shows almost an unsaturated leakage characteristics. The current densities of the capacitor with (n+a)-Ni–Al and n-Ni–Al, measured at 5 V, are 9.4×10^{-5} A/cm^2 and 6.9×10^{-2} A/cm^2, respectively. The severe leakage of the capacitor with n-Ni–Al implies the failure of the device function.

It is reported that grain boundaries, microcracks, or pinholes often present in oxidation diffusion barrier, and provides the path for transport of atoms or irons, causing oxidation of Cu metal phase and generation of its metalloid phase [16]. It will form some surface defects, such as hillock, pits and microholes. In this case, morphologies of PZT/LSCO/Barrier/Cu/a-Ni–Al/SiO_2/Si heterostructure pre-capacitor using (n+a)-Ni–Al and n-Ni–Al as oxygen diffusion barrier layer is observed, as shown by SEM in Fig. 5. We can see that

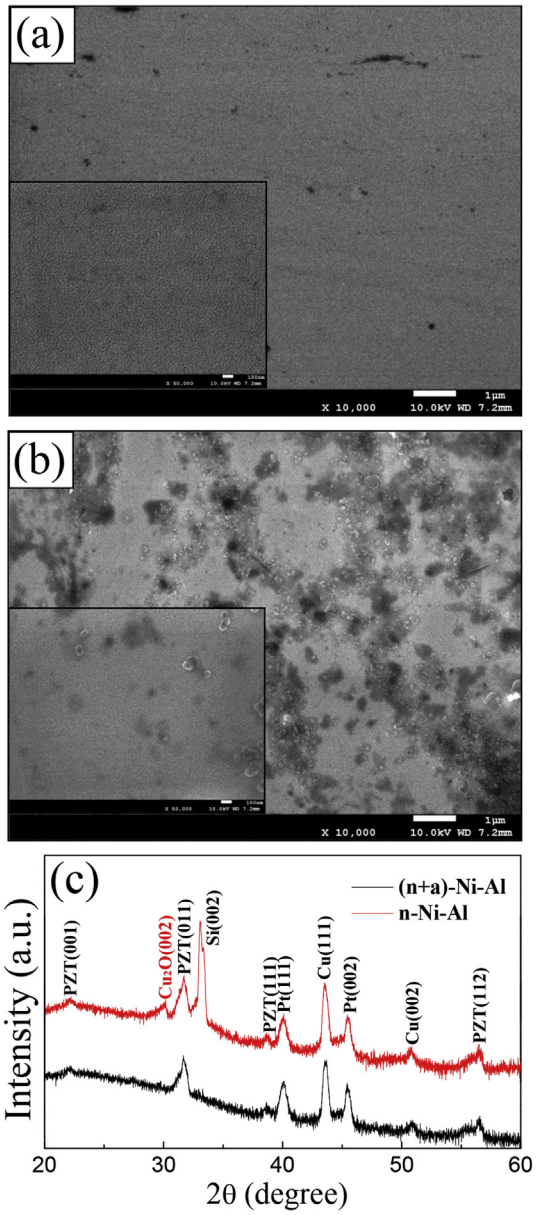

Fig. 5. SEM micrographs of the surface of PZT/LSCO/Ni–Al/Cu/Ni–Al/SiO_2/Si heterostructure using (a) (n+a)-Ni–Al, (b) n-Ni–Al as conducting diffusion barrier layers. The whole images are ×10,000 magnification and their insets at bottom left are ×50,000 magnification. (c) Comparison of XRD patterns of the Pt/LSCO/PZT/LSCO capacitors grown on the two types of conducting diffusion barrier layers.

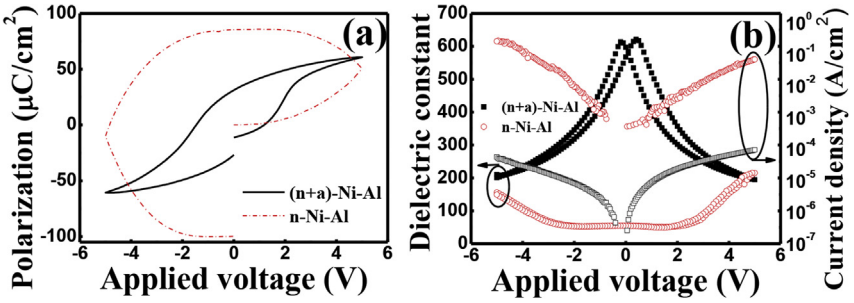

Fig. 4. Comparison of the physical properties, including (a) Ferroelectric hysteresis loop, (b) C–V curve and J–V curve of the Pt/LSCO/PZT/LSCO capacitors grown on the two types of conducting diffusion barrier layers.

the surface of sample using (n+a)-Ni–Al as oxygen barrier layer is uniform, there are no defects on it and only some nanovoids are observed. However, for the sample using n-Ni–Al as oxygen barrier layer, its surface becomes highly deteriorated and there are some apparent defects, such as pits, hillocks, and microholes, forming all over the surface [Fig. 5(b) and its inset]. This is indicative of failure of the layer structure of the heterostructure capacitor and probably due to Cu oxidized. To clarify this mechanism, XRD is employed again for detection of Cu metalloid phase, as shown in Fig. 5(c). The x-ray diffraction pattern for Pt/LSCO/PZT/LSCO/n-Ni–Al/Cu/a-Ni–Al/SiO_2/Si stack structure, unlike the sample with (n+a)-Ni–Al, the onset of the signal of Cu oxides (Cu_2O (200)) indicates that reactions between Cu and perovskite oxides happen.

4. Discussions

Surely, a high-quality ferroelectric capacitor displaying good ferroelectric switching behavior would not be achieved with a failed barrier layer material system. The excellent physical properties, including the ferroelectric, such as P_r of ~26 μC/cm^2 and V_c of ~1.18 V, the reliability and dielectric results, also indirectly indicate the good conductivity of Ni–Al/Cu/Ni–Al multilayered electrodes and a probable ohmic contact to LSCO without the occurrence of obvious reactions. It is also proved that a competent barrier scheme and successful materials integration strategies have been realized.

Diffusion barrier property of pure amorphous phase Ni–Al is readily understood, and being devoid of grain boundaries is the main reason why the barrier overcomes the failure since grain boundaries generally provide paths for oxygen diffusion [19,20,31]. The challenge that the a-Ni–Al barrier layer faces is only the high temperature, which is overcome by the high thermal stability of a-Ni–Al material. The smoothing surface from Si substrate and the room temperature deposition without oxygen avoid a series of intractable problems, and eventually an ultrathin barrier layer is presented. 4.5-nm-thick thickness also allows the a-Ni–Al to give a good conductivity due to the presence of metallic phase. However, when the same Ni–Al material is used as oxygen diffusion layer between Cu and LSCO, its work conditions are very different with a-Ni–Al as diffusion layer between Cu and Si due to the following reasons: (i) Interfaces of the Ni–Al film with its adjacent layers in Oxides/Barrier/Cu are different from those in Cu/Barrier/Si. The surface of Cu grown on Ni–Al/SiO_2/Si, as the growth basis of Ni–Al oxygen diffusion barrier layer, is also not smooth like that of Si but rather undulatory with the RMS roughness of ~20 nm. This rough surface enlarges interaction area of dislocations from neighboring interfaces and results in the complex behavior of interface energy; (ii) the Ni–Al has to encounter oxygen environment (with pO_2 in 3 Pa atm of mixture gas with a ratio of Ar:O_2 = 3:1) and high temperature (at 400–550 °C) when LSCO is fabricated on it; (iii) Some stresses in multilayer stack structure are also more perplexing because of different thermal expansivity and interface formation energy from layer to layer.

200-nm-thick mixed-phase (n+a)-Ni–Al, composed of ~160 nm n-Ni–Al and ~40 nm a-Ni–Al, as oxygen diffusion barrier layer, can effectively solve a series of problems above. For one thing, n-Ni–Al in (n+a)-Ni–Al can effectively stuff "valleys" of surface of Cu/Ni–Al/SiO_2/Si substrate and make the surface smoothing. Moreover, the relaxation of stress encountered during amorphous-to-crystalline transitions in forming thin films [32]. The function of the n-Ni–Al dispersed in a-Ni–Al matrix film also includes the relaxation of the stress for relieving the materials mismatch between metal and oxides, avoiding cracks of thin film, and maintaining the integrity of multilayer stack heterostructure capacitors. It is reported that the interface formation energy is a result of competition between dislocation interactions and strain energy. This competition results in nonmonotonic dependence of the interface formation energy on interface distance below 20 nm and decrease of overall strain energy to a constant value beyond a distance of about 20 nm [33]. The particular microstructure of the n-Ni–Al, made of embedded nanoscale grains and amorphous matrix, can effectively mitigate the dilatation of Ni–Al phase with larger interface distance and reduce accumulated elastic strain energy. Unlike polycrystalline Ni–Al, large grains make its lattice to be more close to that of Cu, leading to the decrease of interface distance and then increase of interface formation energy. And big grain boundaries generally provide more cavities as paths for oxygen diffusion. For another, a-Ni–Al in (n+a)-Ni–Al with thin thickness, devoid of grain boundaries, can effectively restrain the oxygen penetration and stop Cu oxidized in order to protect the integrity of Cu wiring in the heterostructure capacitor. This understanding can be powerfully proved by our experimental results. If a polycrystalline Ni–Al were employed to act as the same task, it is found that the layer structure of the heterostructure is very difficult to keep being intact and often collapses in the step of LSCO growth. What the multilayer structure took on serious collapse could be readily identified by eyes (not shown here), while n-Ni–Al is introduced as this role, the failure from eyes can be eliminated to show intact layer structure.

This plausible intact multilayer film capacitor with n-Ni–Al oxygen barrier, seems to surpass the one with polycrystalline Ni–Al, but its physical properties, such as the ferroelectric, dielectric and leakage, tell us that is deceptive. Further SEM and XRD analysis demonstrate the n-Ni–Al as oxygen barrier against oxygen into Cu thin film is also failure in nature. Its mechanism is similar to the failure of Cu electrode reported by Ref. [16] and here it is likely elucidated by three steps. In the step 1, oxygen in Ni–Al/LSCO interface breaks through barrier layer across some active diffusion paths, such as grain boundaries, and start oxidizing Cu layer. The volume expansion of the Cu oxide will enlarge the path and allow more oxygen to go through, which results into drastic interdiffusions or interreactions between Cu and oxides (Step 2). The growing Cu oxide may burst the n-Ni–Al barrier layer and thin film capacitor at locations where oxidation starts by the transport of Cu^+ from the metal, and deteriorate the surface of the multilayer structure, leading to the formation of some defects and eventually the failure of device.

In view of this, amorphous phase is introduced again to form a mixed-phase alloy thin film, which is simply operated in process, only by a power switch. It was mentioned that the formation of nanocrystalline Ni–Al grains in the mixed-phase thin film is not resulting from heat treatment [24]. Because any diffusion-based atomic restructuring process initiated by heat treatment should be required at a temperature comparable to half of the melting point of material (550 °C was used in this work, but the melting temperature of Ni_3Al is about 1430 °C) [34,35]. The nonlinear dependence of the deposition rate on sputtering power in this work indicates the change of ion energy during depositing, not just the ionization rate. It can be concluded that the tailor of crystallinity of the Ni–Al film should be mainly achieved by the deposition energy during sputtering. The a-Ni–Al was achieved at low deposition energies. The formation of (n+a)-Ni–Al encountered a high–low transition of deposition energies.

The ideal properties of the capacitor with (n+a)-Ni–Al can be attributed to the intact Cu wiring, the intact layer structure and the good interfaces. The unexpected results of the one with n-Ni–Al, causing poor ferroelectric and dielectric properties, can be ascribed to the Cu–O reactions which bring out the failure of Cu metallization and microstructure of multilayer capacitor.

5. Conclusions

In summary, the potential of introducing Cu interconnects into the next high density FeRAMs in Si semiconductor IC has been excavated by integrating PZT ferroelectric capacitor on Cu/Barrier/SiO_2/Si stack structure using Ni–Al as dual functional barrier layer for Cu/Si and Cu/oxides. 4.5-nm-thick ultrathin amorphous Ni–Al layer was fabricated between Cu and SiO_2. HRTEM and XRD data prove the ultrathin amorphous Ni–Al layer has a good thermal stability, and the lack of grain boundary should be responsible for its success. We have further successfully integrated PZT-based capacitor on Cu/Barrier/SiO_2/Si stack structure using Ni–Al films as the oxygen diffusion barrier between Cu and LSCO film. In this multilayer structure, a mixed-phase (n+a)-Ni–Al has been employed as oxygen barrier layer due to its particular architectures, in which n-Ni–Al plays an important role to level interfaces up and relax stresses and a-Ni–Al prevents Cu oxidized. Excellent structural and ferroelectric properties of the samples reveal that the inexpensive Ni–Al can be used as a multifunctional barrier material to integrate Cu with the silicon-based ferroelectric capacitors for the new generation devices. An oxygen diffusion barrier layer with thickness of 200 nm seems to be a blemish on this work because of a requirement of smaller device dimension for high density FeRAMs, so further work will be required to make the Ni–Al barrier between Cu and oxide film as thin as possible.

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