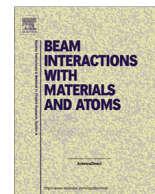




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The channeling effect of Al and N ion implantation in 4H–SiC during JFET integrated device processing

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ABSTRACT

A strong channeling effect is observed for the ions of Al and N implanted in 4H–SiC due to its crystalline structure. This effect causes difficulties in subsequent accurate estimation of the depth of junctions formed by multiple ion implantation steps. A variety of lateral JFET transistors integrated on the same 4H–SiC wafer have been fabricated. Secondary Ion Mass Spectrometry measurements and Monte-Carlo simulations were performed in order to quantify and control the channeling effect of the implanted ions. A technological process was established enabling to obtain devices working with the presence of the channeling effect.

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1. Introduction

Silicon carbide (SiC) is a wide bandgap semiconductor. The bandgap of the 4H–SiC (the most frequently polytype used in power electronic devices) is 3.27 eV, conferring higher thermal stability compared to conventional silicon. The thermal conductivity is also 3 times higher and the breakdown critical electric field approximately 10 times higher [1,2].

Power discrete SiC devices are already commercialized as Schottky diodes, BJT, JFET and MOSFET. A monolithic integration of this type of devices in SiC single crystal wafers is suitable to improve performance and reliability in power electronics. The size of the resulting converters is thus reduced, improving the switching operation and significantly decreasing the power loss.

For this purpose, structures must be fabricated involving a high number of specific technological steps as the plasma reactive-ion-etching (RIE) and doping by ion implantation. Due to the low values of diffusion coefficients of dopants in silicon carbide (SiC), ion implantation is required during fabrication of power SiC devices. Al and N are the typical dopants to form p and n-type layers in 4H–SiC.

In this work we fabricated a variety of 4H–SiC JFET transistors with lateral channel conduction (L-JFET). A considerable number of ion implantations of Al and N have been performed in order

to realize p and n-type wells under the contact electrodes, buried channels and other specific layers necessary to prevent the electric field increase inside the device. The distribution in the hexagonal 4H–SiC crystalline structures of the implanted ions and particularly the channeling effect [3] are critical for the JFET operation and their electrical output characteristics. Wafer and consequently crystal disorientation are imposed in order to minimize the channeling effect in 4H–SiC without being able to completely eliminate it [4]. In order to quantify and accurately control the depth of the implanted layers and the influence of the channeling effect of the dopant ions, we have performed a specific experimental study based on Secondary Ion Mass Spectrometry (SIMS) measurements and Monte-Carlo (MC) simulations. A number of batches of JFET transistors have been fabricated.

2. Experimental details

To avoid amorphisation, ion implantations have been performed at ~400 °C in disoriented 4H–SiC wafers. The tilt was 7° from the wafer normal and the rotation 90° with respect to the wafer flat, assuming a 8° off-axis surface and the wafer flat parallel to (1120). Multiple energy implants always started with the highest energy. To electrically activate the Al and N ion implanted dopants, post-implantation annealing at 1700 °C during 30 min has been performed in a RF-induction furnace with a C-cap [5]. The different structures are isolated by dry RIE etching using

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SF₆/O₂ chemistry and Ni based hard mask [6]. Ohmic contacts have been obtained using Ni for the back-side of the n⁺ substrate and on n⁺ wells, and using a specific Ni–Ti–Al alloy on the p⁺ wells [7]. These contacts have been annealed by Rapid-Thermal-Annealing under Ar at 900 °C and 800 °C, respectively.

The transistors fabricated in this process have been electrically characterized by current–voltage (*I*–*V*) measurements with a “Signatone S1160” probe station and “Keithley 2410” Source Measure Unit (SMU). Electrical characterizations were carried out at room temperature without a substrate bias.

3. First batches of SiC L-JFET

Lateral SiC-JFETs were fabricated on 4H–SiC epitaxial wafers, and JFETs with p and n-type channels have been obtained on individual n⁺ and p⁺ substrates (Fig. 1). The drift region between the drain and the source areas has a double RESURF (Reduced Surface Field) structure based on the super-junction theory [8]. These areas with the channel have been made by ion implanting.

Considering also the p⁺ and n⁺ wells under the contacts, a number of six ion implantations have been made, the type of doping of various layers depending on the type of transistor (n-channel or p-channel). The doping profiles have been obtained and optimized

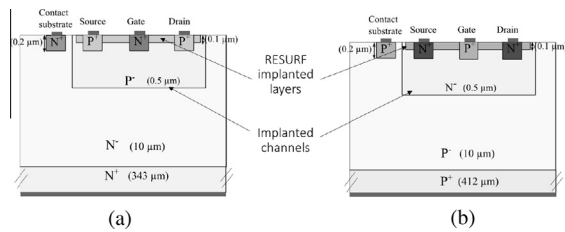


Fig. 1. Schematic presentation of the SiC L-JFET with, (a) p-type channel and (b) n-type channel.

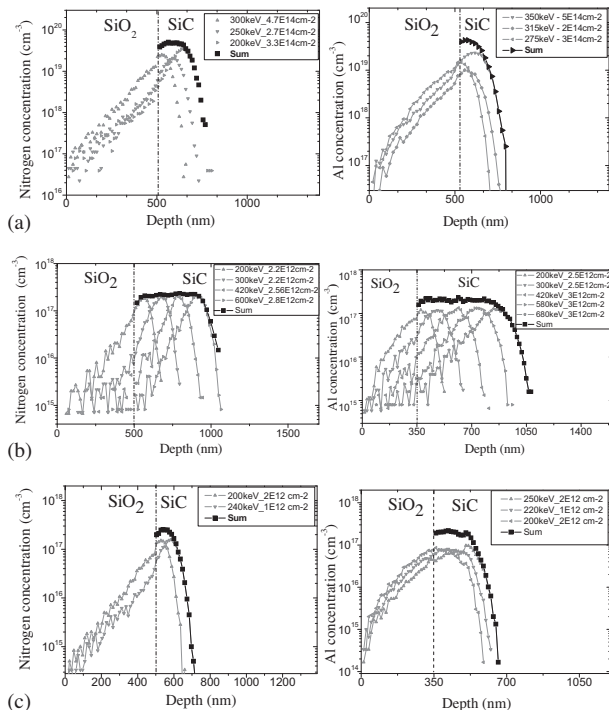


Fig. 2. Ion implantation parameters obtained by SRIM simulations for: (a) source, drain and gate of n⁺ and p⁺ wells, (b) n-type and p-type channels and (c) n-type and p-type RESURF layers.

by SRIM (Stopping and Range of Ions in Matter) Monte Carlo-type simulations [9]. The doping profiles are shown in Fig. 2.

During fabrication of the transistors from the first lot only one ion implanter accelerator 100–400 kV has been used. We created “box” profiles with multiple ion energies of Al and N over the ranges between 200 and 680 keV. Double charged ions have been implanted to avoid contaminations (¹¹B¹⁶O has the same mass as ²⁷Al). In order to obtain profiles close to the SiC surface a thin SiO₂ layer has been deposited onto the SiC samples. The thickness has been calculated by SRIM simulation considering the whole structure (SiO₂ and SiC).

Fig. 3 presents typical *I*_{DS}–*V*_{DS} electrical characteristics, plotted as a function of *V*_{GS}, for both n and p-type JFETs. We obtain a modulation of the channel resistivity by varying the *V*_{GS} gate–source bias only for the N-JFET. The drain saturation current is 6 mA at a gate voltage of 1 V. For the P-JFET the current is very small (in the μA range) and the p-type channel seems to be always blocked off. As we designed (600 V) power devices, structures with large distances between wells have been fabricated (in the order of 10 μm), leading us to the conclusion that the blocking behavior is not due to a lateral undermask penetration of ions which is limited to few micrometers [10].

The electrical characteristics obtained on the fabricated transistors determined us to analyze and reconsider the ion implantation parameters and the technological process employed. If high energy ion implantation is benefic to obtain deep channels it seems to be an impediment in the creation of isolated p⁺ and n⁺ wells in surface. High energies involve also high projected ranges (ΔR_p), and a spreading in the depth of the gate profiles. Moreover, the MC simulations with SRIM do not consider the crystalline structure of the 4H–SiC and consequently the presence of the channeling phenomenon was ignored. The channeling of the Al implanted ions in 4H–SiC is quite difficult to control and to eliminate even when an amorphous layer as SiO₂ is present in the surface [11]. Therefore the channel of the P-JFET seems to be obstructed and even hidden by the presence of the gate layer implanted at the surface, as Fig. 4 schematically presents.

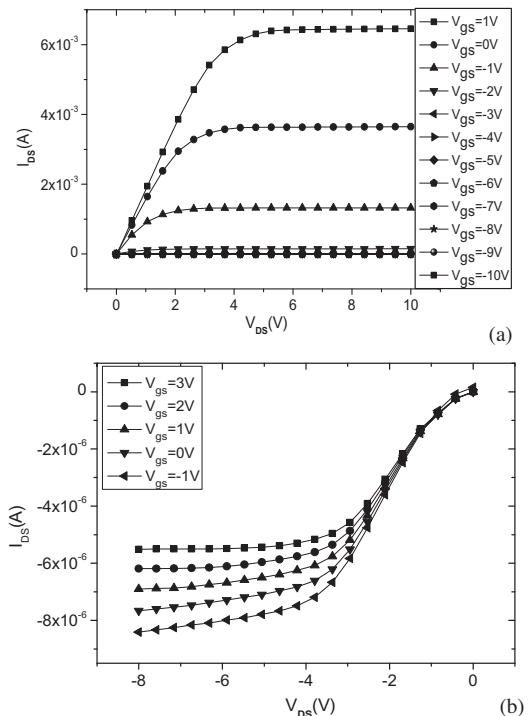


Fig. 3. Typical *I*_{DS}–*V*_{DS} versus *V*_{GS} characteristics of the (a) N-JFET and (b) P-JFET from the first batches.

The thickness of the channel is drastically decreased, and as an effect it strongly increases the on-resistances of the transistors.

4. Improved SiC L-JFET batches

For the second batches of L-JFET the technological process has been modified considering the analyses on the results we obtained on the first batches. Moreover, the final structures have been changed in order to integrate the P and N-JFETs monolithically on the same substrate. Two kinds of structures have been designed and fabricated: a low power structure and a high voltage structure (Fig. 5). For the high voltage structures the p and n-type channels are obtained by Al and nitrogen ion implantation whereas the channel conduction in the low power structures is directly ensured by the epitaxial CVD layers.

Prior to ion implantation the CVD epitaxial layers have been measured by SIMS in order to confirm their thickness and doping parameters. The spectra are presented in Fig. 6. The parameters furnished by the wafer's suppliers [12,13] have been confirmed.

Overall, only a number of four ion implantation steps have been performed: for the n^+ and p^+ sources, drains and gates wells under the electrode contacts and for the p and n-type channels in the case of high voltage structure. The RESURF layer in the surface has been eliminated in order to focus our study on the channel conduction.

The SiO_2 thin layer in the surface has also been eliminated which allowed us to utilize $I^2\text{SiC}$ [11] Monte-Carlo simulations which consider the crystalline structure of 4H-SiC.

Compared to SRIM, the $I^2\text{SiC}$ software could predict the channeling part of the doping profiles. An example is presented in Fig. 7 where SIMS measurements and $I^2\text{SiC}$ simulations spectra are compared for a “box” profile obtained by multiple Al ion implantation in 4H-SiC. An offset is observed in the channeling part, not more than 50 nm, probably due to material swelling at these high implanted doses and/or to the incertitude on the measured SIMS crater depth. We note that for our JFET devices, 50 nm is not a negligible percent of the channel depth.

In Fig. 8 we present the superposition of the optimized Al and nitrogen doping profiles of the gate and the channel, obtained by MC $I^2\text{SiC}$ simulations. Spectra are presented for both N-JFET and P-JFET integrated in the high voltage structure.

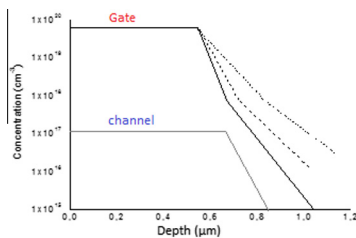


Fig. 4. Schematic presentation of the channel hidden by the gate implanted for the P-JFET.

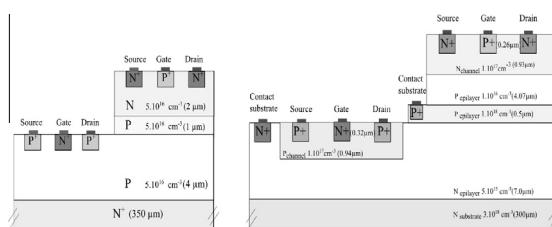


Fig. 5. Schematic presentations of the SiC L-JFET for the low power structure (on the left) and high voltage structure (on the right).

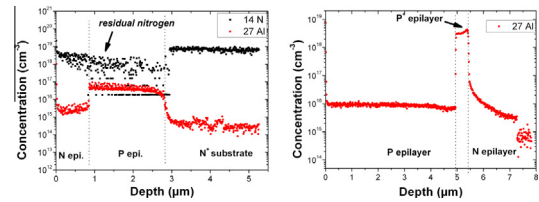


Fig. 6. Al and nitrogen doping profiles of the epitaxial CVD layers measured by SIMS on the low power structure (on the left) and high voltage structure (on the right).

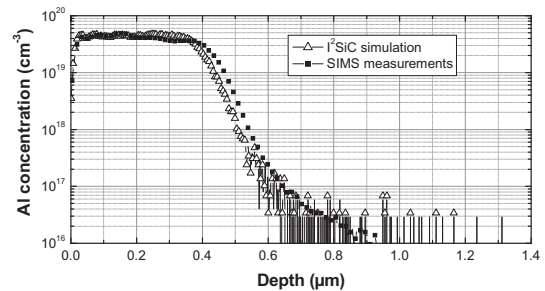


Fig. 7. Al ion implantation profile in 4H-SiC determined by SIMS measurements and $I^2\text{SiC}$ MC simulations.

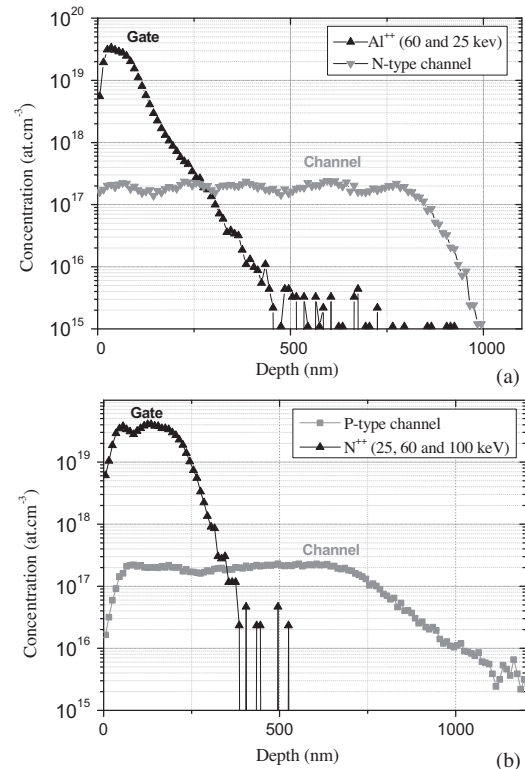


Fig. 8. Ion implantation parameters optimized by MC simulations with $I^2\text{SiC}$ for (a) N-JFET and (b) P-JFET from the high voltage structure.

Compared to the first batches, lower ion implantation energies could be used to create the p^+ and n^+ wells, thanks to the lack of the SiO_2 layer in surface. For the p^+ and n^+ wells we changed also the ion implanter accelerator, a medium current Eaton has been utilized. This allowed us to decrease the ion energies in the 25–60 keV for the Al and 25–100 keV for the nitrogen. Therefore lower ΔR_p values have been obtained for the multiple ion implants performed for the p^+ and n^+ gates.

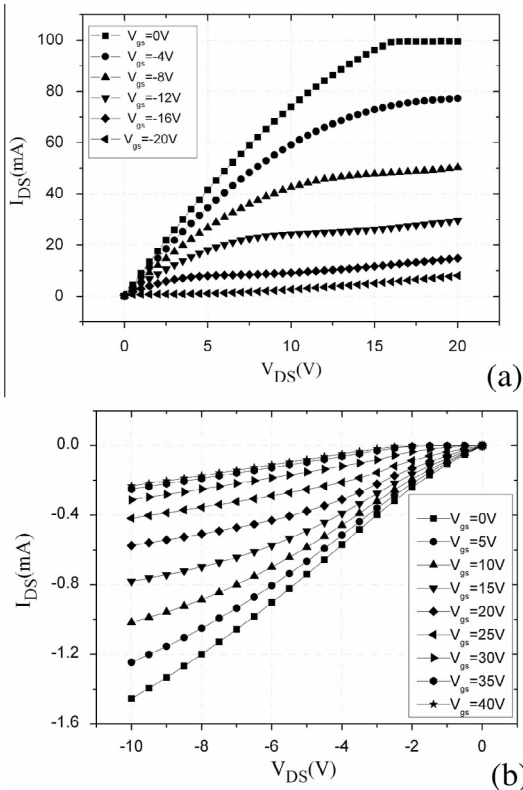


Fig. 9. Typical I_{DS} - V_{DS} versus V_{GS} characteristics of the (a) N-JFET (high voltage structure) and (b) P-JFET (low power structure) from the second batches.

Decreasing the thickness of the gates by decreasing the ion implantation energies and predicting the channeling part of the doping profiles allowed us to obtain thicker n and p-type channels. Fig. 9 shows the I_{DS} - V_{DS} electrical characteristics plotted as a function of V_{GS} for n and p-type JFETs from the second batches. The N-JFET is measured on the high voltage structure and the P-JFET on the low power structure. We can observe that even the electrical current through the n-type channel is increased. The drain saturation current is measured at 100 mA at a gate voltage bias of 0 V.

The conduction in the lateral P and N-JFET is improved by decreasing the channel resistances both by increasing the channel depths and by preserve the channel doping from the compensation which can occur from the channeling part of the gate doping.

Monolithically integrated P and N-JFET transistors with a normally-on conduction are obtained.

5. Summary

We fabricated various JFET transistors, with n and p-type channels, integrated on the same 4H-SiC wafer. A considerable number of ion implantations have been performed in order to obtain p and n-type wells under the contact electrodes, buried channels and other specific layers necessary to prevent the electric field increase inside the device. In order to quantify and control the influence of the channeling effect of the implanted ions, we have performed an experimental study based on SIMS measurements and MC simulations with a dedicated code considering the 4H-SiC crystalline structure. Several processing batches have been fabricated, and finally a new technological process was defined that enables to obtain P and N-JFET devices working within the presence of the channeling effect.

The number of ion implantation steps has been reduced. A particular effort has been done in order to carefully preserve the channel and avoid masking by the channeling part of the gate doping. The depth of the channels has been increased by implementing the highly doped wells for the gates in surface using low energy ion implantations while keeping high energy ion implantations for the realization of channels. For the low power structures the channels were not created by ion implantation, the channel conduction being ensured directly by the epitaxial CVD layers.

Limiting (but not eliminating) the channeling phenomenon in the hexagonal SiC, we showed that it becomes possible to fabricate on the same 4H-SiC wafer integrated and operating lateral JFET with even a p-type conduction channel. Increasing the tolerances of the structural device parameters (thickness and doping) allows us to obtained JFET transistors with a normally-on conduction.

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