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High performance top-gated indium-zinc-oxide thin film transistors with *in-situ* formed HfO_2 gate insulator

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Abstract:

We report on top-gated indium-zinc-oxide (IZO) thin film transistors (TFTs) with an *in-situ* formed HfO_2 gate dielectric insulator. Building on our previous demonstration of high-performance IZO TFTs with Al_2O_3/HfO_2 gate dielectric, we now report on a one-step process, in which Hf is evaporated onto the 20 nm thick IZO channel, forming a partially oxidized HfO_x layer, without any additional insulator in-between. After annealing in air at 300 ^oC, the *in-situ* reaction between partially oxidized Hf and IZO forms a high quality HfO_2 gate insulator with a low interface trapped charge density $N_{TC} \sim 2.3\times10^{11}$ cm^{-2} and acceptably low gate leakage < 3×10^{-7} A/cm^2 at gate voltage $V_G = 1$ V. The annealed TFTs with gate length $L_G = 50$ μm have high mobility ~95 $cm^2/V\cdot s$ (determined via the *Y*-function technique), high on/off ratio ~10^7, near-zero threshold voltage $V_T = -0.02$ V, and a subthreshold swing of 0.062 V/decade, near the theoretical limit. The on-current of our proof-of-concept TFTs is relatively low, but can be improved by reducing L_G, indicating that high-performance top-gated HfO_2-isolated IZO TFTs can be fabricated using a single-step *in-situ* dielectric formation approach.

Keywords: indium zinc oxide; top gate; *in-situ* process; thin film transistors; hafnium; HfO_2 gate insulator

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1. INTRODUCTION:

In the last ten years, amorphous oxide semiconductors have become important materials in the fabrication of high performance thin film transistors (TFTs). Such amorphous oxide semiconductors as In-Zn-O (IZO) and In-Ga-Zn-O (IGZO) have a large bandgap, relatively high mobility and can be deposited at room temperature, making them very competitive compared to amorphous Si technology [1-4]. High-performance TFTs should have a large on/off ratio, a threshold voltage close to zero, a sharp subthreshold slope and, ideally, a reasonably high on-current. While back-gated TFTs with thick insulators under the amorphous oxide channels can provide adequate performance, in order to make further progress a promising approach is to fabricate top-gated TFTs with high-quality gate insulators, which should have small interface trapped charge, high capacitance per unit area and low leakage. To fabricate high-quality gate insulators, one can reduce the gate insulator thickness, use high dielectric constant materials (such as HfO_2 or Al_2O_3) or use a multilayer gate stack [5-8].

In this paper, we improve on our previous demonstration of top-gated IZO TFTs using an *in-situ* formed dielectric layer [9] by turning to a one-step metal deposition process using Hf as the source of the *in-situ* reacted HfO_2 gate insulator. The channel material of our top-gated IZO TFTs consists of 90 wt.% In_2O_3–10 wt.% ZnO. The formation of dielectric gate insulator is based on the reaction between the metal and the IZO channel material at an intermediate temperature T ~ 200–300 ^oC in atmosphere. Metals (such as Hf and Al) that are thermodynamically unstable in contact with In_2O_3 will undergo solid state oxidation (in the absence of kinetic constraints) to produce a dielectric insulator layer (Al_2O_3 or HfO_2). The reaction between metal and IZO will consume oxygen from the IZO channel, leaving behind oxygen vacancies, or, in some configurations, oxidation of the metal may proceed via oxygen

diffusion from the atmosphere. To predict which metals can be used for *in-situ* dielectric formation by reacting with IZO, one can use the free energies of oxides to find the free energy change of overall reaction [10]. For example, the free energy of the reaction between Al and In_2O_3 ($2Al + In_2O_3 = Al_2O_3 + 2In$) can be found by subtracting free formation energy of In_2O_3 from free formation energy of Al_2O_3. At 200 ^oC, $\Delta G^R = \Delta G^F_{Al2O3} - \Delta G^F_{In2O3} = -752.6$ kJ/mol, the negative sign indicating that without any kinetic constraints, IZO will be chemically reduced by Al to form Al_2O_3. Several metals with suitable oxides can be similarly identified including: Al ($\Delta G = -752.6$ kJ/mol), Hf ($\Delta G = -807.6$ kJ/mol), Ti ($\Delta G = -509.7$ kJ/mol), and Mg ($\Delta G = -876.1$ kJ/mol). An additional consideration is the bandgap of the resulting oxide, which must provide the needed isolation between the gate metal and the IZO channel.

Previously [9], we reported top-gated IZO TFTs with *in-situ* formed Al_2O_3 interlayer between IZO channel and HfO_2 gate insulator (those TFTs will be referred as Al-TFTs in this paper). A schematic across-sectional view of those TFTs is shown in Fig. 1(a). There is a 2–3 nm thick sputter-deposited Al layer between IZO and HfO_2, deposited by atomic layer deposition (ALD). This Al layer protects the IZO channel from the oxygen ion bombardment damage during ALD-deposition of HfO_2. After annealing at 300 ^oC, the thin Al layer will be oxidized via reaction with IZO, forming an Al_2O_3/ HfO_2 gate stack. Those TFTs showed high mobility, high on/off ratio, and a good subthreshold slope [9]. However, a major disadvantage of using a thin layer Al between HfO_2 is the additional metal deposition step, which also necessitates addition lithographic alignment, increasing the fabrication process complexity.

In this report we present top-gated IZO TFTs by using Hf metal (those TFTs will be referred as Hf-TFTs in this paper) deposited in a single step, without any additional metal or dielectric deposition. The schematic across-sectional view of the Hf-TFTs is shown in Fig. 1(b). During

the Hf evaporation, the background pressure in the deposition chamber, while low (~3×10^{-3} Pa), is sufficient to partially oxidize the Hf. We believe that this partially oxidized material, when annealed, becomes fully oxidized HfO_2 near the IZO/HfO_x interface via a reaction with the IZO to produce a dielectric insulator layer that, as we shall demonstrate below, provides both low leakage and a manageable density of interface trapped charge N_{TC}. We demonstrate that these devices have promising performance, with excellent on-off ratio and sharp switching even for relatively long L_G = 50 μm TFTs, and small gate leakage currents.

2. EXPERIMENTAL PROCEDURE:

Both the Al-TFTs and Hf-TFTs shown in Fig. 1, were fabricated on a silicon wafer coated with 500 nm thermally grown SiO_2. All the source, drain and gate electrodes, as well as the IZO active area, were patterned by using optical lithography and lift-off processes. In the Al-TFTs of Fig. 1(a), 10 nm of Mo was sputtered at room temperature on the source and drain area. Then 10 nm of IZO was sputtered from a 90 wt.% In_2O_3-10 wt.% ZnO target at room temperature by dc magnetron sputtering with a power density of 0.22 W/cm^2, an Ar/O_2 volume ratio of 86/64 and a dc bias of 280 V. After deposition of IZO, a 2–3 nm Al layer was deposited at room temperature by using rf-sputtering. Then, 10 nm Mo, 10nm Cr and 70 nm Au were deposited on source and drain area using sputtering (Mo) and e-beam evaporation (Cr and Au). The HfO_2 dielectric layer was deposited by using ALD technique from a $Hf(N(CH_3)_2)_4$ precursor at 200 ^oC. Finally, the gate electrode (10/70 nm Cr/Au) was made using e-beam evaporation at room temperature. The width to gate length (W/L_G) ratio of the measured TFTs was 250/50 μm.

The Hf-TFTs, shown in Fig. 1(b), are also fabricated on a silicon wafer coated with 500 nm thermally grown SiO_2. Unlike the Al-TFTs, the 20 nm IZO channel was deposited directly on

SiO_2 using the same magnetron sputtering process (device isolation of finished TFTs was achieved by dilute HCl etching). The source and drain contacts consisted of sputtered 50 nm Mo, followed by 10 nm Cr and 100 nm Au deposited by e-beam evaporation. After that, Hf metal was deposited on the gate area by using e-beam evaporation, forming a partially oxidized HfO_x layer due to reaction with residual oxidants in the chamber, followed by 20 nm Cr and 70 nm of Au top gate metallization. Finally, a 24 nm layer of HfO_2 was deposited using ALD as a passivation layer. The width to gate length (W/L_G) ratio of the final TFTs was 200/50 μm.

Then the capacitance was measured on a Hewlett-Packard multi-frequency LCR meter (model 4275A), whereas the current-voltage characterization used Agilent 4155C semiconductor parameter analyzer.

3. RESULTS and DISCUSSION:

The as-deposited Al-TFTs and Hf-TFTs show good TFT characteristics only after anneal, because before annealing, Al-TFTs have a thin layer of Al metal shorting the source to the drain, whereas the Hf-TFTs do not have a high-quality gate dielectric/IZO interface. After anneal at 300 ^oC in air, gate capacitance was measured with an LCR meter in a light-tight box using a 100 kHz ac signal on both Al-TFTs and Hf-TFTs. During capacitance measurement, source, drain and substrate Si wafer are all connected and grounded together. The gate voltage V_G was swept from negative to positive and then backward. Figure 2 demonstrates the obtained C–V_G curves, normalized by the gate area. For the annealed Al-TFTs, when $V_G > 1$ V, capacitance reaches a maximum constant value C_{MAX} corresponding to the IZO channel in accumulation. Since we know the thickness of ALD-deposited HfO_2 to be 24 nm, the measured C_{MAX} yields a dielectric constant of HfO_2 of ~16 (with small uncertainty from the thin *in-situ* formed Al_2O_3 interlayer),

which is a reasonable number for ALD-deposited HfO_2. For the Hf-TFTs, shown in Fig. 2(b), a ~80 nm thick layer of Hf-rich material was deposited. This layer was shown by energy-dispersive X-ray spectroscopy to be substoichiometric HfO_x, which is unsurprising, as Hf is a highly efficient oxygen getter. Taking the corresponding C_{MAX} value at V_G = 1 V and assuming the dielectric constant to be 16, the thickness of *in-situ* formed HfO_2 layer is ~40 nm, meaning that only part of the 80 nm partially oxidized HfO_x layer became high-quality non-leaking HfO_2 layer with a good interface in contact with IZO.

Follow-on studies will investigate the chemical change between HfO_x and IZO before and during annealing. One particularly effective tool for this would be X-ray photoelectron spectroscopy, which, as described in elsewhere [11-13], can offer insight into the composition and structure of I(G)ZO thin films. The structure of our devices – thin IZO channel material covered by thicker HfO_x – will make these experiments quite challenging.

The hysteresis observed in the measured C–V_G curves of Fig. 2 makes it possible to estimate the interface trapped charge density $N_{TC} \sim C_{MAX} \times \Delta V_G/q$, where $\Delta V_G \sim 0.2$ V for annealed Al-TFTs and $\Delta V_G \sim 0.1$ V for annealed Hf-TFTs. For annealed Al-TFTs we obtain $N_{TC} \sim 7.2\times10^{11}$ cm^{-2}; for annealed Hf-TFTs, $N_{TC} \sim 2.3\times10^{11}$ cm^{-2}. Such N_{TC} values are much lower than reported results on HfO_2 insulator layers on IZO [14] and IGZO [6]. The annealed Hf-TFTs have smaller N_{TC}, and more interestingly, have opposite sign of trapped charge. The quality of annealed Hf-TFT interfaces and the charge-trapping mechanisms require further study, but the low N_{TC} values are promising for high-performance top-gated TFTs.

The TFT characteristics were measured using a semiconductor parameter analyzer in a light-tight box with the substrate grounded. Figure 3(a) shows the transfer curves of Al-TFTs, after annealing at 300 ^oC for 8 hours. The on/off current ratio exceeds 10^7 and the subthreshold swing

(SS) is 0.14 V/decade, with no measurable threshold shift as V_D is changed from 0.1 to 1 V. The gate leakage, which we evaluate at V_G = 1 V (corresponding to an electric field of ~ 0.4 MV/cm), is below 2×10^{-7} A/cm^2, 6 orders of magnitude below I_D at the same V_G. A thicker HfO_2 dielectric or optimized ALD deposition could be used to reduce the leakage to below 10^{-7} A/cm^2 [14]. More importantly, reducing L_G would decrease leakage and increase I_D, making the leakage negligible.

While the saturation mobility is often used for amorphous oxide TFT characterization [9, 15, 16], a more reliable value of channel mobility can be estimated by using the *Y*-function, which is widely used in MOSFETs [17]:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W}{L_G}\mu_0 C_{ox} V_D (V_G - V_T)}$$

where μ_0 is the low-field mobility, C_{OX} is the gate capacitance per unit area, and $g_m = \partial I_D/\partial V_G$ is the transconductance. Figure 3(b) shows the linear fit to the *Y*-function at V_D = 0.1 V, from which we extract a threshold voltage V_T = 0.23 V and a low-field mobility μ_0 ~ 135 cm^2/V·s.

The corresponding transistor characteristics of Hf-TFTs after 4 hours of annealing at 300 ^{o}C are shown in Fig. 4. Figure 4(a) shows the output I_D–V_D characteristics, with well-behaved current saturation (as well as indications of relatively high contact series resistance, which can be improved as in [18]). Figure 4(b) shows the transfer characteristics, taken at V_D = 0.1 and 1.0 V, together with the gate leakage current (of ~ 3×10^{-7} A/cm^2, evaluated at V_G = 1 V (corresponding to a field of ~ 0.3 MV/cm). Again, the leakage is very small compared to I_D and can be reduced further by optimizing the deposition conditions to improve the HfO_2 stoichiometry. The on/off current ratio is about 10^7 and no threshold shift is observed as V_D is changed from 0.1 to 1 V.

Figure 4(c) shows the *Y*-function extraction of the low-field mobility, estimated at 95 $cm^2/V{\cdot}s$, and the threshold voltage V_T = –0.02 V, in agreement with the C–V_G in Fig. 2(b).

A surprising feature of the transfer characteristics in Fig. 4(b) is the very good SS of 0.062 V/decade, which is near the room-temperature theoretical limit of $2.3k_BT/q$ = 60 mV/decade. This limit can only be reached if the capacitance of the dielectric layer HfO_2 is negligible compared to that of the IZO channel, whereas in our Hf-TFTs the thickness of the *in-situ* formed HfO_2 is ~40 nm, as inferred from the C_{MAX} value in Fig. 2(b) using a dielectric constant of 16. The explanation for such a good SS will require further study.

4. CONCLUSION:

We demonstrate the fabrication of top-gated IZO TFTs with an *in-situ* formed HfO_2 gate dielectric layer deposited in a single-step process. Those Hf-TFTs are compared with our previously fabricated Al-TFTs. The use of *in-situ* formed HfO_2 layer can simplify the TFT fabrication process (no additional deposition of gate dielectric layer). More importantly, the Hf-TFTs showed very high mobility ~95 $cm^2/V{\cdot}s$, high on/off ratio ~10^7, small V_T = –0.02 V, very low interface trapped charge density N_{TC} ~ 2.3×10^{11} cm^{-2}, a very sharp SS ~ 0.062 V/decade, and negligible gate leakage. The excellent observed SS requires additional study. The *in-situ* method of fabricating IZO TFTs shows promise of making high performance TFTs in a simple, low-temperature process.

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Fig. 1. (a) Schematic across-sectional view of as-deposited Al-TFTs with W/L_G = 250/50 μm; (b) schematic across-sectional view of as-deposited Hf-TFTs with W/L_G = 200/50 μm. Both types of devices are then annealed at 300 ^{o}C to form a high-quality gate dielectric of either Al_2O_3/HfO_2 (a) or HfO_2 (b) via metal-IZO reaction.

Fig. 2. (a) C–V_G curves of Al-TFTs after annealing at 300 ^{o}C for 8 hours; (b) C–V_G curves of Hf-TFTs after annealing at 300 ^{o}C for 4 hours. The insets show the cross sectional TEM images. The gate voltage V_G was swept from negative to positive then backward. The ac test signal is at 100 kHz.

Fig. 3. (a) Transfer I_D–V_G curves of Al-TFTs after annealing at 300 ^{o}C for 8 hours. Gate leakage I_G is also shown (total leakage on the left axis, leakage density on the right axis). (b) Y-function based on the transfer curve at V_D = 0.1 V, together with a linear fit (dashed line) from which the mobility can be extracted.

Fig. 4. Characteristics of Hf-TFTs after annealed at 300 ^{o}C for 4 hours. (a) Output I_D– V_D curves, with gate voltage V_G = –0.25 to 1.0 V with a step of 0.25 V. (b).Transfer I_D-V_G curves at V_D = 0.1 and 1.0 V, with gate leakage I_G also shown (total on the left axis, density on the right axis). (c) Y-function based on transfer curve at V_D = 0.1 V, with a linear fit to the Y-function shown with a dashed line.

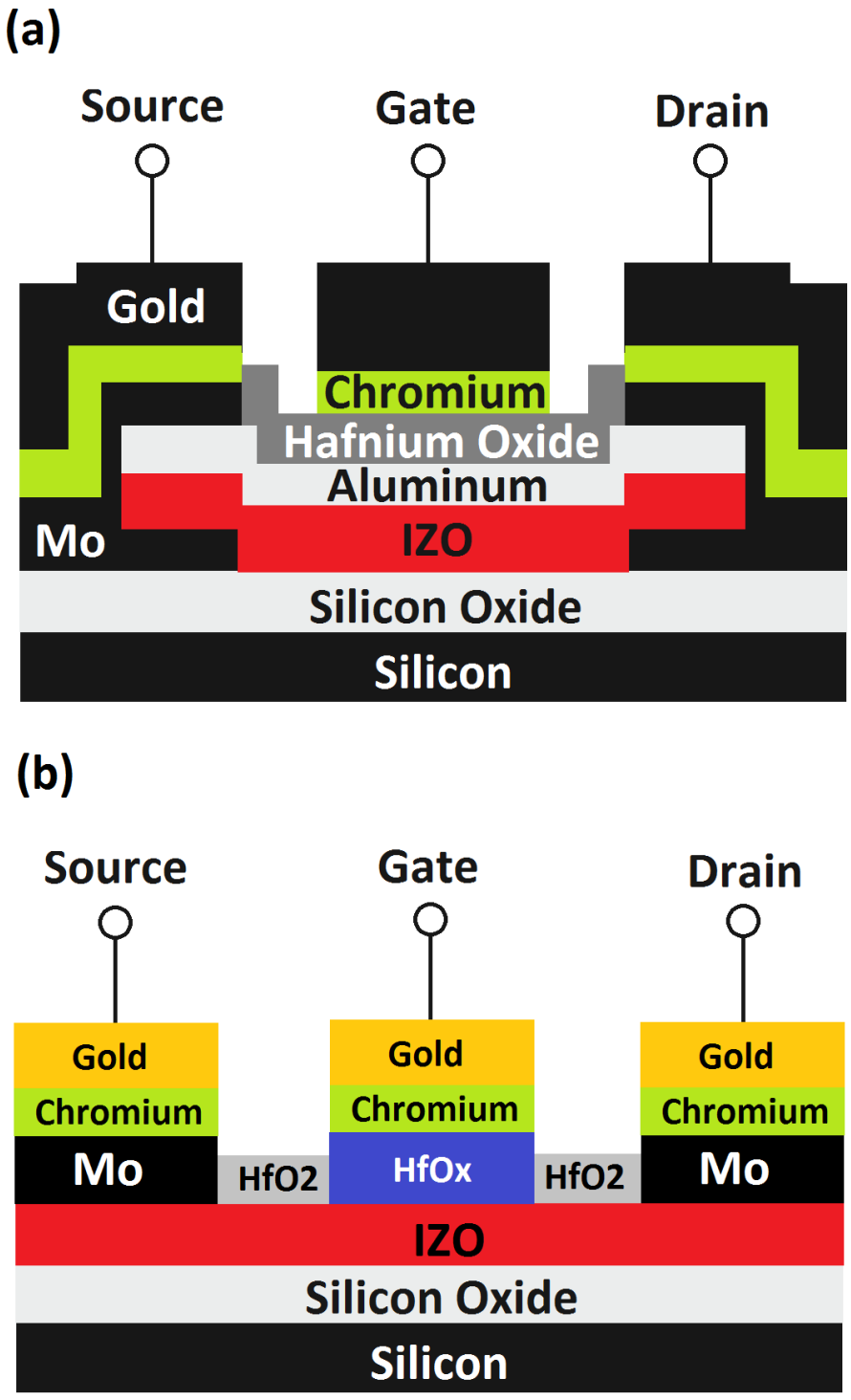

Figure 1

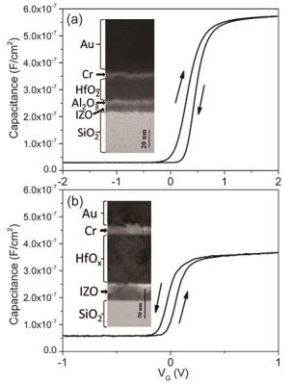

Figure 2

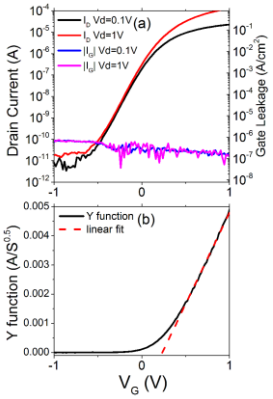

Figure 3

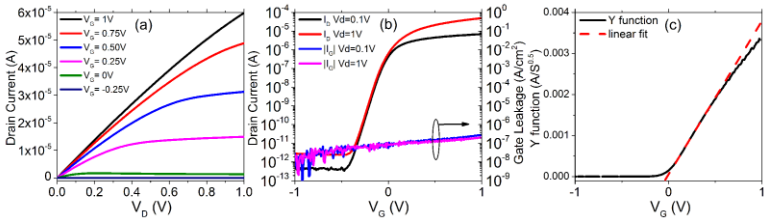

Figure 4

Highlights:

- High-performance indium-zinc-oxide (IZO) thin film transistors (TFTs).
- Single-step *in-situ* dielectric formation approach simplifies fabrication process.
- During anneal, reaction between HfO_x and IZO channel forms a high quality HfO_2 layer.
- Gate insulator HfO_2 shows low interface trapped charge and small gate leakage.
- TFTs have high mobility, near-zero threshold voltage, and a low subthreshold swing.