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# Fabrication and characterization of gold nanohole electrode arrays

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ABSTRACT

We report a fabrication method for gold nanohole electrodes array using photolithography, deep reactive ion etching, wet etching, and focused ion beam lithography techniques. The electrode arrays were fabricated by drilling of nanoholes on a 100 nm silicon nitride membrane over a large area of titanium/gold thin film, exposing disk-type gold nanoelectrodes at the base of holes. The electrode arrays were characterized using scanning electron microscopy (SEM), cyclic voltammetry (CV), and chronoamperometry (CA). SEM imaging of the arrays showed that the each hole is circular at the mouth and cone recessed disk (truncated cone) at the base. Near "steady-state" voltammetric behavior was achieved for the oxidation of 1 mM ferrocenedicarboxylic acid in 10 mM phosphate buffered saline (PBS) at these electrode arrays. The steady-state responses increase with increasing the number of nanoholes in the array. Because of good reproducibility, high accuracy, and miniaturization compatibility of the proposed fabrication technique, we believe that it has potential applications in developing portable devices for biosensing.


## 1. Introduction

The development of micro- and nanofabrication techniques makes possible the facile fabrication of nanoelectrodes. The use of nanoelectrodes in electrochemical studies and applications offer numerous advantages compared to planar macroscopic electrodes such as enhanced mass transport due to the dominance of radial (3 dimensional) diffusion, as well as decreased charging current and minimized adverse effects of uncompensated solution resistance [1]. Recent advances in nanotechnology have enabled fabrication of nanoelectrodes with different shapes and sizes that can be used in developing miniaturized and portable devices for applications in health care (*e.g.*, point-of-care devices for diagnostics) [2], on-site detection of explosives [3] and environmental pollutants [4].

Over the last decade, lithographic and non-lithographic techniques have widely been used for the fabrication of gold [5] and platinum [6,7] nanoelectrodes. For example, Shao et al., developed a non-lithographic technique for the fabrication of platinum nanoelectrodes by stretching metal wires sealed on glass using a laser-based micropipette puller [8]. This electrode was successfully employed to study heterogeneous electron-transfer kinetics by cyclic voltammetry (CV) and scanning electrochemical microscopy (SECM) techniques [9]. In another method, disk-type gold nanoelectrodes have been prepared using electrochemical deposition of gold onto platinum nanopore electrode [10]. Plasma enhanced chemical vapor deposition [11], chemical etching [5], self-assembly of gold nanoparticles have also been used to fabricate nanoelectrodes [12].

Lithographic techniques offer better process control during on-chip fabrication of nanoelectrodes compared to non-lithographic fabrication techniques in terms of reproducibility and robustness of the process, and provide potential of industrial up scaling. In recent years, electron beam lithography [13–16], nano-imprint lithography [15,16], and focused ion beam lithography (FIB) [14] have widely been used to fabricate devices with nanostructured substrates. Among these techniques, FIB is a rapid and versatile technique for fabricating nanostructured substrates with precise dimensions because of its direct writing capability over large surface areas [17]. Arrigan and his colleagues have used this technique to fabricate platinum nanopore electrodes [18] and silicon nitride nanopore membranes [19], with the later one used to study the ion transfer mechanism between two immiscible electrolyte solutions [19] and the former one employed to characterize diffusion profile located at the base of each nanopore [18]. In case of the former process, the thickness of deposited silicon nitride (*e.g.*, 400–500 nm) however limits the fabrication of sub-100 nm platinum nanoelectrodes at the base of the each pore due to the high aspect ratio of the pore [18]. To the best of our knowledge, there has been no report available for the fabrication of sub-100 nm electrode array on a 100 nm silicon nitride membrane in an open microchannel.

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Herein, we report a method for the fabrication of gold nanohole electrodes array (50 nm diameter) in an open microchannel. Our technique is based on the stress control of thin silicon nitride ($SiN_x$) membrane over a large area using thin layer of titanium/gold (Ti/Au) as support. A combination of photolithography, deep reactive ion etching, KOH etching, and FIB was used to fabricate these electrodes arrays. After fabrication, the electrodes were characterized by scanning electron microscopy, cyclic voltammetry and chronoamperometry.

## 2. Experimental

### 2.1. Fabrication

Silicon wafers (4″, 300 μm thick, prime grade, orientation 100, double-side polished) coated with 100 nm super low stress silicon nitride on both the sides (refractive index: >2.3, film stress: <100 MPa, low-pressure chemical vapor deposition (LPCVD)) were obtained from Micro Materials & Research Consumables (MMRC), Australia. The photomasks were designed using layout editor (L-Edit V15, Tanner Research Inc., CA) and printed onto 5″ × 5″ high precision emulsion plates (HRP-SN-2, Konica-Minolta, Japan) using flatbed photoplotter (MIVA 1624E T3, Miva Technologies GmbH, Germany).

The schematic representation of the fabrication of gold nanohole array is shown in Fig. 1. Briefly, the cleaned silicon wafer passivated with a 100 nm silicon nitride layer was further coated with positive photoresist (AZ1518, Microchemicals, Germany) to obtain a 2 μm thick resist layer, followed by soft bake for 10 min at 95 °C. The coated wafer was then UV exposed for 15 s (~250 mJ/cm$^2$) using a mask aligner (EVG620, EV Group GmbH, Austria), developed in AZ 326 developer solution (Microchemicals, Germany) for 30 s, followed by rinsing with deionized (DI) water (Millipore Pvt. Ltd., Australia) and dried under the flow of nitrogen ($N_2$) gas. A 200 nm gold with 10 nm titanium adhesion layer was then deposited on the wafers using a sputter coater, and patterned *via* a lift off process. Finally, the wafer was rinsed with IPA and dried under the flow of $N_2$ gas. A typical gold electrode was about 5 μm in width ($w$) and 600 μm in length ($l$) connected with relatively large pads of 2 mm × 2 mm. Gold alignment marks were also patterned on the wafer.

In the second lithographic step, back-side alignment was used to pattern SU8-2025 negative photoresist on the top side of the wafer as shown in Fig. 1(d). Briefly, SU8-2025 photoresist was spin-coated to obtain 20 μm thick layer, followed by soft backing for 3 min at 65 °C and 10 min at 95 °C. The SU8-2025 coated wafer was then exposed under UV for 35 s (430 mJ/cm$^2$) using the backside alignment technique with a mask aligner. The wafer was then post baked for 1 min at 65 °C and 10 min at 95 °C. Finally, SU8-2025 was developed in propylene glycol monoether acetate (PGMEA, Sigma Chemical, MO) followed by rinsing with IPA and drying under the flow of $N_2$ gas.

The SU8-2025 pattern acts as a protective mask during the deep reactive ion etching (DRIE) process, as shown in Fig. 1(f). The unprotected area in the wafer was etched using Versaline$^{TM}$ DRIE (Plasma-Therm, USA) system using $C_4F_8$ and $SF_6$ as reactive gasses. This process allows etching of 100 nm $SiN_x$ top layer and 220 μm of silicon to leave a silicon layer of ~80 μm thickness. After this step, the wafer was diced into 25 mm × 25 mm individual chips. The side with the gold electrode pattern was protected by bonding a glass cover slip (25 mm × 25 mm) using black wax. This step was designed to support the thin bottom $SiN_x$ layer. The chips were then placed in 30% solution of KOH in DI water containing 1% IPA at 80 °C for 90 min. The etching rate for silicon under these conditions was approximately 1 μm/min. The bottom silicon nitride layer acts as a hard mask for KOH with a slow etch rate. During this process, the SU8-2025 was detached from the chip as a thin film, which was then removed from the solution. The chips were then rinsed excessively with DI and dried under the flow of $N_2$ gas.

After this step, the underlying gold microelectrodes ($w \times l$ = 5 μm × 600 μm) were exposed, as shown in SEM micrographs (Fig. 2). Each chip was then subjected to sequential drilling (hole diameter ($d$) = 50 nm or radius ($r$) = 25 nm; center-to-center distance ($d_{cc}$) = 200 nm) using FIB technique (Helios Nanolab Dual Beam FIB/SEM). The parameters used to drill the nanoholes were as follows: dwell time of 25 ns, current of 1.5 pA. The nanohole arrays (3 × 3 and 10 × 10) with a hole density of 8 ($d_{cc}/r$) were drilled using gallium ion beam. As the silicon nitride layer was only 100 nm thick, a very low dose of ion beam was required to expose the gold electrode at the base of each nanohole. The nanohole arrays were imaged using the *in situ* SEM facility available with the FIB technique.

### 2.2. Electrochemical measurements

Cyclic voltammetric (CV) and chronoamperometric (CA) experiments were conducted at room temperature (22 ± 1 °C) in an open channel using an electrochemical analyzer CHI 730C (CH Instruments, Austin, TX), where nanohole electrodes array was used as a working electrode, a Pt wire counter electrode, and an Ag wire quasi reference electrode. The electrodes were electrochemically cleaned by cycling potential between −0.3 and +1.5 V in 50 mM $H_2SO_4$ until a stable voltammogram was obtained. The redox behavior of ferrocenedicarboxylic acid (FcDCA) (1 mM FcDCA in 10 mM PBS) was tested at the nanohole electrodes by CV and CA techniques. The effective working area of the clean nanohole electrodes array was determined under CV conditions for the one-electron reduction of ferrocenedicarboxylic acid (1 mM in 10 mM PBS) and by using Randles–Sevcik relationship [20].

## 3. Results and discussion

Gold nanohole electrode arrays were fabricated using a combination of techniques such as photolithography, DRIE, wet etching, FIB and stress control of $SiN_x$ membrane. A 100 nm layer of silicon nitride was used as the membrane in an open channel, while the nanoholes were patterned using FIB to expose the underlying gold nanoelectrodes at the base of each nanohole. Firstly, a photolithographic step was performed to fabricate an array of gold electrodes (5 μm × 600 μm) at the designated area of the wafer, as shown in Fig. 1. Subsequently, the negative photoresist SU8-2025 was patterned on the top side of the wafer by backside alignment between the gold electrodes and the alignment marks. The SU8-2025 pattern acts as a protective mask during DRIE process and defines the etching area of the wafer.

The dry etching step removes the top $SiN_x$ layer and a large fraction of the silicon, thus leaving an ~80 μm of silicon, which was finally etched during the wet etching step to expose the underlying silicon nitride layer. The formation of the silicon nitride layer was examined under SEM. As can be seen in Fig. 2A, SEM images for silicon nitride layer appeared as wide rough and wavy morphology. Furthermore, the gold microelectrodes patterned can also be seen through the insulating silicon nitride membrane (left of Fig. 2A). This insulating layer was useful to protect gold micro electrodes (5 μm × 600 μm) from the aqueous environment in the open channel.

The apparent rough and wavy morphology of the membrane was believed to be due to the stress on the membrane after release from the bulk silicon support and/or insufficient support provided by the black wax backing. The residual stress of the $SiN_x$ films can be

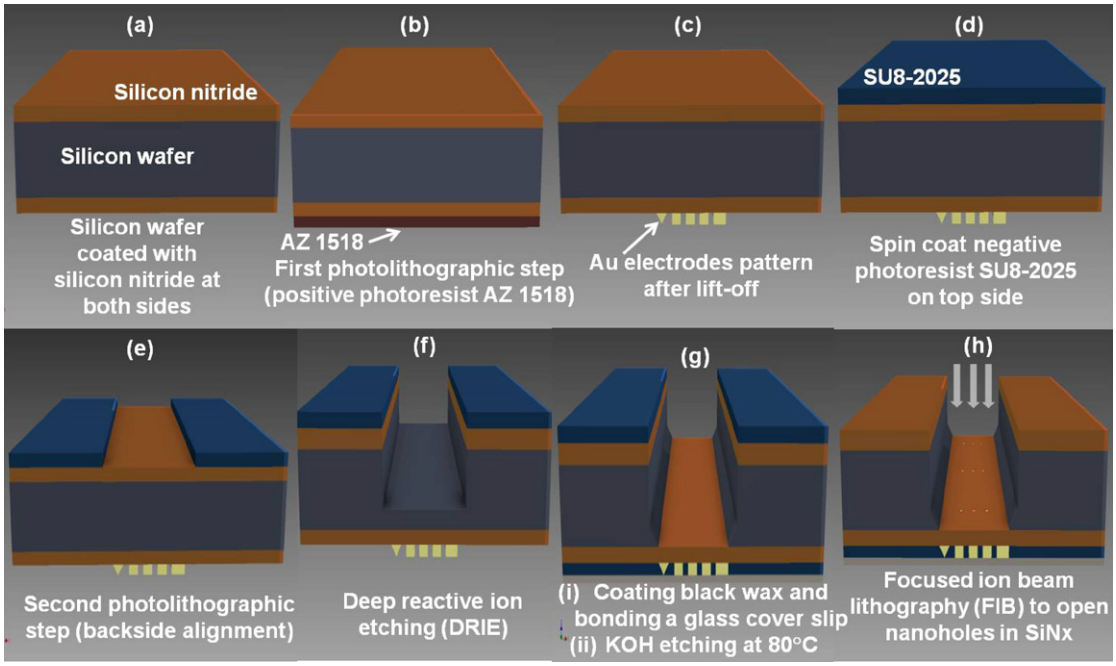


**Fig. 1.** Schematic view of the fabrication process for the fabrication of gold nanoelectrodes using thin silicon nitride membrane as an insulator.

compressive or tensile, depending on the parameters used in the deposition step (temperature, total pressure, and ratio of the gas flow rates) [21]. However, the morphological characteristic of the membrane (*e.g.*, surface characteristics) can be improved by controlling the stress values during the deposition, which is a tedious method. In the present work, we have used a relatively straightforward method to overcome this problem. We designed a large bed of gold and inter electrode gold supports along with the gold electrodes, with no interfacial connection with the electrodes, while providing sufficient support to the thin $SiN_x$ membrane (Fig. 2B). The distance between the gold electrodes and the gold support was 20 μm. The rationale behind this approach was dictated by our observations that the $SiN_x$ membrane was remarkably smooth over the gold microelectrodes. After repeating all the fabrication steps as described above, we observed significant improvement in the morphology of the thin $SiN_x$ membrane (Fig. 2B). It has been reported that the metal layers deposited on to the silicon substrates generally impose tensile stress [22]. We hypothesized that the tensile stress of deposited metal layers of Ti/Au compensated the residual stress in $SiN_x$ membrane, thereby stabilizing the membrane and provided excellent flatness to the membrane. This interesting fact discovered in our current study can offer a new method of supporting $SiN_x$ membrane on a large area.

After using the new fabrication scheme to generate a batch of chips, we subsequently fabricated gold nanoelectrode arrays by drilling nanoholes in the $SiN_x$ membrane and exposing the gold electrodes underneath the membrane. A low dose of Gallium ions was required to make nanoholes on the 100 nm thin $SiN_x$ membrane. Fig. 3 shows SEM images of the $3 \times 3$ and $10 \times 10$ nanoholes fabricated using FIB with each nanohole of nominal diameter of 50 nm. The average diameter of the fabricated nanoholes in a $3 \times 3$ array was 49.8 nm with the relative standard deviation

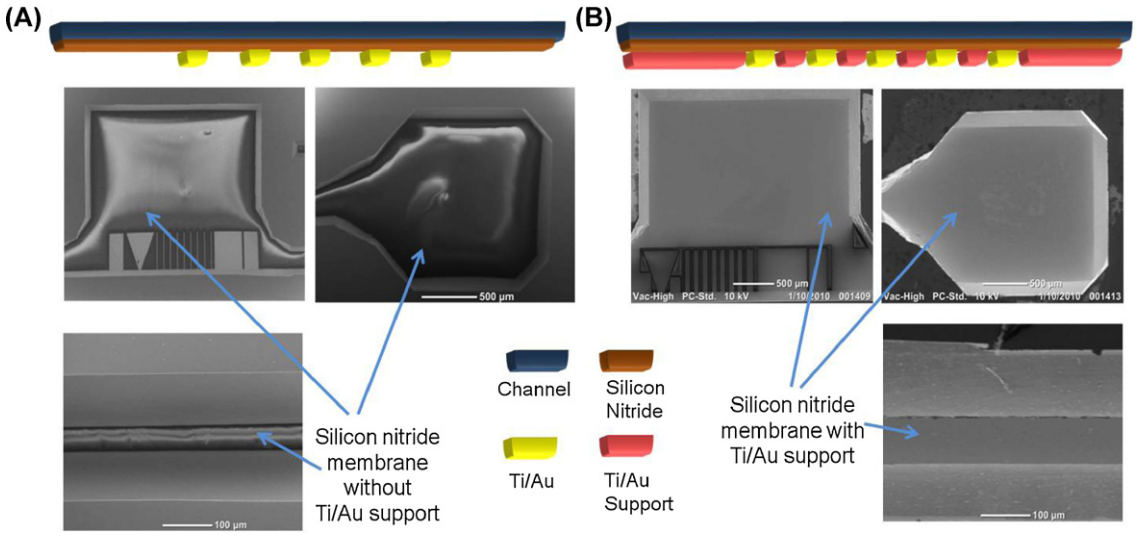


**Fig. 2.** Schemes and scanning electron microscopy images of gold electrodes after KOH etching without (A) and with (B) extra gold pattern to support $SiN_x$ membrane. In these schemes, five working electrodes were shown for simplicity.

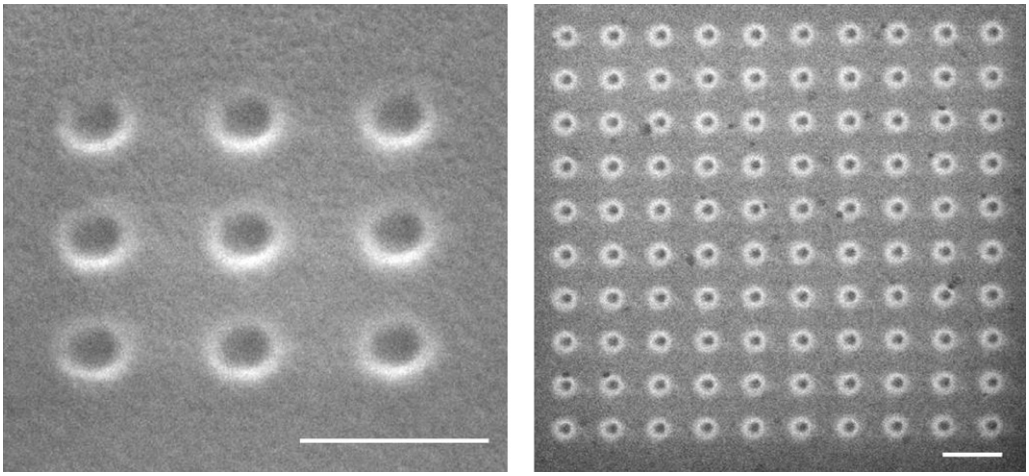

**Fig. 3.** Scanning electron microscopy images of the nanohole array gold electrodes fabricated using FIB. (Left) a 3 × 3 nanohole array, the scale bar is 250 nm. (Right) 10 × 10 nano-hole array, the scale bar is 250 nm.

(% RSD) of 2.5% ($n$ = 9). This diameter in a 10 × 10 array was 48.9 nm with the RSD of 4.2% ($n$ = 100). The reproducibility of the nanohole fabrication process was calculated by measuring the overall nanohole diameters in three separate arrays fabricated in three different batches. The RSDs of these measurements were found to be 3.06% and 6.30% ($n$ = 3) for the 3 × 3 and 10 × 10 array electrodes, respectively, indicating the nanohole fabrication process was reproducible. It is clear from the SEM micrographs that the nanoholes are disk-shaped thereby resulting in the disk-type gold nanoelectrodes underneath. The areas, which were not exposed to the ion beam continued to act as passivation mask, thus defining the gold nanoelectrodes.

These nanohole electrode arrays were characterized by electrochemical measurements. Initially, the electrodes were electrochemically cleaned by cycling the potential between −0.3 and +1.5 V in 50 mM $H_2SO_4$. The formation of the gold oxides at electrode surface generated a reduction peak during the reverse scan of this process (*e.g.*,+1.5 to −0.3 V). Fig. 4A shows a typical reduction peak at 0.6 V (*vs.* Ag wire), corresponds to the reduction of gold oxides at both the 3 × 3 and 10 × 10 electrode arrays with relative standard deviation (RSD) of <5% ($n$ = 5). During this cleaning process, an increased reduction peak current was observed at the 10 × 10 array (Fig. 4A(red)), as expected for a larger electrode array (3 × 3 *vs.* 10 × 10 arrays). By measuring the area under the gold oxide reductive peak, it is possible to determine the electroactive surface area of the gold recessed nanoelectrode arrays. Using the literature value of 450 μC cm$^{-2}$ [23] for the charge passed per unit area on the surface of bulk gold, we estimated the electroactive surface area of the gold recessed nanoelectrode arrays for 3 × 3 and 10 × 10 electrode arrays. The electrode area calculated by this method was found to be about 30 times higher than the geometric areas of 3 × 3 and 10 × 10 electrode arrays. These findings are in line with the previously reported data where a 10–20 times higher values of the electrode areas were reported for nanowell electrode arrays [24].

The redox behavior of the $FcDCA^{0/+}$ process ($FcDCA + e^- \rightleftharpoons FcDCA^+$) in 10 mM PBS has been examined at the nanohole electrodes by using CV and CA techniques. Fig. 4B shows a near 'steady-state' limiting current ($I_{lim}$) for the oxidation of 1 mM FcDCA in 10 mM PBS at the 3 × 3 electrode array (RSD = <5%, $n$ = 5), indicating that the geometry of the nanohole electrodes at the base of the hole is cone recessed disk (truncated cone), as described previously by Arrigan et al. [18]. According to the Arrigan et al.'s model, the $I_{lim}$ value for the oxidation of ferrocenecarboxylic acids at nanopore electrode arrays with truncated cone geometry can be defined as [18]:

$$I_{lim} = \frac{[4\pi nFCDr_L(r_L - L\ \tan\alpha)]}{[4L + \pi(r_L - L\tan\alpha)]} \quad (1)$$

where $n$ is the number of electrons transferred per molecule in the electrochemical reaction, $F$ is the Faraday constant, $D$ is the diffusion coefficient, $C$ is the bulk solution concentration of the redox active species, $r_L$ is the radius of the mouth of the hole, $L$ is the recess depth of the hole, and $\alpha$ is the wall angle. Using the $I_{lim}$ value, $L = 1 \times 10^{-5}$ cm, and $\alpha = 3^\circ$ (*e.g.*, FIB producing wall angle of 2–10° [18] for 3 × 3 electrode array, the $r_L$ was found to be very similar to that obtained by SEM measurements (*e.g.*, $2.25 \times 10^{-5}$ cm, the radius of the mouth of each hole is 25 nm). These results again indicate that the diffusion profile of the nanoelectrodes follow the Arrigan et al.'s [18] model for cone recessed disk (truncated cone) geometry.

Fig. 4B and C provides a comparison of the $I_{lim}$ value obtained at the 3 × 3 and 10 × 10 electrode arrays for the oxidation of FcDCA in 10 mM PBS using both the voltammetric and amperometric technique. Clearly, the value of $I_{lim}$ is a function of the number of nanohole electrodes in the array. The effect of the scan rates on the $I_{lim}$ value has also been studied at these electrodes (Fig. 4D). As expected for disk-type microelectrodes [18], the $I_{lim}$ value is independent over the range 5–100 mV/s with departures at high scan rates. The departure in $I_{lim}$ at higher scan rates is attributed to the presence of the radial diffusion, which clearly indicates that at the higher scan rates the response is controlled by diffusion to the pore mouth rather than to the bottom disk-type electrode [18].

Finally, the double layer capacitance ($C_{dl}$) per unit area for the electrode in 1 mM FDCA (in 10 mM PBS) was obtained from voltammetric profiles by plotting the capacitance current ($I_c$) at a selected potential range where no Faradaic current is evident *vs* the scan rate ($\upsilon$). Under ideal conditions, the relationship $I_c = AC_{dl}\upsilon$ exists [25], where $I_c$ is the charging current, $A$ is the electrode area (cm$^2$), and $C_{dl}$ is the capacitance of the double layer per square centimeter. Thus, $C_{dl}$ may be calculated from the slope of a plot of $I_c$ *vs* $\upsilon$. A linear $I_c$ *vs* $\upsilon$ relationship with $C_{dl} = 2.3 \times 10^{-2}$ μF cm$^{-2}$ was found to apply over the potential range of 100–250 mV *vs* Ag wire (data not shown). Similar experiments have been undertaken at the nanohole array electrode in the absence of FDCA over the potential range of 100–600 mV *vs* Ag wire and $C_{dl}$ was calculated to be $2.2 \times 10^{-2}$ μF cm$^{-2}$. These results indicate that the presence of the

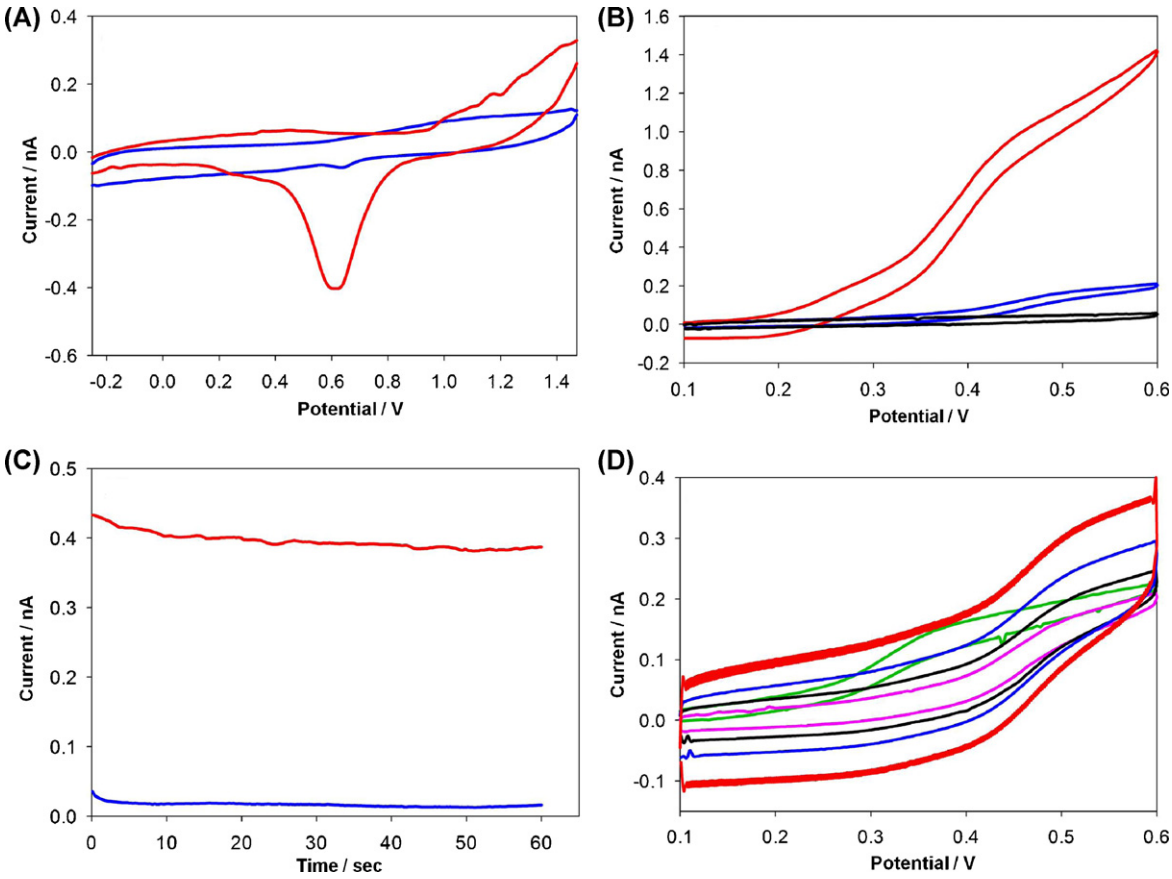


**Fig. 4.** (A) Cyclic voltammogram of 50 mM $H_2SO_4$ at 10 × 10 (red) and 3 × 3 (blue) nanoelectrode array recorded at a scan rate of 25 mV/s; (B) cyclic voltammograms of 1 mM ferrocenedicarboxylic acid in 10 mM PBS at 10 × 10 (red) and 3 × 3 (blue) nanoelectrode arrays recorded at a scan rate of 10 mV/s, and 3 × 3 nanoelectrode array response to 10 mM PBS only (black) at a scan rate of 10 mV/s; (C) amperometric *i–t* curves at 0.350 V *vs.* Ag wire at 3 × 3 and 10 × 10 nanoelectrode arrays for 1 mM ferrocenedicarboxylic acid in 10 mM PBS; (D) the influence of increasing scan rate [5 (green),10 (purple), 25 (black), 50 (blue) and 100 (red)] mV/s on the $I_{lim}$ measured for 1 mM ferrocenedicarboxylic acid in 10 mM PBS at 3 × 3 nanoelectrode array.

nanohole electrodes did not change the $C_{dl}$ of the structure, which is again in good agreement with previously published observation [18]. In both cases, however, the capacitance was normalized to the geometric areas of the recessed electrodes, and ignored any contributions from stray capacitance due to the $SiN_x$ contaminant, on-chip metal pads, *etc.*

## 4. Conclusions

We fabricated gold nanohole electrode arrays (sub-100 nm) using combination of photolithography, deep reactive ion etching, wet chemical etching, and focused ion beam lithography in an open microchannel. We have also demonstrated that a thin metal layer deposition of Ti/Au reduces the stress on $SiN_x$ and provides excellent support to the thin $SiN_x$ films over a large area. The electrochemical characterization of the gold nanohole electrodes array exhibited typical voltammetric responses for the oxidation of FcDCA at electrodes with cone recessed disk (truncated cone) geometry, which confirmed the successful fabrication of the electrode array. The fabrication scheme presented in this work could be considered as a general method for the fabrication of thin $SiN_x$ membrane based nanohole electrodes array. The level of the reproducibility and robustness of the fabrication process coupled with inherent advantages of nanoelectrodes renders it a promising methodology for fabricating metal nanostructured electrodes in sub-100 nm regime.

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