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Analysis of efficiently poled electro-optic polymer/Tio_2 vertical slot waveguide modulators

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ABSTRACT

We analyze the advantages of an electro-optic (EO) polymer/TiO_2 vertical slot waveguide modulator based on a low-index EO polymer (SEO125). This modulator can realize a lower half-wave voltage (V_π)-electrode length (L_e) product ($V_\pi L_e$) when compared with hybrid EO polymer (EOP)/sol–gel silica waveguide modulators because of the high mode confinement of the guided light and the high poling efficiency. We show the enhancement of the poling efficiency in these devices when the EO polymers are poled with TiO_2 and sol–gel silica layers. We also enhance the EO coefficient to a level of 260 pm/V at a wavelength of 1.31 μm for a high-index EOP (SEO100) deposited on TiO_2, a sol–gel silica cladding layer, and an additional interfacial layer.

1. Introduction

Polymer modulators have been the only optical modulators to have bandwidths of >60 GHz, with a widest reported bandwidth of 113 GHz, because of the low dielectric dispersion of the electro-optic polymers (EOPs) used in these devices [1]. We have previously demonstrated a low half-wave voltage (V_π) in the 0.65–1.0 V range [2,3] with relatively low optical propagation loss of 5 dB/cm, using a hybrid EOP/sol–gel (SG) silica waveguide modulator with an in-device electro-optic (EO) coefficient of 142 pm/V at a wavelength of 1550 nm. The $V_\pi L_e$ product (where V_π is the half-wave voltage, and L_e is the electrode length) is considered to be an appropriate figure of merit (FOM) for a complementary metal-oxide-semiconductor (CMOS)-compatible integrated optical modulator for optical interconnections based on Si modulators [4–8]. Only a few reports on Si modulators have focused on the optical losses for realistic applications. A combination of the FOM and the optical loss can be defined as a more realistic FOM as the $V_\pi Loss$ product [V dB], in which $V_\pi L_e$ [V cm] was multiplied by the optical propagation loss [dB/cm] in the active region (phase shifter). Our hybrid polymer modulator has a $V_\pi L_e$ product of 1.56 V cm and a $V_\pi Loss$ product of 7.8 V dB in the hybrid EOP/SG silica waveguide modulator [2]. To the best of the authors' knowledge, one of the best reported Si modulators to date showed a $V_\pi L_e$ product of 0.78 V cm and a $V_\pi Loss$ product of 6.7 V dB [4], although other Si modulators showed $V_\pi L_e$ products of 1–3 V cm with higher $V_\pi Loss$ products of >27 V dB [5–8]. Other CMOS compatible modulators include the III–V electro-absorption modulator (EAM) with a bandwidth of 52 GHz [9], EOP/Si slot waveguides, and EOP/Si photonic crystal (PC) waveguide modulators [10–14], and the properties of these devices are summarized in Table 1.

EOP/Si slot waveguide modulators were demonstrated based on coplanar Si slot waveguides [11–13], in which no optical modes exist in the high-index Si; instead, the waveguide mode was confined within the low index EOP between the Si slots, because the Si size is critically reduced to a less than single mode condition ($\lambda/2n_{effective}$), where λ is the wavelength and $n_{effective}$ is the effective refractive index of the waveguide. EOP/Au slot waveguide modulators were demonstrated using Au plasmonic slot waveguides. For actual application of these devices to optical interconnections, the optical propagation loss must be further reduced, and another FOM, the $V_\pi Loss$ product, must also be considered. We have demonstrated an all-dielectric EOP/TiO_2 multilayer vertical slot waveguide modulator for the first time [15] that provides higher poling efficiency, a wider EO modulation bandwidth and lower optical propagation losses without using highly-doped Si layers that limit device performance. We reduced the $V_\pi L_e$ product to 2 V cm and the $V_\pi Loss$ product to 14 V dB by using low-index EOP (SEO125, with refractive index of 1.621, and in-device EO coefficient $r_{33}=78$ pm/V at a wavelength of 1.55 μm), based on the enhanced conductivity of the SG silica under a cladding layer [16]. In this modulator, the enhanced conductivity of the SG silica under

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Table 1
CMOS-compatible optical modulators.

Type	$V_\pi L$ [V cm]	Loss	$V_\pi Loss$ [V dB]	3 dB-BW [GHz]	r_{33}	Ref.
EOP/SG	1.56	5	7.8		142	2
Si	0.78	6.6	6.7		–	4
Si	1	31	31		–	5
Si	1.4	19	27	12(1 mm) 30 (0.25 mm)	–	6
Si	3.5	12	42	15	–	7
Si	2.7	10	28	26	–	8
III–V (EAM)	0.022	49	52	74	–	9
EOP/Si PC	0.029	–	–		89	10
EOP/Si slot	0.5	–	–		30	11
EOP/Si slot	0.052	60	3.12	10	230	12
EOP/Si slot	1.1	60	66		18	13
EOP/Au slot	–	4000	–		21	14
EOP/TiO_2 slot	2	7	14		78	16

Loss: Optical loss [dB/cm].

cladding realized efficient poling of the EOP with a selective TiO_2 layer. We also demonstrated high EO coefficients of 226 and 198 pm/V at wavelengths of 1.31 and 1.55 μm, respectively, for an efficiently poled high refractive index EOP film of SEO100 deposited on a TiO_2 selective layer and SG silica cladding [17]. In this paper, we analyze the advantages of EOP/TiO_2 slot waveguide modulators for further reduction of the $V_\pi L_e$ product when compared with hybrid EOP/SG silica waveguide modulators.

2. EO polymer/TiO_2 slot waveguide modulators

2.1. Analysis and demonstration of EO polymer/TiO_2 vertical slot waveguide modulators

Mach–Zehnder-type EOP/TiO_2 multilayer slot waveguide modulators were fabricated using a 0.3–0.6-μm-thick EOP layer sandwiched between two 0.1-μm-thick TiO_2 thin film layers. A cross-sectional view of a 4-μm-wide Mach–Zehnder-type waveguide used in the modulator is shown in Fig. 1(a). A standard hybrid EOP/SG silica waveguide modulator is also shown in Fig. 1(b) [2]. The half-wave length V_π is expressed as

$$V_\pi = \frac{\lambda d_{effective}}{2n^3 r_{33} L_e \Gamma} \quad (1)$$

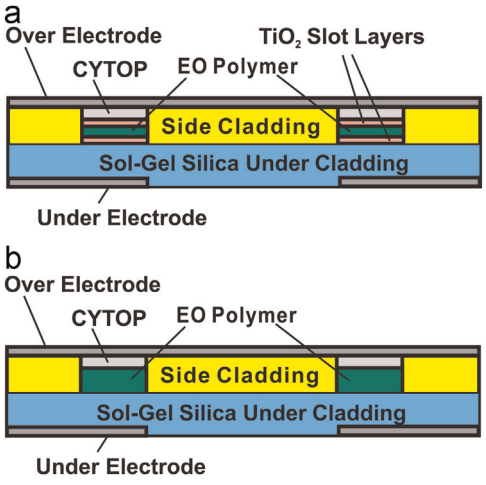

Fig. 1. Schematic cross-sectional views of active regions. (a) EOP/TiO_2 multilayer vertical slot waveguide modulator. (b) Hybrid EOP/sol–gel silica waveguide modulator.

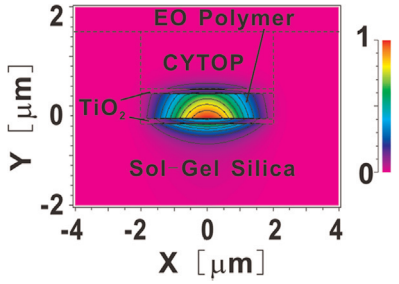

Fig. 2. One mode profile for the thickness of the EOP (t_{EO}) of 0.5 μm in the electro-optic polymer/TiO_2 vertical slot waveguide modulator.

$$d_{effective} = d_{EO} + \sqrt{\varepsilon_{EO}/\varepsilon_{TiO_2}}\, d_{TiO_2} + \sqrt{\varepsilon_{EO}/\varepsilon_{CYTOP}}\, d_{CYTOP} + \sqrt{\varepsilon_{EO}/\varepsilon_{SG}}\, d_{SG} \quad (2)$$

where $d_{effective}$ is the effective electrode distance, n is the refractive index of the active material, and Γ is the mode overlap integral between the optical wave in the active region and the applied electric field. ε_{EO} (~3), ε_{TiO2} (>30), ε_{CYTOP} (~2), and ε_{SG} (~3) are the dielectric constants for the EOP, TiO_2, CYTOP and SG layers, respectively. d_{EO}, d_{TiO2}, and d_{CYTOP} are the thicknesses of the EOP, TiO_2 and CYTOP layers, respectively. Because the TiO_2 layer thickness is 0.1 μm, the term d_{TiO2} can be neglected. The thicknesses of the SG silica layer under cladding and the CYTOP layer were 4 μm and 1.2 μm, respectively. The refractive indices of the SEO125 EOP, TiO_2, CYTOP, and SG silica cladding layers were 1.621, 2.567, 1.328, and 1.487, respectively. As a first step, the mode profile in the slot waveguide was calculated using the three-dimensional finite-difference time domain (3D FDTD) method. One mode profile for the thickness of the EOP (t_{EO}) of 0.5 μm was shown in Fig. 2. Γ/d_{eff} with respect to the t_{EO} was obtained from the result for the profile as shown in Fig. 3.

Next, the $V_\pi L_e$ products of the EOP/TiO_2 slot waveguide modulators and those of standard hybrid modulators were calculated from the in-device r_{33} value of 70 pm/V and the obtained value of Γ. The dependence of the $V_\pi L_e$ product for the slot waveguide modulator (see Fig. 1(a)) on the EOP thickness was obtained for 1-μm-thick and 4-μm-thick SG silica under cladding layers, as shown in Fig. 4. The same dependence of the $V_\pi L_e$ product for a standard hybrid modulator (see Fig. 1(b)) was also obtained for comparison. When t_{sg} is 4 μm, the slot waveguide modulator does

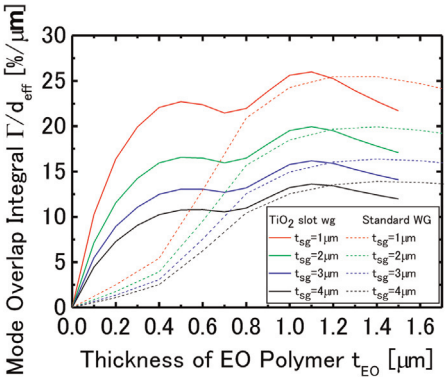

Fig. 3. Normalized mode overlap integral Γ between the optical mode and the applied electric field divided by the effective electrode distance $d_{effective}$ with respect to the thickness of the EOP layer, t_{EO}. The solid lines (EOP/TiO_2 vertical slot waveguide modulators) in red, green, blue, and black show the results for SG silica thicknesses under cladding of 1, 2, 3, and 4 μm, respectively. The dotted lines (standard hybrid EOP/SG silica waveguide modulators) in red, green, blue, and black show the results for SG silica thicknesses under cladding of 1, 2, 3, and 4 μm, respectively. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

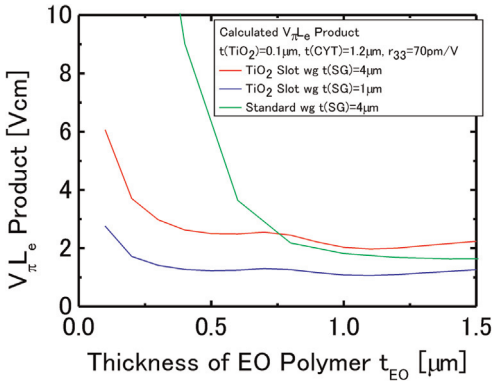

Fig. 4. $V_\pi L$ product with respect to the EOP (SEO125) thickness, as calculated by the 3D FDTD method. The thicknesses of the TiO_2 and CYTOP layers are 0.1 and 1.2 μm, respectively. $r_{33}=70$ pm/V. Red and blue lines show the product values for EOP/TiO_2 slot waveguide modulators with sol–gel silica layer thicknesses under cladding of 4 and 1 μm, respectively. The green line shows the product for the standard hybrid EOP/sol–gel silica waveguide modulator. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

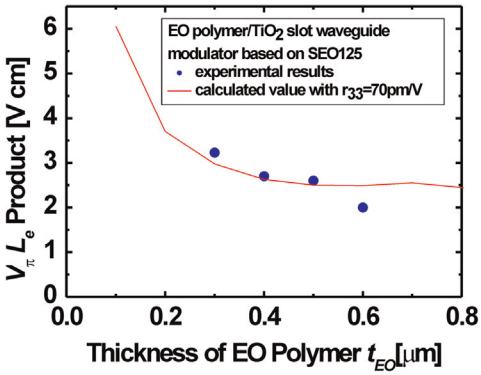

Fig. 5. $V_\pi L_e$ product with respect to the thickness of the EOP (SEO125). Blue closed circles denote the experimental results and the red line shows the result calculated by the 3D FDTD method. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

not show any significant advantage for >0.75-μm-thick EOP layers. In this calculation, we assumed that the in-device EO coefficient r_{33} (70 pm/V) was same for both the TiO_2 slot waveguide modulators and the standard modulator. In the actual modulator devices, the in-device EO coefficient for the TiO_2 slot waveguide modulator is higher than that for the standard modulator, which resulted in a lower $V_\pi L_e$ product because the poling efficiency of the EOP layer was improved by the TiO_2 and SG layers [17]. It was also difficult to pole 0.3–0.6-μm-thick EO polymers without the TiO_2 and SG layers because of dielectric breakdown at lower poling voltages of <100 V at a glass transition temperature of 150 °C. When the EO polymer was deposited on the TiO_2 and SG layers, the EOP was efficiently poled without the occurrence of the breakdown, which was a major advantage of the EOP/TiO_2 slot waveguide modulators. When t_{sg} is critically reduced to 1 μm, the $V_\pi L_e$ product calculated for the EOP/TiO_2 slot waveguide modulator is two times lower than that of the modulator (t_{sg} of 4 μm), as shown in Fig. 4.

A SG solution was prepared for the waveguide side cladding and under-cladding layers, consisting of methacryloyloxy propyltrimethoxysilane (MAPTMS) and an index modifier (zirconium (IV)-*n*-propoxide) with a molar ratio of 95(MAPTMS)/5 mol%. A 0.1-N HCl solution was used as a catalyst, and Irgacure 184 (Ciba) was used as a photoinitiator for the side cladding solutions to accelerate the hydrolysis of the silica for subsequent wet etching in isopropanol. A 4-μm-thick under-cladding layer was coated on a 100-nm-thick Au/10-nm-thick Ti lower electrode/silica (6 μm)-on-silicon substrate structure. The under-electrode was separated for dual-drive (push-pull) EO modulation. A 4-μm-thick sol–gel silica side-cladding layer was then spin-coated on the under-cladding. Mercury i-line (365 nm) radiation was delivered from a mask aligner to the sol–gel layer through a photomask to etch a 4-μm-wide core region. The regions that were exposed to radiation were then cross-linked to form a silica network. The ultraviolet-irradiated areas became insoluble in isopropanol, which was used as a wet etchant. The SG silica waveguide was hard baked at 150 °C for 1–2 h, and a 100–nm-thick TiO_2 layer was sputtered at radio frequency to form a lower slot core layer on the under-cladding between the etched SG side-cladding layers. A 0.3–0.6-μm-thick low-index EO polymer (SEO125) with 35 wt% chromophore doping in amorphous polycarbonate (APC) was then spin-coated under the TiO_2 slot layer and baked overnight at 80 °C in a vacuum oven. After the EO polymer was poled between an Au poling electrode deposited on the EO polymer and the under-electrode, the poling electrode was removed using an iodine and potassium iodine solution in deionized water. Finally, another 100-nm-thick TiO_2 slot layer was sputtered on the EO polymer, and a 1.2-μm-thick low-index perfluorinated polymer Cytop® layer was spin-coated to act as a buffer layer for consecutive deposition of an Au over-electrode.

The $V_\pi L_e$ product was experimentally measured at 1 kHz for several modulators with different EOP thickness (t_{EO}) values, ranging from 0.3 to 0.6 μm, as shown in Fig. 5. The measured $V_\pi L_e$ products were well matched with the theoretically calculated values. When the baking time for the SG silica was reduced to 0.75 h, the $V_\pi L_e$ product showed its lowest value of 2.0 V cm, and the highest in-device r_{33} value of 78 pm/V was obtained for the 0.6-μm-thick SEO125 EOP at the wavelength of 1.55 μm because of the increased conductivity of the SG silica and the reduced conductance of the EOP [11]. The $V_\pi Loss$ product was 14 V dB (propagation loss of 7 dB/cm). We measured a coupling loss of 7 dB/facet between a standard single mode fiber and the modulator without a mode convertor or a grating coupler when light through the fiber was butt-coupled into the modulator. Total optical insertion loss was 17 dB for the 14-mm-long MZ modulator, including a propagation loss of 10 dB (7 dB/cm) and a butt -coupling loss of 7 dB/facet between a standard SM fiber and the modulator when the fiber was butt-coupled into the slot waveguide modulator and an output light was focused on a power meter using a microscope lens. However, the possibility of breakdown was increased when the baking time was critically reduced. When the SG silica was baked for 2 h, the conductivity for the multiple TiO_2 slot and SG layers reduced. We obtained a similar in-device r_{33} of 70 pm/V for EOP thicknesses in the range from 0.3 to 0.5 μm, as shown in Fig. 5. When the under-cladding thickness in the hybrid modulator was reduced to <4 μm, the optical propagation loss increased to >20 dB/cm. In contrast, the EOP/TiO_2 vertical slot waveguide modulators all showed similar propagation losses (e.g., 15 dB/cm), even when t_{sg} was reduced to 1.8 μm, because the mode tail in the slot waveguide was reduced. For the modulators that have 1.8-μm-thick sol–gel silica undercladding, the $V_\pi L_e$ was more than 7 V cm because the poling efficiency for the EO polymer was not optimized. The propagation loss was varied and depended on the waveguide quality of the modulator samples. Even though some modulator samples did not have optimized poling efficiency, we obtained the lowest propagation loss of 3.5 dB/cm for the modulators that have 4-μm-thick sol–gel under cladding. The propagation loss was varied from 3.5 to 8.6 dB/cm for each waveguide in the same samples. The propagation loss was much lower than other Si slot waveguide modulators (e.g. 60 dB/cm) as shown in Table 1.

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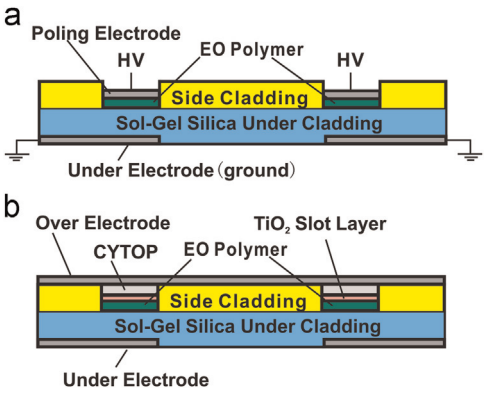

Fig. 6. Schematic cross-sectional view of the active region of the EOP/single TiO_2 slot waveguide modulator. (a) Poling setup for the modulator without TiO_2 underlayer. (b) The modulator fabricated after the poling.

2.2. Enhancement of the in-device electro-optic coefficient

We also examined the $V_\pi L_e$ product for an EOP/single TiO_2 slot waveguide modulator, in which the EOP was poled without the TiO_2 and CYTOP buffer layers, as shown in Fig. 6(a). The poling setup is same as that used for the EOP/TiO_2 vertical slot waveguide modulators, except for the removal of the TiO_2 underlayer. Therefore, we can find the difference in poling efficiency between these structures (i.e., when poled with and without the TiO_2 layer) from the measured V_π. After poling of the 0.4 μm-thick SEO125 EOP, the poling electrode was removed by a wet-etching method. Then RF-sputtered TiO_2 and CYTOP buffer layers were deposited on the EOP, and a final Au over-electrode was deposited, as shown in Fig. 6(b). This process is common for EOP/TiO_2 vertical slot waveguide modulators. The $V_\pi L_e$ product was 5.2 V cm (V_π=10.3 V for L_e=0.5 cm), and the $V_\pi Loss$ product was 41.6 V dB (propagation loss of 8 dB/cm). The in-device r_{33} was 39 pm/V at a wavelength of 1.55 μm. Because the in-device r_{33} was 70–78 pm/V when the SEO125 EOP was poled on the TiO_2 underlayer and SG silica layer in the EOP/TiO_2 vertical slot waveguide modulator, as shown in Fig. 1(a), the in-device r_{33} was therefore increased by a factor of 2.

We examined the increased poling efficiency of the high-index SEO100 EOP when coated on TiO_2 and SG silica layers using an ITO glass substrate. The poling setup is the same as that used for the EOP/TiO_2 slot waveguide modulator. Because the refractive index of SEO100 was 1.702, the refractive index of the slot layer must be increased to ensure sufficient mode confinement in the EOP/TiO_2 slot waveguide modulator and to reduce the optical losses. To date, the highest reported EO coefficients of 260 and 215 pm/V at wavelengths of 1.31 and 1.55 μm, respectively, were obtained using Teng and Man's ellipsometric method [18]. When SEO100 was poled without the TiO_2 and sol–gel silica layers, dielectric breakdown occurred frequently when the poling voltage was <10 V at the glass transition temperature of 150 °C. The EO coefficient for poled SEO100 on TiO_2 and SG silica layers was three times higher than that for SEO125. When we successfully use SEO100 in the modulator, the $V_\pi L_e$ product would be reduced by a factor of six with the reduced thickness of the SG silica and the enhanced EO coefficient, which will then result in a $V_\pi L_e$ product of less than 0.3 V cm and a $V_\pi Loss$ product of 2.3 V dB.

3. Conclusion

We have analyzed EOP/TiO_2 vertical slot waveguide modulators and have examined the poling efficiency in these modulators. The in-device EO coefficient was successfully enhanced in the devices when the EOP was poled with TiO_2 and SG layers.

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