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LETTER

Design of high-reliability LDO regulator with SCR based ESD protection circuit using body technique and load transient detection

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Abstract External capacitors in conventional LDO regulators can reduce transient response characteristics such as overshoot and undershoot. However, the capacitor-less LDO regulator proposed in this study achieves the transient response improved by applying body technique to the pass transistor, thereby provides the high areal efficiency and excellent current driving capability, and shows the improved ESD robustness characteristics. Also, the proposed ESD protection device based on due to the SCR (Silicon Control Rectifier) built into the output node and the power line. As a result, it was confirmed that the transient response characteristics of the proposed LDO regulator were improved and free space could be secured by applying the body technique of the pass transistor. The operating conditions of the proposed LDO regulator were set as an input voltage varying from 3.3 V to 4.5 V, a maximum load current of 200 mA, and the output voltage of 3 V. As a result of the measurement, when the load current was 200 mA, the voltage was found to be 23 mV in the undershoot state and 29 mV in the overshoot state. In addition, the ESD robustness characteristic of HBM is secured at 8 kV or higher.

Keywords: LDO, low drop out, ESD, SCR, capacitor-less LDO
Classification: Electron devices, circuits and modules (silicon, compound semiconductor, organic and novel materials)

1. Introduction

As the demand for battery-powered devices with high efficiency and performance increases, PMIC designers must design systems that not only consume the least amount of power, but also control the highest performance. The LDO regulator is used to provide a more stable and accurate output voltage, thereby typically requires an external capacitor. External capacitors are required for transient response and stability of the system, but are usually bulky and take up space on the PCB board and cannot guarantee long-term reliability. The absence of an external capacitor is an effective method because the PCB area can be activated and the bill of materials (BOM) cost can be reduced [1, 2, 3, 4, 5, 6, 7]. There are also disadvantages that are opposite to the advantages described above. Capacitor-less LDO regulators have an internal dominant pole that varies with the load current. The hardest part is providing reliable operation over all load current ranges. Therefore, it is essential to build an internal system for stable operation of the capacitor-less LDO regulator [8, 9, 10, 11, 12]. Capacitor-less LDO regulators, which are practical and versatile, are emerging as a key component in battery-based portable information terminals because of the space and cost savings achieved by converting the voltage required in each application into a single chip [13, 14]. As shown in Figure 1, the integration of high-efficiency power management ICs is expected to gradually intensify in order to cope with the increase of increasingly complex applications and the functions added to the terminals. In addition, since the high-efficiency power management IC is integrated into one IC, the interference or noise components may increase [15, 16, 17]. Because a lot of power is integrated in a small area, heat is generated greatly. Therefore, the development of circuit technology to increase power efficiency is required. In particular, since the design of a portable device is made within a reduced form factor, continuous efforts are required to develop a capacitor-less LDO regulator [18, 19]. In addition, as the demand for high-spec semiconductor devices increases, the latest semiconductor process technology tends to be highly integrated. It is necessary to respond to circuit technology due to the development of low-voltage applications that are vulnerable to ESD, such as smart watches and mobile device. The junction depth of these devices and the thickness of the oxide film are decreasing, thereby the design range of ESD is very narrow. As a result, the failure and destruction of ESD integrated circuits has become an increasingly serious problem. Therefore, an important parameter in IC manufacturing is maintaining high ESD immunity at reduced chip area. To solve this problem, the proposed LDO regulator has a built-in SCR-based ESD protection circuit designed by itself to counter the IC destruction caused by static [20, 21, 22, 23, 24].

2. Body effect technique

2.1 Body technique

Figures 2, 3 represent the P-MOSFET transistors shown to illustrate the body technique. In general, the pass transistor of the LDO regulator prevents control by the body terminal by shorting the body terminal and the source terminal to prevent loss due to leakage current. However, voltage is applied to the body terminals individually without shorting the body and source terminals, and the current characteristics of the ground circuit change, which is called the body effect. The proposed LDO regulator used a body effect to take better current characteristics and area efficiency to the pass transistor. The body effect refers to a change in the depletion region according to the source-body voltage.

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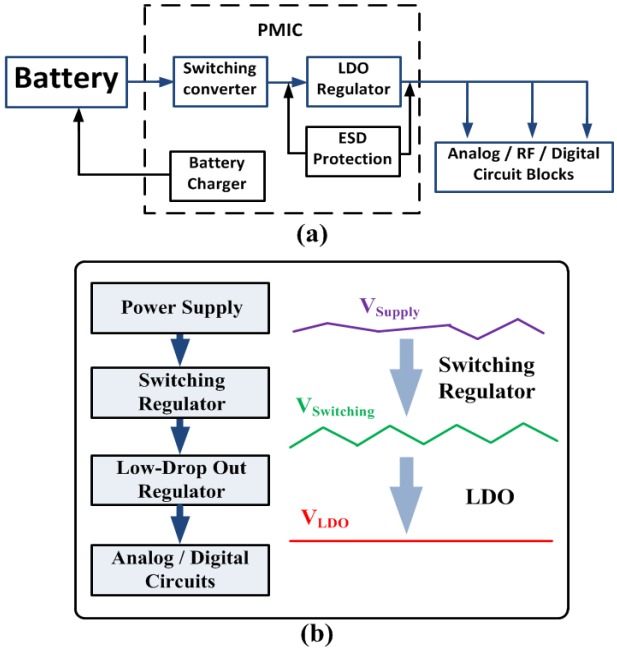

Fig. 1 Power management integrated circuit.

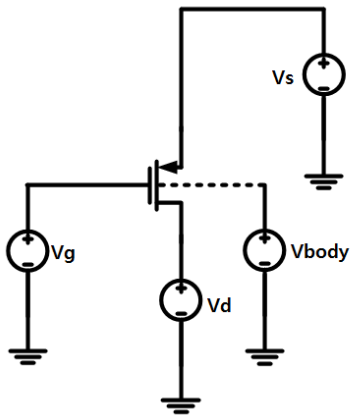

Fig. 2 Body biasing in PMOSFET.

When the source-body voltage becomes a positive voltage, a forward bias is applied between the P-WELL body and the N-WELL source, so that the depletion region is reduced. If a forward bias is applied, the effect of lowering the threshold voltage can be seen. As a result, the current amount of the P-MOSFET transistor increases.

2.2 Body technique simulation

If the body voltage is too high compared to the operation of the parasitic P-N diode, large leakage current can cause power loss and circuit failure. In this paper, in order to achieve a design that prevents the operation of parasitic diodes and provides a leakage current value insensitive to power consumption, the operation of the transistor in this study is confirmed and analyzed through the change of the forward body voltage. Figure 4 shows the value of the minimum leakage current generated by applying the body voltage of the pass transistor. The body voltage of the proposed LDO regulator was set to 2.8 V, which is a 25 nA leakage current. Based on these results, the proposed LDO regulator pass transistor has sufficient current driving capability to withstand the load current.

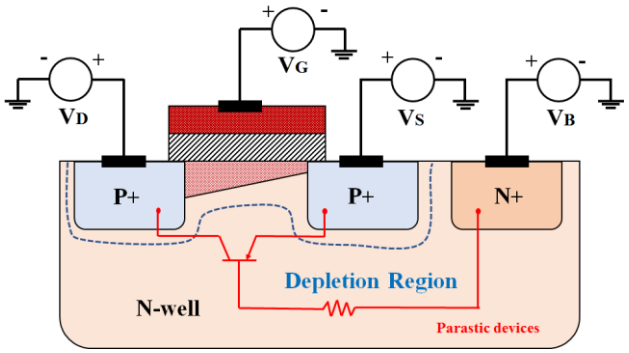

Fig. 3 Body technique cross-section in PMOSFET.

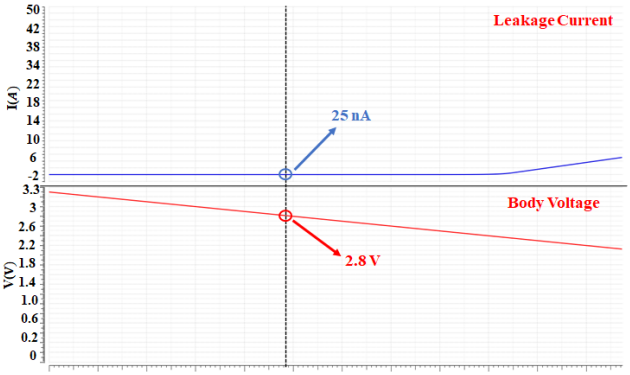

Fig. 4 Body terminal voltage biasing in proposed LDO regulator pass transistor.

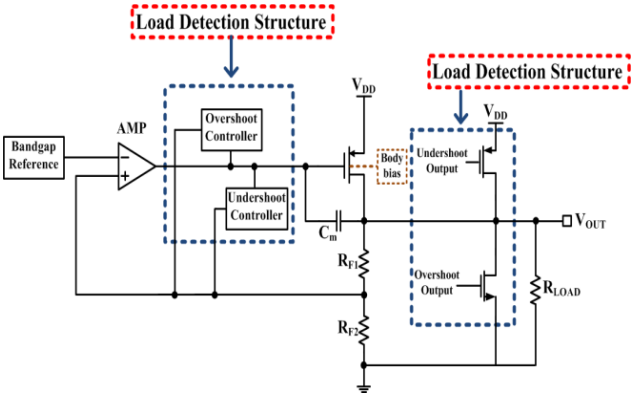

Fig. 5 Functional block diagram in proposed LDO regulator.

3. Load transient detection capacitor-less low drop out regulator

3.1 Proposed LDO regulator

Figure 5 shows a block diagram for the designed IC. The IC includes a pass transistor for driving the load current, a band gap reference for providing a reference voltage, an error amplifier for comparing the difference between the feedback voltage and the reference voltage, load transient detection structure.

Figure 6 shows the circuit used to detect and control the undershooting at the output voltage as the load current rapidly increases. If an undershooting phenomenon occurs at the output voltage, M1-M4 with the inverter structure

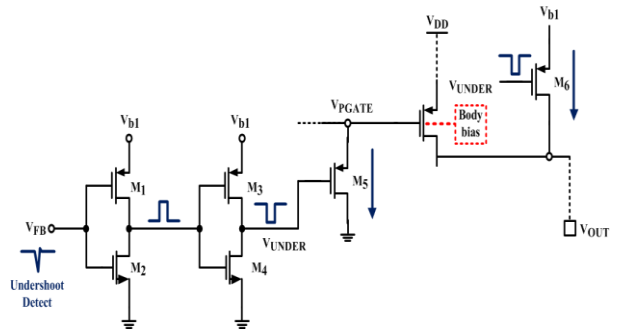

Fig. 6 Operation of the proposed LDO regulator in case of undershoot.

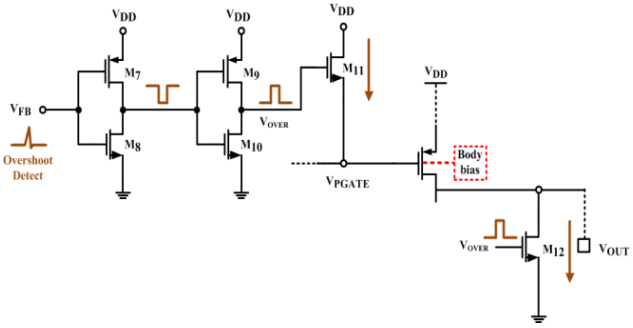

Fig. 7 Operation of the proposed LDO regulator in case of overshoot.

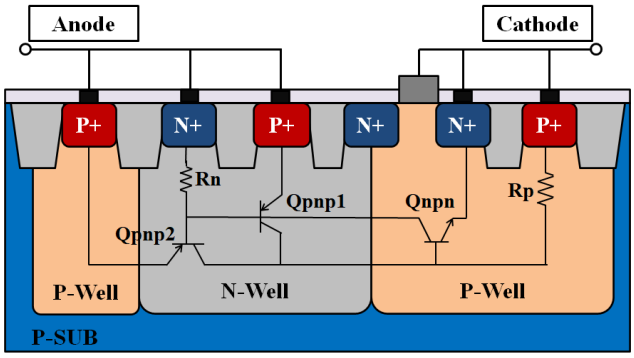

Fig. 8 LRSCR (low ron silicon controlled rectifier).

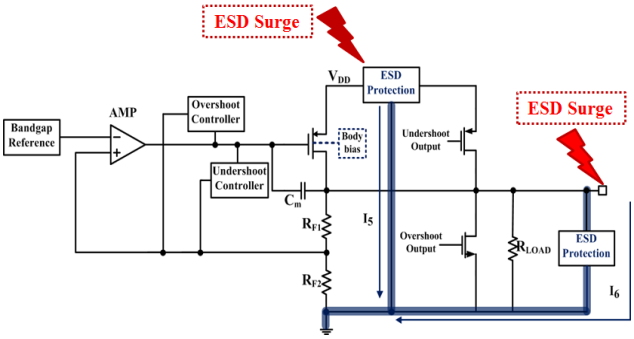

Fig. 9 The proposed LDO regulator with ESD protection.

transmits a feedback voltage to generate a VUNDER signal. According to the signal, M5 is turned on, and then the current of VPGATE, the gate node of the pass-through element, flows to the ground. If undershoot occurs for the VUNDER signal output, the voltage of Vb1 is set to have a bias voltage of 2.5 V. Since the bias voltage of Vb1 is set according to VFB. The VFB voltage becomes 1.2 V, and the MOSFET for inverters is set to PMOS 15/2 and NMOS 5/2 so that the VUNDER voltage can be detected when undershooting occurs. Therefore, it is designed to detect undershoot more efficiently. At the same time, the VUNDER signal turns on the M6, generates a current path to the output node, and provides additional current. Consequently, the gate capacitor of the pass transistor is rapidly discharged. The pass transistor temporarily increases the amount of current flowing through the load. Namely, this control method allows the dual path to operate rapidly in the event of an undershoot and reduce changes in the output voltage. Figure 7 shows the circuit used to detect and control the overshoot of the output voltage when the load current decreases sharply. When an overshoot occurs at the output voltage, M7 to M10 of the inverter structure detect the feedback voltage and generate a VOVER signal. When the overshooting occurs, the VDD voltage is set to 3.3 V. The VFB voltage becomes 1.2 V. The dimensions of MOSFETs for inverters are set to PMOS 15/2 and NMOS 30/1 so that the VOVER voltages can be detected in the event of overshooting. Therefore, it is designed to detect the overshoots more efficiently. At the same time, M12 is turned on to generate a current path to the ground. As a result, the gate capacitor of the pass transistor is charged rapidly, and the amount of current flowing through the pass transistor into the load can be temporarily reduced. This control method reduces the output voltage fluctuations by diverting the current to a double path even if overshoot occurs.

3.2 SCR-based ESD protection structure

Figure 8 shows the sectional and internal circuit diagrams of the proposed ESD protection circuit. The first structural feature of LRSCR is that GGNMOS is inserted into the SCR structure to cause avalanche breakdown at the N+/P well junction. This lowers the breakdown voltage and significantly reduces the trigger voltage. The second characteristic is to insert the P well and P+ diffusion region into the anode node and turn on the parasitic PNP BJT. Therefore, when ESD current flows, additional PNP BJTs provide parallel discharge paths to reduce on-line resistance and improve durability. LRSCR operates according to the following principles: As ESD current flows through the anode node it is accompanied by avalanche breakdown, which produces electron-hole pairs at the N + bridge region/P-well junction. At this time, the generated hole moves to the cathode via the P well. Consequently, the potential voltage rises. When the potential voltage of the P-well is higher than the potential voltage of the internal electric field from the P-well/N+ junction, the two junctions is forward biased and the parasitic NPN BJT is switched on. In addition, the generated electron current flows to the anode through N-well like a hole, causing forward bias in the P+/N-well junction and turning on parasitic PNP BJT1 and 2. The BJT then forms a positive feedback loop and discharges a large amount of ESD current. Figure 9 shows the LDO regulator block combined with the proposed ESD clamp. Considering the safe discharge of surges when the proposed LDO regulator operating voltage is introduced, ESD clamps with parameters optimized for 3.3 V ESD design window are coupled between VDD and VSS, VOUT and VSS. Surges

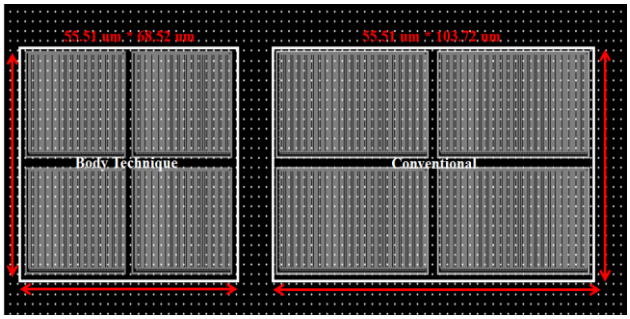

Fig. 10 Comparison of layout (proposed vs. conventional).

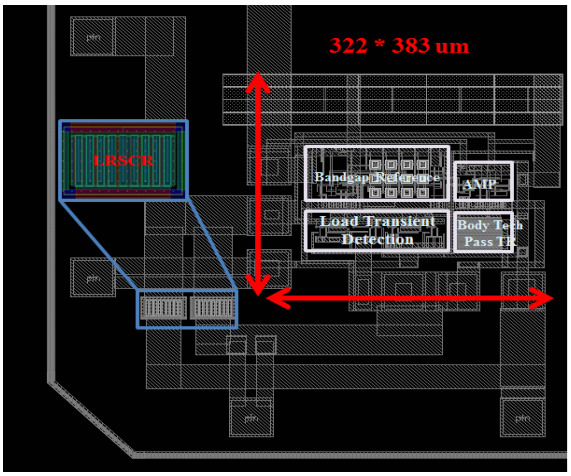

Fig. 11 The proposed LDO regulator layout.

flowing through VDD and VOUT pins can be safely discharged to GND pins through ESD clamps before the gate oxide and transistor connections are broken, thus ensuring normal operation of the LDO regulator can be ensured in ESD conditions [25, 26, 27, 28, 29, 30, 31].

4. Measurement results

Figures 10, 11 illustrate the layout of the proposed LDO regulator. The pass transistor of the proposed LDO regulator secured 33.9% area efficiency compared to the existing LDO regulator. It has the same current driving ability and has efficiency for the area. The size of the proposed LDO regulator is 322 * 383 um. ESD protection structure was applied to the VDD-VSS and VOUT-VSS nodes. Load transient response is the response characteristic of the output voltage waveform to abrupt load changes at the output node. Figure 12 shows the results of the proposed LDO. It was confirmed that the proposed LDO regulator showed a change of 23 mV under the undershoot condition and 29 mV under the overshoot condition. These results confirm that the LDO regulator using the load transient sensing scheme shows improved performance. In addition, it was confirmed that the proposed LDO regulator using the body effect on the pass transistor improves the current driving ability.

Figure 13 shows the measurement results of line regulation. As the input voltage of the LDO regulator constantly changes, the change in the output voltage can be determined. It was confirmed that the output voltage of the proposed LDO

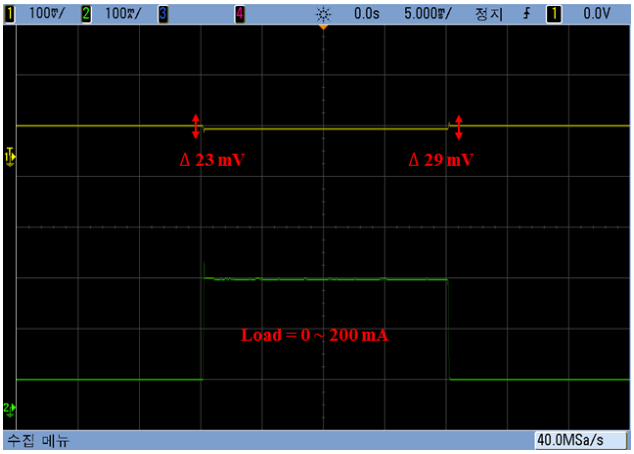

Fig. 12 Load transient of the proposed LDO regulator.

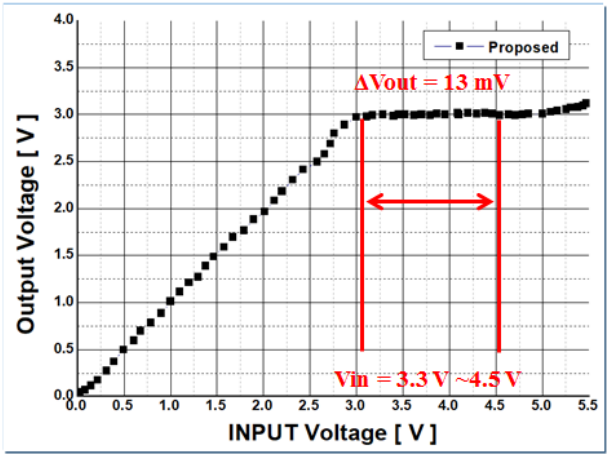

Fig. 13 Line regulation of the proposed LDO regulator.

regulator changed by about 13 mV in the 3.3 V~4.5 V range of the input voltage.

Figure 14 shows the results of the load regulation measurement. The change in output voltage is determined by the continuous increase in the load on the output cluster of the LDO regulator. It has been confirmed that the output voltage of the proposed LDO regulator varies by 16 mV in the load current range from 100 uA to 200 mA. Figure 15 shows the chip level TLP (Transmission Line Pulse) I–V curve of the proposed ESD protection circuit. It was confirmed that the holding voltage of LRSCR was 6.1 V while the trigger voltage was 8.4 V, which was higher than the proposed LDO supply voltage and lower than the gate oxide breakdown voltage. It was also confirmed that it had a low on-resistance of 1.19 ohm and a current driving capability of 6.5 A due to the parallel discharge path.

5. Conclusion

In order to alleviate overshoot and undershoot phenomena of existing devices, LDO regulators with load transient detection structures and body technique have been proposed. Therefore, the proposed LDO regulator proposed in this study was designed to have improved transient response characteristics by forming a new control load transient detection structure- in addition to the feedback path of the conven-

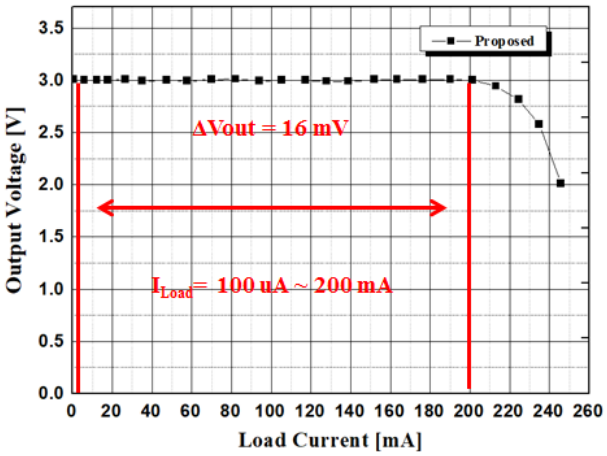

Fig. 14 Load regulation of the proposed LDO regulator.

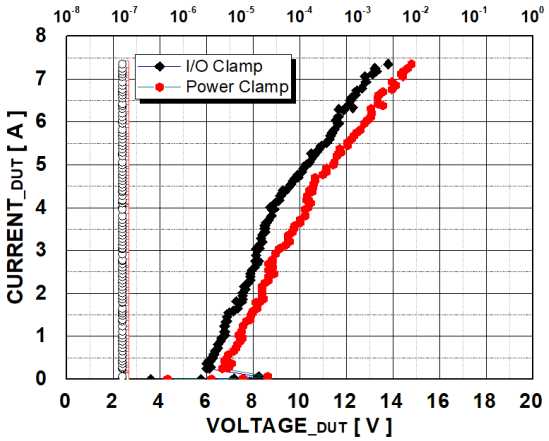

Fig. 15 TLP I-V curve of ESD clamp.

tional LDO. The operating speed of the pass transistor is improved by charging and discharging current to the pass transistor's gate node. As a result, in the undershoot condition, a voltage of 23 mV was confirmed depending on the load, and in the overshoot condition, a voltage of 29 mV was confirmed. Therefore, it was confirmed that the load transient detection structure, which is a new control path to which the body technique is applied, can effectively control the output voltage. As a result, the proposed LDO regulator pass transistor applies body technique, has excellent current driving capability, and secures an area efficiency of 33.9% compared to the conventional LDO regulator. In addition, since the LDO regulator, which is inevitably an IC circuit, has the problem of electrostatic destruction, the proposed LDO regulator in this study is applied with an SCR (Silicon Controlled Rectifier)-based ESD protection circuit to ensure a high reliability characteristic of HBM 8 kV and MM 800 V or higher.

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References

[1] S.K. Lau, *et al.*: "A low-dropout regulator for SoC with Q-reduction," IEEE J. Solid-State Circuits **42** (2007) 658 (DOI: 10.1109/JSSC.2006.891496).
[2] M. Al-Shyoukh, *et al.*: "A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation," IEEE J. Solid-State Circuits **42** (2007) 1732 (DOI: 10.1109/JSSC.2007.900281).
[3] Y.-S. Koo: "A design of low-area low drop-out regulator using body bias technique," IEICE Electron. Express **10** (2013) 0300 (DOI: 10.1587/elex.10.20130300).
[4] J. Moon, *et al.*: "Design of low-power, fast-transient-response, capacitor-less low-dropout regulator for mobile applications," IEICE Electron. Express **13** (2016) 0882 (DOI: 10.1587/elex.13.20160882).
[5] A. Maity and A. Patra: "Tradeoffs aware design procedure for an adaptively biased capacitorless low dropout regulator using nested miller compensation," IEEE Trans. Power Electron. **31** (2016) 369 (DOI: 10.1109/TPEL.2015.2398868).
[6] M. Fujishima and P.K.T. Mok: "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," IEEE J. Solid-State Circuits **38** (2003) 1691 (DOI: 10.1109/JSSC.2003.817256).
[7] F. Lavalle-Aviles, *et al.*: "A high power supply rejection and fast settling time capacitor-less LDO," IEEE Trans. Power Electron. **34** (2019) 474 (DOI: 10.1109/TPEL.2018.2826922).
[8] S.S. Chong, *et al.*: "A sub-1 V transient-enhanced output-capacitorless LDO regulator with push–pull composite power transistor," IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **22** (2014) 229 (DOI: 10.1109/TVLSI.2013.2290702).
[9] N. Liu and D. Chen: "A transient-enhanced output-capacitorless LDO with fast local loop and overshoot detection," IEEE Trans. Circuits Syst. I, Reg. Papers **67** (2020) 3422 (DOI: 10.1109/TCSI.2020.2991747).
[10] J. Tang, *et al.*: "Low-power fast-transient capacitor-less LDO regulator with high slew-rate class-AB amplifier," IEEE Trans. Circuits Syst. II, Exp. Briefs **66** (2018) 462 (DOI: 10.1109/TCSII.2018.2865254).
[11] J.-H. Jung, *et al.*: "A fast transient response hybrid LDO with highly accurate DC voltage using countable bidirectional binary search and soft swap switching," IEEE Trans. Circuits Syst. II, Exp. Briefs **67** (2020) 3272 doi[10.1109/TCSII.2020.2992056]10.1109/TCSII.2020.2992056.
[12] X. Ma, *et al.*: "A fully integrated LDO with 50-mV dropout for power efficiency optimization," IEEE Trans. Circuits Syst. II, Exp. Briefs **67** (2020) 725 (DOI: 10.1109/TCSII.2019.2919665).
[13] A. Nakhlestan, *et al.*: "Low-power area-efficient LDO with loop-gain and bandwidth enhancement using non-dominant pole movement technique for IoT applications," IEEE Trans. Circuits Syst. II, Exp. Briefs **68** (2021) 692 (DOI: 10.1109/TCSII.2020.3013646).
[14] W.-C. Chen, *et al.*: "A switchable digital–analog low-dropout regulator for analog dynamic voltage scaling technique," IEEE J. Solid-State Circuits **49** (2014) 740 (DOI: 10.1109/JSSC.2013.2297395).
[15] R.J. Milliken, *et al.*: "Full on-chip CMOS low-dropout voltage regulator," IEEE Trans. Circuits Syst. I, Reg. Papers **54** (2007) 1879 (DOI: 10.1109/TCSI.2007.902615).
[16] Y. Lu, *et al.*: "A fully-integrated low-dropout regulator with full-spectrum power supply rejection," IEEE Trans. Circuits Syst. I, Reg. Papers **62** (2015) 707 (DOI: 10.1109/TCSI.2014.2380644).
[17] E.N.Y. Ho and P.K.T. Mok: "A capacitor-less CMOS active feedback low-dropout regulator with slew-rate enhancement for portable on-chip application," IEEE Trans. Circuits Sys. II, Exp. Briefs **57** (2010) 80 (DOI: 10.1109/TCSII.2009.2038630).
[18] Q.-H. Duong, *et al.*: "Multiple-loop design technique for high-performance low-dropout regulator," IEEE J. Solid-State Circuits **52** (2017) 2533 (DOI: 10.1109/JSSC.2017.2717922).
[19] K. Keikhosravy and S. Mirabbasi: "A 0.13-μm CMOS low-power

capacitor-less LDO regulator using bulk-modulation technique," IEEE Trans. Circuits Syst. I, Reg. Papers **61** (2014) 3105 (DOI: 10.1109/TCSI.2014.2334831).
[20] K.-I. Do, *et al.*: "4H-SiC-based ESD protection design with optimization of segmented LIGBT for high-voltage applications," IEEE J. Electron Devices Soc. **9** (2021) 1017 (DOI: 10.1109/JEDS.2021.3121212).
[21] K.-I. Do, *et al.*: "A 4H-SiC MOSFET-based ESD protection with improved snapback characteristics for high-voltage applications," IEEE Trans. Power Electron. **36** (2021) 4921 (DOI: 10.1109/TPEL.2020.3032917).
[22] K.-I. Do, *et al.*: "A novel dual-directional SCR structure with high holding voltage for 12-V applications in 0.13-μm BCD process," IEEE Trans. Electron Devices **67** (2020) 5020 (DOI: 10.1109/TED.2020.3023064).
[23] K.-I. Do, *et al.*: "Design of 4H-SiC-based silicon-controlled rectifier with high holding voltage using segment topology for high-voltage ESD protection," IEEE Electron Device Lett. **41** (2020) 1669 (DOI: 10.1109/LED.2020.3022888).
[24] K.-I. Do, *et al.*: "A gate-grounded NMOS-based dual-directional ESD protection with high holding voltage for 12 V application," IEEE Trans. Device Mater. Reliab. **20** (2020) 716 (DOI: 10.1109/TDMR.2020.3022897).
[25] K.-I. Do, *et al.*: "A novel low dynamic resistance dual-directional SCR with high holding voltage for 12 V applications," IEEE J. Electron Devices Soc. **8** (2020) 635 (DOI: 10.1109/JEDS.2020.2999108).
[26] K.-I. Do, *et al.*: "A new SCR structure with high holding voltage and low on-resistance for 5-V applications," IEEE Trans. Electron Devices **67** (2020) 1052 (DOI: 10.1109/TED.2020.2963994).
[27] K.-I. Do, *et al.*: "A new dual-direction SCR with high holding voltage and low dynamic resistance for 5 V application," IEEE J. Electron Devices Soc. **7** (2019) 601 (DOI: 10.1109/JEDS.2019.2916399).
[28] K.-I. Do, *et al.*: "Study on 4H-SiC GGNMOS based ESD protection circuit with low trigger voltage using gate-body floating technique for 70-V applications," IEEE Electron Device Lett. **40** (2019) 283 (DOI: 10.1109/LED.2018.2885846).
[29] B.-B. Song, *et al.*: "SCR-based ESD protection using a penta-well for 5 V applications," IEEE J. Electron Devices Soc. **6** (2018) 691 (DOI: 10.1109/JEDS.2018.2817636).
[30] K.-I. Do, *et al.*: "A novel dual-directional SCR structure with high holding voltage for 12-V applications in 0.13-μm BCD process," IEEE Trans. Electron Devices **67** (2021) 5020 (DOI: 10.1109/TED.2021.3073182).
[31] Y.-C. Huang and M.-D. Ker: "A latchup-immune and robust SCR device for ESD protection in 0.25-μm 5-V CMOS process," IEEE Electron Device Lett. **34** (2013) 674 (DOI: 10.1109/LED.2013.2252456).