LETTER

A radiation-hardened 14T SRAM cell for highly reliable space application

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Abstract A 14T SRAM bit-cell, implemented in 130-nm CMOS technology, with excellent read stability and soft error tolerance performance has been proposed. The parasitic extracted simulations show that compared with considered memory cells, the proposed cell achieves up to 146% read access time saving at the cost of acceptable layout area and leakage power dissipation overhead. The RSNM of 14T bit-cell is about x2.6 that of DICE structure, revealing excellent read stability. In addition, the proposed cell provides larger the critical charge, which indicates more superior soft error resilience ability.
Keywords: SRAM cell, single event upset, high read stability, critical charge
Classification: Circuits and modules for storage

1. Introduction

Devices dimensions are increasingly descending as the technology node scaling, which renders static random access memories (SRAMs) extensively applied in aerospace are more sensitive to single event upsets (SEUs) induced by radiation particles [1, 2, 3, 4, 5, 6, 7]. SEUs caused by a reversed-bias p-n junction collecting excessive charge on which energetic particles striking give rise to data upset, namely, destroy the data integrity and then conduce to function failure of logic elements, such as latch [8, 9, 10, 11, 12, 13], DFF, SRAM bit-cell. Among these digital modules, we focus on the memory cell occupying a large portion of total memories area. In recent years, various methods have been proposed to harden SRAM cells, including chiefly three categories: 1) layout level; 2) circuit level design; 3) system level design. On the one hand, the application of layout design techniques is restricted by complicated layout design rules. On the other hand, radiation hardening techniques by system level design such as error correction codes (ECC) [14, 15, 16, 17, 18, 19] tend to bring about non-negligible area and delay overheads.

In terms of radiation hardening of circuit level design, the majority of effective solutions are to create redundant logic structures to shelter stored data, of which one commonly investigated is to increase extra transistors. In past several decades, lots of SRAM cells aiming to mitigate SEU have been reported, such as 10T-StackN, 10T-StackP [20], 10T-Quatro [21], 12T-QUCCE [22] and 12T-DICE [23]. However, 10T-StackN and 10T-StackP can only tolerate $1 \rightarrow 0$

SEU and $0 \rightarrow 1$ SEU respectively. Similarly, only a $1 \rightarrow 0$ SEU can be mitigated by 10T-Quatro. 12T-QUCCE and 12T-DICE can fully recover two types SEU by approximately feedback structure, whereas they suffer from weak read static noise margin and develop diverse soft error resilience ability.

In this paper, a new radiation-hardened and highly reliable SRAM cell named as HRSC has been proposed. More superior performance has been acquired by the separation of write and read operation compared with these cells mentioned above. Eventually, the proposed cell consists of 14 transistors.

The rest of this paper is primarily arranged as follows. Section 2 presents the structure, operation process, SEU tolerance analysis of the proposed 14T HRSC. Post-layout netlist simulations results including validating the effectiveness of alleviating SEU, related stability comparisons in several supply voltage regions, cost comparisons and soft error resilience performance in terms of these cells mentioned above are shown in Section 3. Finally, Section 4 concludes this paper.

2. Proposed 14T HRSC

2.1 Schematic and read/write operation

The schematic of the proposed cell is shown in Fig. 1, which has four storage nodes (Q1, Q2, QN1, QN2). The nodes Q2 and QN2 are the redundant nodes of nodes Q1 and QN1 with opposite logic states. The circuit includes a four-inter-locked-branches structure identical with DICE and two NMOS transistors N9 and N10 controlled by node QN1 and RWL respectively.

In the following function analysis, we assume the proposed cell stores '0' state, namely, the logic states of nodes Q1, Q2, QN1 and QN2 are '0', '0', '1' and '1' respectively.

When both WWL and RWL are deactivated, the pass
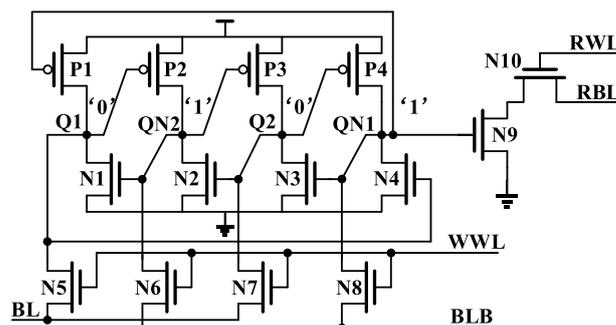
Fig. 1 The schematic of proposed 14T HRSC.

gates N5-N8 are turned off. Therefore, the four nodes are isolated from BL/BLB and RBL, thus their original states are maintained.

For write '1' operation, as depicted in Fig. 1, BL and BLB are set to be '1' and '0' respectively. When WWL is activated, the data of BL and BLB is fed to four nodes by four access transistors. In this case, even though the BL voltage produces a threshold voltage loss after transported by transistors N5 and N7, both nodes Q1 and Q2 are still able to build up a right '1' state rapidly thanks to nodes QN1 and QN2 turning on the pull-up transistors P1 and P3 respectively.

Instead of reusing WWL and BL/BLB for write and read operation, we separate write and read operation by introducing transistors N9 and N10. In order to read '0' state successfully, on the one hand, WWL is set to '0' to make four nodes immune to the states of BL and BLB. On the other hand, RBL is pre-charged to supply voltage initially, RWL is enabled subsequently to switch on transistor N10. Different from discharging BL or BLB to amplify the voltage difference between them for a traditional DICE cell, RBL of the proposed cell begins to be discharged by additional transistors N9 and N10, of which the voltage drop will be amplified by a single-end sense amplifier. Eventually, the logic '0' state will be output accurately.

2.2 Error tolerance analysis

Supposing the proposed cell state is shown as in Fig. 1, i.e., Q1 = '0', QN1 = '1', Q2 = '0' and QN2 = '1' respectively, the SEU tolerance analyses and soft error recovery mechanism of four nodes are given as follows.

When suffering from an SEU, node Q1 will be charged to state 1. As a result, transistors N4 and P2 will be turned on and off respectively, then node QN1 will be pulled down to '0' state resulting in transistors P1 and N3 being turned on and switched off respectively. In this case, both nodes QN2 and Q2 are utterly immune to the impact of the SEU. Hence nodes Q and QN1 will recover to right logic state and keep steady with the persistent help of storage nodes QN2 and Q2 maintaining correct state. Similar SEU recovery analyses are suitable for node Q1 on account of the symmetry of the proposed cell storage structure.

If node QN2 is discharged to 0 by a radiation particle, transistors P3 and N1 will be turned on and off respectively. Therefore, node Q2 will be pulled up to '1' state, which switched transistors P4 and N2 off and on respectively. Under such circumstance, nodes Q1 and QN1 will maintain their original states constantly, thereby nodes Q2 and QN2 will recover to their original states. Analyses are similar to that of node QN1.

The layout of the 14T HRSC has been given in Fig. 2 based on 130-nm CMOS technology and implemented in Cadence Virtuoso. In addition, all simulations in this paper are obtained in HSPICE and performed with utilizing post-layout netlist extracted by Calibre PEX. As demonstrated in Fig. 3, write and read function of the proposed cell have been achieved successfully with setting related conditions mentioned above.
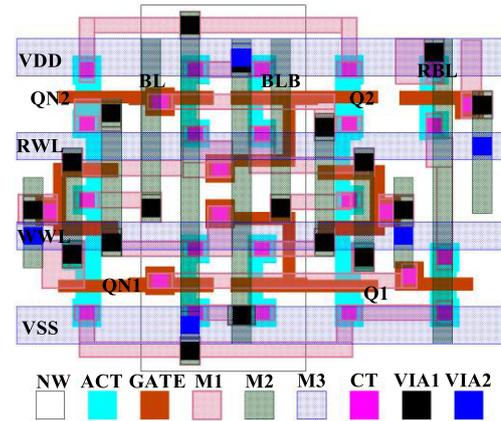

Fig. 2   Layout of the proposed HRSC.
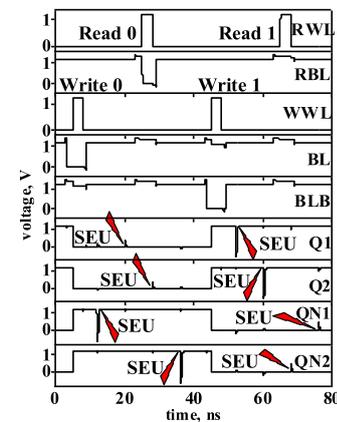
Fig. 3   Transient post-simulations of functional operations and SEU tolerance.

3. Evaluation

3.1 SEU tolerance verification

The reverse-biased p-n junction is the sensitive region of solid circuits when a radiation particle striking a transistor. Accordingly, a positive and a negative transient pulse are generated for a PMOS transistor and a NMOS transistor respectively.

An exponential current source is exerted to approximately represent the transient pulse model and verify the soft error in simulations. The rise and decay time constant of applied current pulse given in [24] were set to be 50 ps and 164 ps, respectively.

It should be noted that both a positive pulse and a negative pulse are likely to be induced for the four nodes of proposed cell. In consequence, each node has been simulated for $0 \rightarrow 1$ and $1 \rightarrow 0$ upset situations in Fig. 3, from which we can observe that four nodes can recover to their original states in typical PVT condition (supply voltage equals to 1.2 V, typical process corner and temperature is 25°C) when suffering from a positive or negative transient pulse (four upset cases for each state, eight upset cases totally).

3.2 Cost comparison

Firstly, the layout areas and leakage power dissipation of diverse memory cells are compared. It is worth noting that

Table I Cost comparisons in typical PVT condition.

	Area (um^2)	AS	Power (nW)	PS
6T	6.9342	-58.12%	12.55	-46.91%
10T_StackN	12.8118	-22.62%	11.86	-49.83%
10T_StackP	12.5849	-23.99%	18.55	-21.53%
10T_Quatro	13.4386	-18.83%	18.45	-21.95%
12T_QUCCE	16.5400	-0.10%	24.77	4.78%
12T_DICE	13.7376	-17.03%	24.93	5.46%
Proposed	16.5564	-	23.64	-

Table II Access time comparisons in typical PVT condition.

	TR (ps)	RS	TW (ps)	WS
6T	95.58	104.01%	35.22	-16.99%
10T_StackN	115.55	146.64%	40.24	-5.16%
10T_StackP	97.60	108.32%	41.40	-2.43%
10T_Quatro	97.67	108.47%	48.87	15.18%
12T_QUCCE	54.92	17.23%	37.21	-12.30%
12T_DICE	51.83	10.63%	41.62	-1.91%
Proposed	46.85	-	42.43	-

these memory cells layout are drawn without violating any design rules. As shown in Table I, layout topology area of the proposed cell costs extra 58.12%, 22.62%, 23.99%, 18.83%, 0.10%, 17.03% of 6T, 10T-StackN, 10T-StackP, 10T-Quatro, 12T-QUCCE, 12T-DICE respectively as a result of the maximum number transistors. Nevertheless, 10T-StackN and 10T-StackP cannot fully tolerate SEU as stated above.

With respect to leakage power dissipation of hold mode, the proposed cell saves 4.78% and 5.46% of 12T-QUCCE and 12T- DICE respectively, but consumes additional 46.91%, 49.83%, 21.53%, 21.95% of 6T, 10T-StackN, 10T-StackP, 10T-Quatro respectively correlated with the transistor counts of cells. Here, AS, PS, RS and WS stand for savings of area, power dissipation, read access time and write access time respectively.

Read and write access time comparisons results of these memory cells have been listed in Table II. HRSC has the smallest read access time by reason of the employment of single-end read structure. When reading 0 state, the parasitic capacitance of RBL has been availably decreased by separating write and read operation, i.e., reducing the load capacitance of pull-down path of write operation by adopting a single RBL instead of a pair of BLs. Nonetheless, single-end structure introduces slight augment of parasitic capacitance of node QN1 resulting in larger write access time. In addition, 10T-Quatro experiences poor write stability [25] resulting in the worst write ability.

3.3 Comparison of static noise margin
Static noise margins (SNM) are universally utilized as evaluating criterion of SRAM cells reliability [26, 27], which can be concretely divided into Read SNM (RSNM), Write SNM (WSNM), Hold SNM (HSNM).

Fig. 4 gives comparisons of RSNM, WSNM and HSNM of diverse memory cells in typical PVT condition. It can be seen that the RSNM of 14T HRSC has been enlarged more than two times by isolating storage node from the BLs as mentioned above in comparison to DICE cell, which means HRSC has excellent read stability.

The WSNM of 12T-QUCCE, 12T-DICE and HRSC are close because of the same write mechanisms that transporting BLs data to all storage nodes, which renders nearly identical write ability. Besides, when entering in write mode,
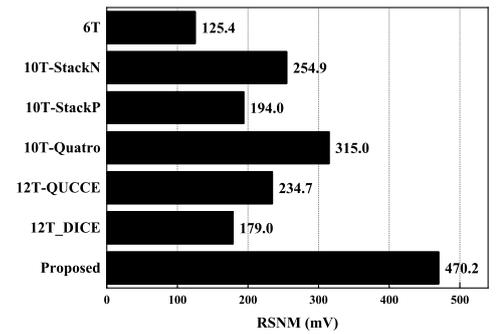
(a)
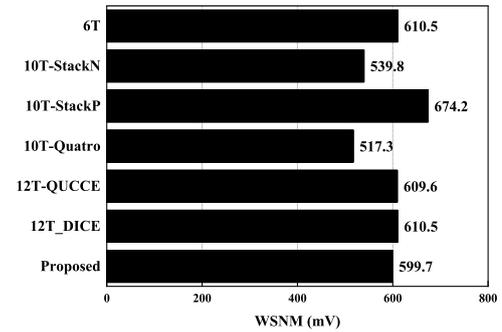
(b)
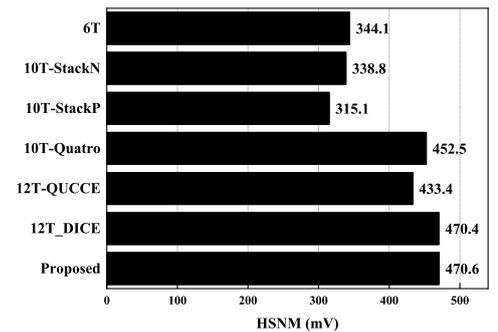
(c)

Fig. 4 SNM comparisons in typical PVT condition. (a) RSNM. (b) WSNM. (c) HSNM.

10T-StackP instantly establishing nodes states by powerful pull-down of NMOS drive transistors. However, contrary to 10T-StackP, 10T-StackN takes advantages of weak PMOS pull-up transistors to build up logic state. As a result, 10T-StackN and 10T-StackP exhibit a lower and highest WSNM respectively as displayed in Fig. 4(b).

In Fig. 4(c), composed of similar feedback structures, 10T-Quatro, 12T-QUCCE, 12T-DICE and HRSC have approximately equivalent HSNM. On the other hand, owing to asymmetric feedback loop of four nodes of 10T-StackP and 10T-StackN, they suffer lowest HSNM.

Fig. 5 shows comparisons of RSNM and HSNM of considered cells in several supply voltages. In lower supply voltage regions, HRSC keeps rather excellent read stability with the biggest RSNM and HSNM and comparable WSNM, which reveals the proposed cell has synthetically splendid operation performance.

(a)

(b)
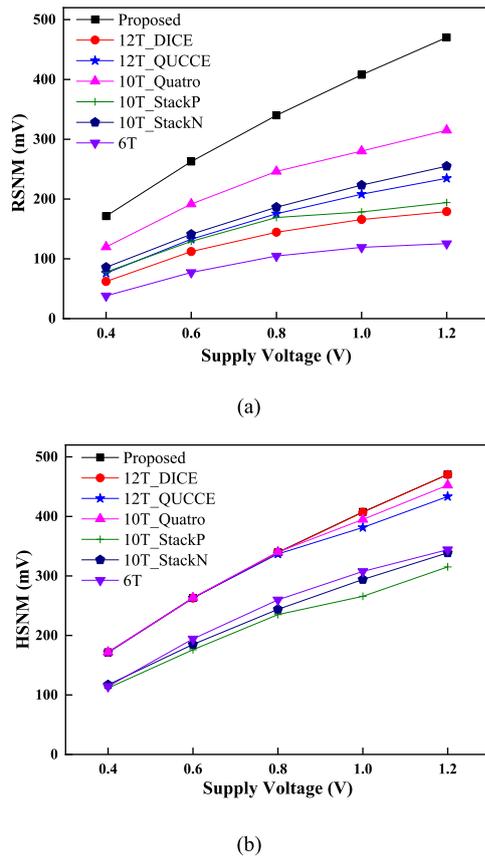
Fig. 5 SNM comparisons in low supply voltage. (a) RSNM. (b) HSNM.

Table III Critical charge in typical PVT condition.

	$Q_{critical}$
6T	3.88fC
10T_StackN	4.10fC
10T_StackP	5.59fC
10T_Quatro	15.96fC
12T_QUCCE	15.96fC
12T_DICE	63.84fC
Proposed	66.12fC

3.4 Critical charge comparison

The charge collected by the inverse-biased p-n junction is larger than critical charge when a particle strikes a storage node, which will lead to a data state upset [28, 29, 30].

As shown in Table III, we compare the magnitude of critical charge of diverse cells in typical PVT condition to evaluate the SEU tolerance. Here, $Q_{critical}$ stands for the minimum critical charge which can upset any one node of all storage nodes of memory cells. 6T has the smallest $Q_{critical}$ for lack of the protection of redundant storage nodes. 10T_StackN and 10T_StackP have comparable $Q_{critical}$ due to inadequate soft error tolerance. $Q_{critical}$ of the proposed cell is about 17x, 16x, 11.8x, 4x and 4x that of 6T, 10T-StackN, 10T-StackP, 10T-Quatro and 12T_QUCCE respectively. In the other hand, compared with 12T_DICE, the improvement of node capacitance of the proposed cell realized by introducing the gate capacitance of N9 leads to the larger $Q_{critical}$. Consequently, HRSC shows the best performance in soft error tolerance under radiation environment.

4. Conclusion

To avoid storage node being disturbed by BLs states directly, we propose a novel 14T SRAM bit-cell, implemented in 130-nm CMOS technology, with effectively enhanced read stability and optimized read speed in this paper. Compared with other SEU-tolerant SRAM cells, post-layout netlist simulations show that the proposed bit-cell has the smallest read access time and comparable write access time in typical PVT condition at the cost of acceptable layout area overhead. With respect to stability, simulations indicate that RSNM of the proposed bit-cell has been significantly improved more than two times compared with DICE cell. Furthermore, WSNM and HSNM of the proposed cell are comparable with other cells. The similar variation tendencies are validated in lower supply voltages. Moreover, compared to DICE cell, the proposed cell has enhanced the critical charge value, which demonstrates it superior in soft error tolerance. Consequently, the proposed memory cell is superior in comprehensive performance in terms of considered memory cells, thus one can be a hopeful candidate of SRAM cells for aerospace application.

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