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LETTER

# A 12.5 Gbps clock and data recovery circuit with phase interpolation based digital locked loop

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**Abstract** This paper presents a high speed dual channel 12.5 Gbps receiver for serial link communication. Each channel consists of a continuous time linear equalizer (CTLE), a novel 12.5 Gbps dual loop clock and data recovery (CDR) circuit based on phase interpolation with only simple CML and CMOS logic, which makes the design simplicity and more tolerant to process, voltage and temperature variations. A single PLL shared by the two channel CDRs generates quadrature clock phases and distributes high frequency clock to each CDR for data recovery. The 12.5 Gbps two channel receiver prototype was designed in 65-nm CMOS technology with phase interpolation based digital locked loop, occupying an active area of 1.3 mm$^2$ and consuming a power of 300 mW from a 1.2 V power source.

**Keywords:** Serdes, clock data recovery, BER, BBPD, phase interpolator, random work filter

**Classification:** Integrated circuits (memory, logic, analog, RF, sensor)

## 1. Introduction

As the dramatically increasing in information communication data rate between chips with I/O pin count limitation in chip packages and backplane wiring constraints, high-speed serial link technology is widely employed for high-throughput inter-chip communication [1, 2, 3, 4]. Due to the wide data bandwidth requirement for state of art wire-linked communication systems growing rapidly, the frequency-dependent loss and impedance discontinuities in the electrical channel have become the limitation for high-speed serial transceivers. The clock and data recovery (CDR) circuit, critical building block of high speed serial links, is utilised to recover clock and data information from serial data stream in the noisy channel and re-time data signal to the optimal sampling position under low bit error rate (BER) [5, 6, 7, 8, 9, 10, 11]. The conventional phase-locked loop (PLL) based CDR uses a voltage controlled oscillator (VCO) to generate a quadrature clock phase at the data rate of received data sequence, providing a tunable bit rate and convenience of easily integrated for multi-channel serial link application with single frequency tracking loop for reference clock generation avoiding the need for PLLs at each pin reducing the area occupation and power consumption significantly [12, 13, 14, 15, 16, 17].

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The dual-loop phase interpolator (PI) based CDR topology offers the benefits of increased system stability, simple structure, low power, faster acquisition and a lock of jitter peaking compared with a PLL-based CDR that needs a charge pump, an analog filter and VCO to align phase to optimize sampling point [1]. At the same time, PI-based CDR can operate over a wide range of data rates with certain allowable frequency offset between transmitter and receiver in a source-asynchronous scenario.

In this paper, we present a 12.5 Gbps dual channel PI-based digital locked loop CDR circuit targeting for high-speed serial communication by utilizing a standard commercial 65-nm CMOS technology with low complicated CML and CMOS logics [13, 18, 19, 20].

## 2. The proposed dual-loop CDR architecture

Fig. 1 shows the proposed architecture of 12.5 Gbps receiver with dual-loop two channel CDRs sharing a PLL as the clock generation source [5, 21]. Each CDR loop is made up of six parts which are a phase interpolator (PI), a binary phase detector (BPD), a random work filter (RWF), an adder, a control logic to complete phase alignment between clock and data, and a deserializer circuit to convert serial data into 40-bits parallel data. In the BPD module, clock CKI and CKQ are used for data sampling. if the clock phase is leading the data, the DN signal will be generated. if the clock phase is lagging the data, the UP signal will be generated. Then, the UP and DN signal generated by the BPD module input into the RWF module. RWF acts as a filter to ensure the single appearance of UP/DN signals, and both UP and DN signals will not appear at the same time which can re-

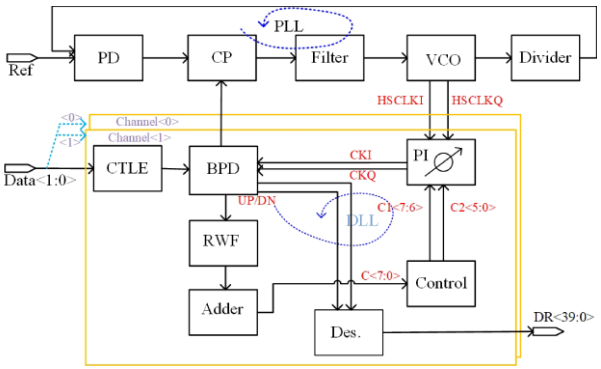


**Fig. 1** The proposed two channel clock and data recovery structure with a PLL as common clock source.

duce the clock jitter. The UP/DN signal after passing RWF enters the accumulator. For every UP signal the accumulator accumulates one, while for every DN signal the accumulator subtracts one. When the phase difference between the clock and the data is 360 degrees, the accumulator results in C[7:0] equals FF in hex. The controller and PI convert the corresponding code into different weights and synthesize HSCKI and HSCKQ into the correctly aligned clock CKI and CKQ. Finally, the deserializer uses the alignment clock to sample data correctly from serial stream.

As an alternative, the UP/DN of channel 0 was introduced into the charge pump (CP) of the PLL loop. This option can be opened if the incoming data stream has frequency drift.

## 3. The phase detector

The proposed receiver uses the Inverse Half-Alexander Bang-Bang phase detector using three consecutive clock edges to decide if the clock is leading or lagging the data, which is widely applied in high-speed clock and data recovery systems for it's simplicity and excellent phase adjustment [1, 7, 22, 23, 24, 25]. The principle of binary detector is shown in the Fig. 2 [26, 27, 28, 29]. As shown in the Fig. 2(a), when the rising edge of clock is aligned with the rising edge of data, UP = DN = 0. Fig. 2(b) shows when the clock leads the data, UP = 0 and DN = 1, the clock phase will be adjusted to be delayed. Fig. 2(c) shows when the clock lags the data, UP = 1 and DN = 0, the clock phase will be advanced.

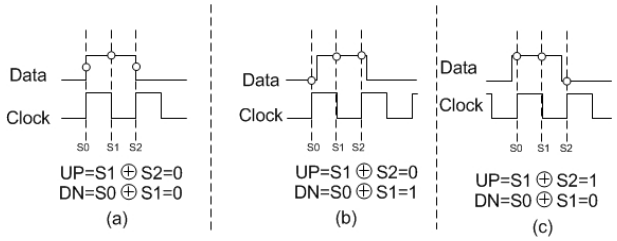


**Fig. 2** The principle of inverse half-Alexander BPD. (a) Ideal condition with phase difference equals 0, (b) early, (c) late.

The circuit structure of PD is shown in Fig. 3 constructed with flip-flops, XOR gates and a majority voter [30]. Each flip-flop unit is a flash cell sampling at the clock rising edge. Since the data rate is 12.5 Gbps and the clock frequency is 6.25 GHz, all of the cells need to be implemented by CML logic other than the low speed CMOS logic.

## 4. The phase interpolator circuit

The phase interpolator use $\alpha$ and $\beta$ signals of two different phases to synthesize $\tau$, a new phase between the two phases [12, 31]. $\alpha$ and $\beta$ come from the same clock source with the same frequency. The phase of the synthesized signal is controlled by the control signal $\psi$. The $\psi$ with different weights synthesize $\tau$ with different phases. It can be expressed as Eq. (1)

$$\tau = \frac{\psi}{\Psi} * \alpha + \frac{\Psi - \psi}{\Psi} * \beta \tag{1}$$

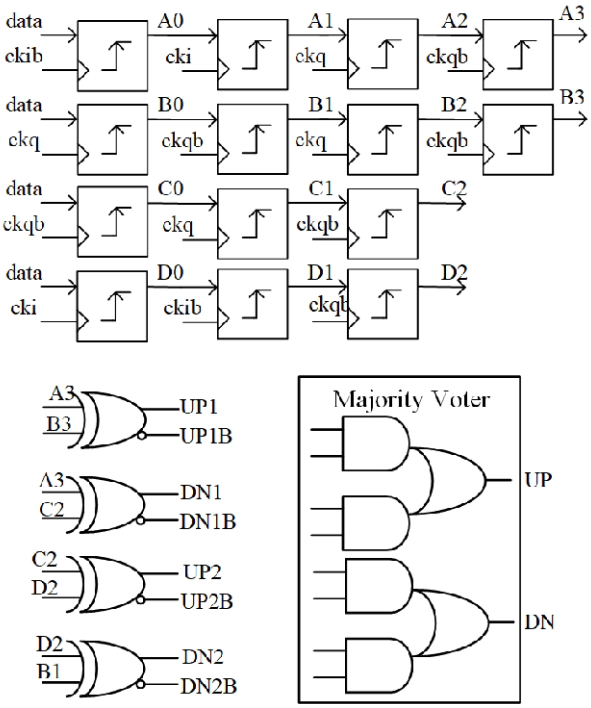


**Fig. 3** The bang-bang phase detector.

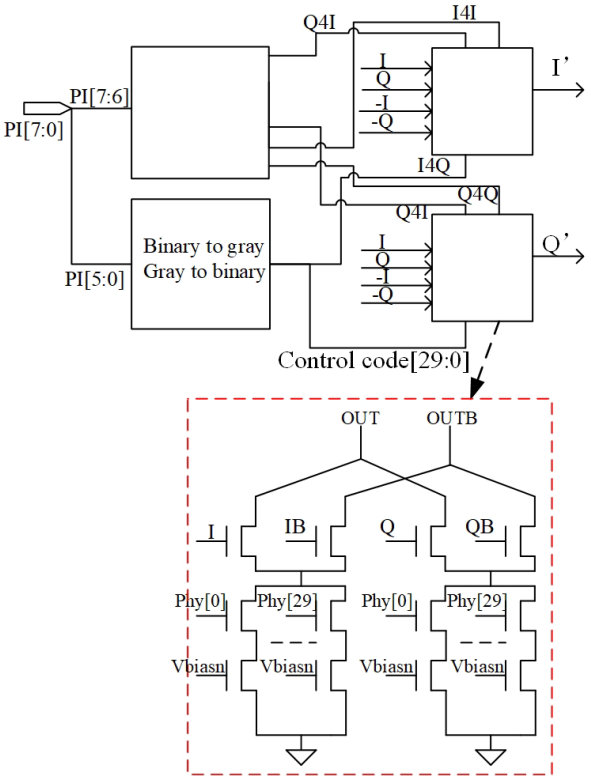


**Fig. 4** The structrue of phase interpolator circuit.

The $\Psi$ is the total weight and the $\psi$ is the variable, which is between 0 and $\Psi$. When $\psi = 0$, $\tau = \beta$, and when $\psi = \Psi$, $\tau = \beta$.

The phase interpolator is shown in the Fig. 4 consisting with code decoders and current units. PD, RWF and counter together generate a 7-bit data C[6:0]. Since the clock cycle is 360 degrees, the code range of C[6:0] is 0000000~11111111, covering a clock phase of 0~360 de-

gree. PLL provides I/Q two-way signals with a phase difference of 90 degrees. According to the previous formula, I/Q can be used to synthesize a signal in the range of 0~90 degrees.

Dividing C[6:0] into four segments, a clock signal of 0~90 degrees can be synthesized. C[6:5] is used to select the quadrant, and C[4:0] is used as the weight to control the generation of signals within 0~90 degrees. The phase precision is determined by the bits of C[4:0], where the precision is 90/32 = 2.8. Increasing the phase precision, there is needed to increase the number of bits.

Additionally, we have modified the current value corresponding different control code C[4:0] in the PI other than uniform unit current, to avoid larger time interval appear at the middle of the temperature code and smaller time interval appear at both sides of the temperature code.

### 4.1 The random work filter

The random work filter (RWF) acts as a filter in the DLL loop to regulate the response time of the DLL and reduce the jitter of the sampling clock ensuring only one of UP and DN appearance. The RWF consists of two RWF2 circuits and one RWF4 circuit, both of them implemented by CMOS state machine logic.

The RWF2, with input signal UP/DN and the output signal UPO/DNO, has three states of S-1 S0 and S1, shown in the Fig. 5. if the input UP/DN equals 00 or 11, it's state remains unchanged; if the circuit is in the state of S0, and UP/DN = 10, it will enter to S1 state and output UPO/DNO = 00; if the input signal at the next time is still UP/DN = 01, the circuit will outputs UPO/DNO = 00 and returns to S0 state; if the circuit is at the beginning of S0 state, and UP/DN = 10, it will enter to S1 state and output UPO/DNO = 00; if the input signal is UP/DN = 01 at next time, it will output UPO/DNO = 00 and return to S0 state; if the circuit at the beginning of S0 state and input signal is UP/DN = 01, it will enter to S-1 state and output UPO/DNO = 00; if the input at the next time is UP/DN = 01, it will output UPO/DNO = 01 and return to S0 state; if it starts at the state of S0 and input is UP/DN = 01, it will enter to the state of S-1 and output UPO/DNO = 00; if the input at the next time is UP/DN = 10, it will output UPO/DNO = 00 and return to the state of S0.

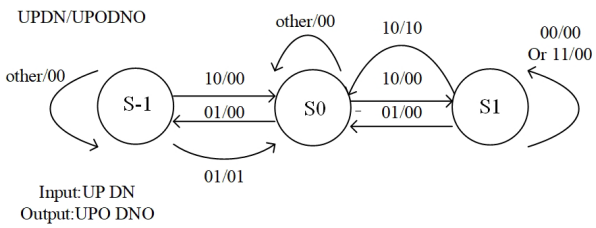


**Fig. 5** RWF2.

As for the RWF4 circuit shown in the Fig. 6, the input signal is UP/DN and the output signal is UPO/DNO. Since the input signal is from RWF2, UP/DN will not be 11 at the same time. The circuit has nine states, S-4, S-3, S-2, S-1, S0, S1, S2, S3, S4. if the value of state S-4, S-3, S-2, S-1, S1, S2, S3, S4 equals 00000000, the circuit will automatically reset

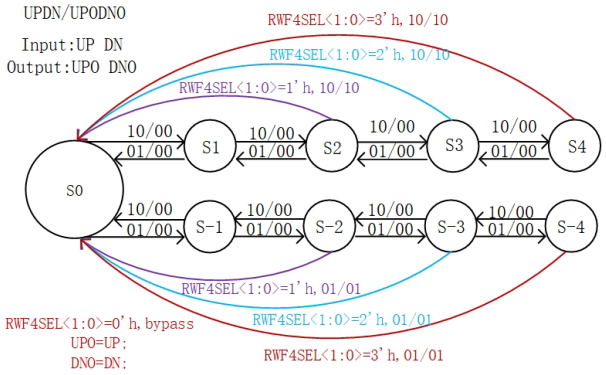


**Fig. 6** RWF4.

to 000010000. Given an example to illustrate the working process of the circuit, assuming RWF4SEL[1:0] = 11. if there is a 1 UP signal and initial circuit state is 000010000, the state will change to 000001000; if there are 2 UPs, it will changes to 000000100; if there are 3 UPs, it will change to 000000010; if there are 4 continuous UPs, it will change to 000000001, with S4 asserting 1 and UPO outputting 1, and then the state will reset to 000010000 waiting for the next signal input. If initial circuit state equals 000010000 and input 1 DN, the circuit state will change to 000100000; if there are 2 input DN signals, the state will change to 001000000; if there are 3 input DN signals, the state will change to 010000000; if there are 4 continuous input UPs, the state will change to 100000000, with S-4 asserting 1 and DNO outputting 1, and then the circuit will reset to 000010000 waiting for the next signal input.

Before the circuit reaches S-4 or S4, for each input of UP, the state moves one bit to right, and for each input of DN, the state moves one bit to the left.

### 4.2 The deserializer

The deserializer is shown in the Fig. 7. The input signals Data0 and Data1 come from BPD after the sampling clock phase is adjusted to the best position. Data0 is an even data stream, numbered 2, 4, 6, etc. Data1 is an odd data stream, numbered 1, 3, 5, etc. The signals are divided into two groups by sampling signals at the rising and failing edges of the same clock. Since the phase difference between the two groups of data is 180 degrees, the phase difference needs to be changed to 0 degrees before being sent into the serial-to-parallel circuit. The rising-edge of CKQ sampling input signal becomes *EVEN*_1, and *EVEN*_1 becomes

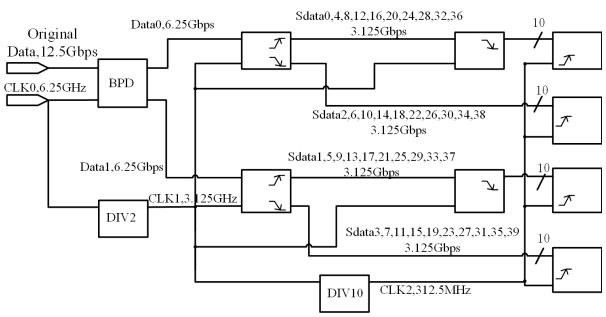


**Fig. 7** The deserializer of one 12.5 Gbps serial data to 40-bits 312.5 MHz parallel data.

*EVEN*_2 after sampling along CKQB rising-edge. *EVEN*_2 becomes *EVEN*_3 after sampling along CKQ rising-edge, and *EVEN*_3 becomes Data0 after sampling along CKQB rising-edge. CKQB rising-edge sampling input signal becomes *ODD*_1, *ODD*_1 becomes *ODD*_2 after CKQ rising-edge sampling, and *ODD*_2 becomes Data1 after CKQB rising-edge sampling. The original data rate was 12.5 Gbps, The frequency of CKQ is 6.25 GHz, and Data0/Data1 data rate is 6.25 Gbps. Then, the input 6.25 GHz clock is divided by two to generate a 3.125 GHz clock named CLK1, and the deserializer uses both rising edge and falling edge of CLK1 to sample Data0 and Data1 resulting four channel data streams (Sdata0, Sdata1, Sdata2 and Sdata3), where each data sampling channel consists of 10 shift registers. The 3.125 GHz clock is further divided by 10 to produce a clock of 312.5 MHz to sample the parallel 40-bits of the four channel data.

### 4.3 Experimental results

The proposed two channel receiver circuit is implemented using a 65-nm CMOS process. The active area of receiver chip is 1.45 × 0.899 mm$^2$ with power dissipation of 300-mW, and its layout is shown in Fig. 8. The signal, equalized by continuous-time linear equalizer, achieves a peak-to-peak jitter of 20 ps at CTLE output after post layout simulation with worst corner as shown in the Fig. 9. When the sampling clock phase is locked at the CDR, The CDR circuit aligns the rising or failing edges of CKQ1 in the middle of the data pulse and samples serial data stream correctly, as shown in the Fig. 10.

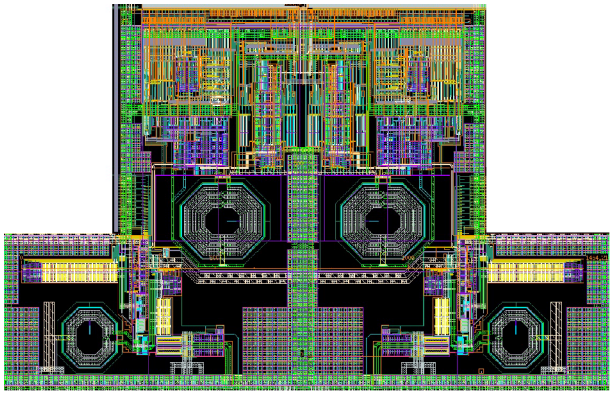

**Fig. 8** The layout of proposed two channel receiver.

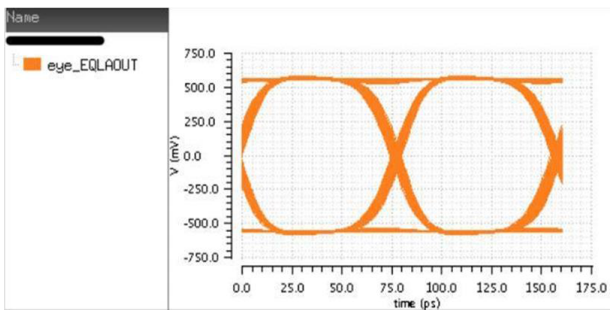


**Fig. 9** Post simulation waveform at continuous time linear equalizer output.

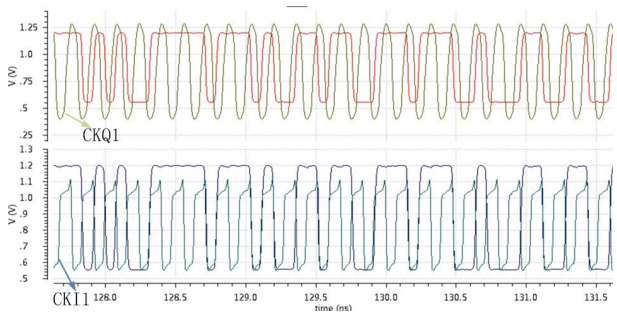


**Fig. 10** Post simulation waveform at BPD output when the CDR is already locked.

## 5. Conclusion

This paper have presented a 12.5 Gbps two channel high-speed dual loop CDR receiver based on phase interpolation (PI) sharing a PLL clock source with simplify CML and CMOS logic at BPD, RWF, counter, deserializer and controller. The whole circuit is implemented in a 65-nm low power CMOS technology, occupying an area of 1.3 mm$^2$. Post simulation results reveal that the proposed CDR show wide capture range from 3.125 Gbps to 12.5 Gbps with 300-mW power consumption from a 1.2 V supply. The proposed two channel receiver provide an ability of low voltage, low power dissipation for the back-plane up to 12.5 Gbps high speed links communication.

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