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LETTER

A low-jitter 2.4 GHz all-digital MDLL with a dithering jitter reduction scheme for 256 times frequency multiplication

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Abstract A new all-digital multiplying delay-locked loop (MDLL) based frequency multiplier architecture with a high frequency multiplication factor N of 256 is presented. The proposed MDLL utilizes a dithering jitter reduction scheme based on a delta-sigma modulation to achieve a low deterministic jitter and a large N factor. Additionally, a new stochastic phase detector is proposed to reduce static phase offset and improve jitter performance. Implemented in a 65-nm 1.0-V CMOS process, the proposed all-digital MDLL generates 2.4-GHz output clock and achieves a peak-to-peak jitter of 6.47 ps with N = 256. It occupies an active area of 0.032 mm^2 and achieves a power efficiency of 0.875 mW/GHz.
Keywords: MDLL, multiplying delay-locked loop, jitter, frequency multiplication, clock generation
Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

One of the traditional techniques for performing frequency multiplication in digital integrated circuit (IC) design is to utilize a phase-locked loop (PLL) that consists of a voltage-controlled oscillator (VCO) [1, 2, 3, 4, 5, 6, 7, 8, 9, 10]. However, basic PLLs usually have a stability problem and have a disadvantage of occupying a relatively large silicon area. Also, PLLs usually have relatively high jitter or phase noise characteristics.

Recently, multiplying delay-locked loops (MDLLs) [11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27], a type of injection-locked voltage-controlled oscillators (VCOs), have received considerable attention as on-chip clock generators for digital ICs and high-performance system-on-chips (SoCs) owing to their excellent jitter and stability performance. A typical MDLL can generate an output frequency that is N times the input clock frequency, where N is an integer. Digital MDLLs [11, 12, 13, 14, 15, 16, 17] are preferred in many applications to reduce the deterministic jitter (DJ) due to mismatch problems of analog components such as phase detectors (PDs) and charge pumps in addition to eliminating lock status loss problems during the power-down mode. Although an MDLL can reduce the integrated jitter by periodically injecting a clean reference clock, the jitter or phase noise performance rapidly degrades as the frequency multiplication factor N increases. The problem of jitter accumulation with N values becomes more acute in digital MDLLs using a bang-bang phase detector (BBPD) and a digitally controlled multiplexed ring oscillator (MRO) [14, 16, 17].

When the digital MDLL is in the lock state, the nonlinearity characteristic of the BBPD and the finite resolution of the MRO cause the phase of the MDLL output clock to move back and forth on the reference clock edge. Thus, the digital code word (DCW), i.e., the control signal of the MRO, is at least one least significant bit (LSB) dithering, assuming the loop latency of zero for simplicity. The problem is that even though the DCW only changes by one LSB during a limit cycle, the integrated phase of the MDLL output clock moves by $N \times \Delta t$, where Δt is the time resolution of the digitally controlled MRO. Consequently, as N increases or as the reference clock period (T_{REF}) increases, the magnitude of deterministic jitter (DJ) of the digital MDLL rapidly increases in proportion to N. Therefore, designing a digital MDLL with a large N is difficult, and most digital MDLLs only have N = 32 or less [12, 13, 16, 17]. To overcome this limitation, the digital MDLL introduced in [14] utilizes a scrambling time-to-digital converter (TDC) with a second-order delta-sigma modulator (DSM) to reduce the limit cycle period to 1/64 and achieve N = 128. However, the digital MDLL in [14] requires the use of an 8-bit current-mode DAC comprising 255 current sources to drive the MRO, which has a large area and high power consumption of 22.5 mW/GHz.

This Letter proposes a simple all-digital MDLL architecture with a dithering jitter reduction scheme based on a delta-sigma modulator (DSM) cell to achieve a lower DJ and larger N. To further improve the jitter performance, a new stochastic phase detector (PD) with a reduced static phase offset (SPO) is also introduced.

2. Proposed all-digital MDLL-based frequency multiplier architecture

Fig. 1 shows the architecture of the proposed all-digital MDLL-based frequency multiplier. The proposed MDLL comprises a digitally controlled MRO, a stochastic PD, a digital loop filter (DLF), three binary-to-thermometer decoders (4-to-15, 6-to-63, and 2-to-3), a second-order DSM, a select logic, and two frequency dividers (/128 and /2) for N = 256.

The proposed stochastic PD is a sub-sampling BBPD that compares the phase difference information of the input clock

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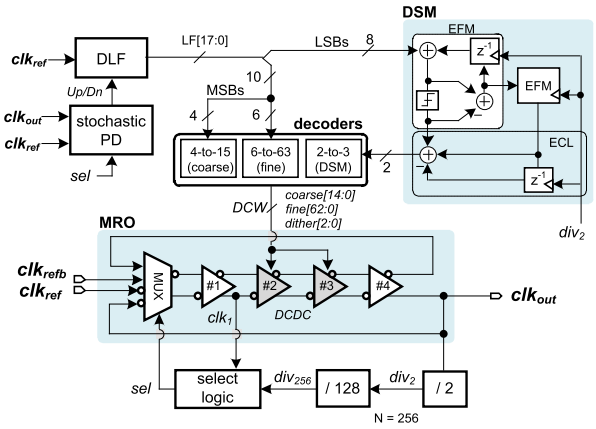


Fig. 1 Proposed all-digital MDLL-based frequency multiplier architecture

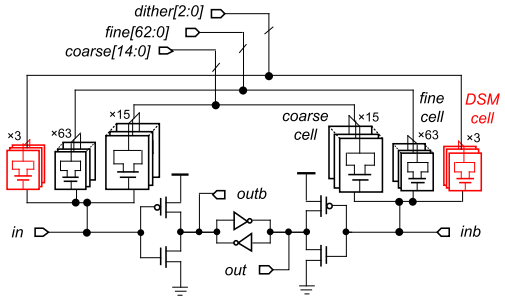


Fig. 2 Proposed digitally controlled delay cell (DCDC) in the MRO

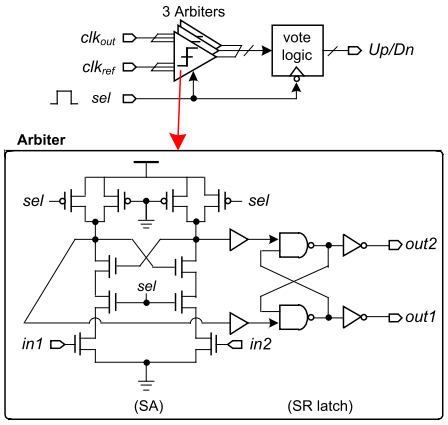


Fig. 3 Proposed stochastic PD (SPD) with reduced static phase offset

(clk_{ref}) and the feedback output clock (clk_{out}). The DLF acts as an accumulator and produces an 18-bit output signal, LF[17:0], which is incremented or decremented by one depending on the output signal Up/Dn of the stochastic PD. Owing to the nonlinear nature of the stochastic PD and the loop delay of the MDLL, the output of the DLF will toggle around the lock position during the limit cycle period. If the DLF is used to control the MRO directly while toggling, the DJ significantly increases. To solve this problem, we introduce a new dithering jitter reduction scheme that utilizes the DLF's 8-bit LSBs as the input to the second-order DSM and uses the output of the DSM directly to control the MRO. The digitally controlled MRO comprises a 2-to-1 differential multiplexer (MUX) and a four-stage pseudo-differential delay line (#1–#4). The upper 4-bits of the DLF output, LF[17:14], generate the coarse[14:0] signal that controls the coarse delay of the MRO through the 4-to-15 thermometer decoder. The LF[13:8] generates the fine[62:0] signal through the 6-to-63 decoder. The 2-to-3 decoder receives the 2-bit output of the DSM and generates the dither[2:0] signal. The second-order DSM comprises two error feedback modulators (EFMs) and an error cancellation logic (ECL). Because the DSM operates at half the frequency of the MDLL output, the DSM cells of the MRO, controlled by the dither[2:0] signal, operate at a frequency 128 times higher than the operating frequency of the stochastic PD. To reduce power consumption, true single-phase clock (TSPC) flip-flops are used as registers in the DSM. The select logic is used to control the MUX and set the enable period for the stochastic PD.

Fig. 2 shows the schematic of the digitally controlled delay cell (DCDC), which constitutes *#2* and *#3* delay cells of the MRO. The DCDC is based on a pseudo-differential inverter structure with varactors. The coarse delay resolution of the coarse cells, which can be adjusted with coarse[14:0], is about 8 ps. The fine delay resolution of the fine cells using fine[62:0] is about 0.13 ps. The DSM generates a control bit dither[2:0] that finely controls the delay of the DSM cells at high frequencies. The dithering delay resolution of the DSM cell is the same as the fine delay resolution.

Fig. 3 shows the schematic of the proposed stochastic PD (SPD), which comprises three identical arbiters (ARBs) and one vote logic. The arbiter is a sense-amplifier flip-flop (SAFF) [28, 29] containing a sense-amplifier (SA) and a set-reset (SR) latch. The SA operates only during the high pulse of the sel signal, and by determining which edge of the two input signals (in1, in2) arrives first, the stochastic PD acts as a sub-sampling BBPD. The PD mismatch due to process variations causes an SPO, which in turn increases the DJ of the MDLL. In this paper, a stochastic approach is used to reduce the PD offset. By applying the same input signal (clk_{ref} and clk_{out}) to the three identical arbiters and using the outputs in the vote logic to determine the majority, accurate phase error information between the two input signals can be obtained. This majority voting task involves choosing the median of the time offset, which renders the characteristics of the proposed stochastic PD closer to the ideal arbiter with a reduced SPO.

The stochastic properties of a set of arbiters have been used in high-resolution time-to-digital converter (TDC) designs [29, 30]. Conventional stochastic TDCs only aim at the digital conversion of time error information. To achieve high resolution and large linear ranges, traditional stochastic TDCs require a significant number of arbiters (e.g., 1024 in [30]), resulting in a very large area and power consumption. However, the proposed stochastic PD is especially designed for PDs with reduced SPO and has a small area because only three arbiters are used. In addition, each arbiter operates only for a very short sel pulse period; hence, the power consumption is very low.

Fig. 4 shows the conceptual illustration of the proposed dithering jitter reduction scheme. As shown in the upper panel, when the DSM is turned off, the DCW of the MRO repeatedly toggles during the limit cycle ($= 2 \times T_{REF}$ in this example). Here, the DCW dithers just one LSB, but the

misalignment between clk_{ref} and clk_{out} edges appears as a period error in the MRO output at each reference injection, showing that the period of MRO (T_{MRO}) significantly deviates from the ideal T_{MRO}. This appears as reference spurs in the output spectrum and leads to a severely increased DJ. The DJ increases in proportion to N and the limit cycle period.

In contrast, when the DSM is turned on, as shown in the lower panel, the DCW toggles 128 times faster than the upper case with the action of the second-order DSM. The DSM generates a high-frequency 2-bit pseudo-random output pattern, the average value of which is equivalent to the low-frequency 8-bit input LF[7:0]. The T_{MRO} does not deviate significantly from the ideal value by continuously controlling the DSM cells (shown in Fig. 2) at high frequencies. This technique is similar to high-frequency delta-sigma dithering applied to a digital phase-locked loop (PLL) design used in [29]. However, [29] requires additional current-mode digital-to-analog converters (DACs), adding the overhead of increased area and power consumption. Consequently, implementing the proposed dithering jitter reduction scheme reduces the jitter accumulation time to 1/128 in proportion to the operating period of the DSM (T_{DSM}) and effectively achieves excellent DJ characteristics even though N is as large as 256. Fig. 5 shows the simulation result of the MDLL using the proposed dithering jitter reduction scheme with N = 256 at 2.4 GHz. The DCW toggles by 3 LSBs and the jitter of the output clock, clk_{out}, is less than approximately 1.5 ps at maximum for a given period.

3. Experimental results

Fig. 6 shows the layout of the proposed all-digital MDLL having an active area of 0.032 mm^2. The MDLL has been designed in a 65-nm 1-V CMOS process. The MDLL achieves a high N of 256 and dissipates only 2.1 mW at 2.4 GHz (= 0.875 mW/GHz) from a reference frequency of 9.375 MHz. Fig. 7 shows the Monte-Carlo simulation result of the proposed stochastic PD. The stochastic PD using one arbiter has a standard deviation of 0.295 ps as the input-referred time offset due to device mismatch. The standard deviation of the stochastic PD using three arbiters is 0.185 ps; thus, the mismatch-induced time offset is reduced by 37.3% compared to the one arbiter structure.

Fig. 8 shows the simulated output clock jitter of the proposed all-digital MDLL operating at 2.4 GHz with N = 256. Fig. 8(a) shows the jitter value when the DSM is turned off, which shows a peak-to-peak (p-p) jitter of 38.59ps

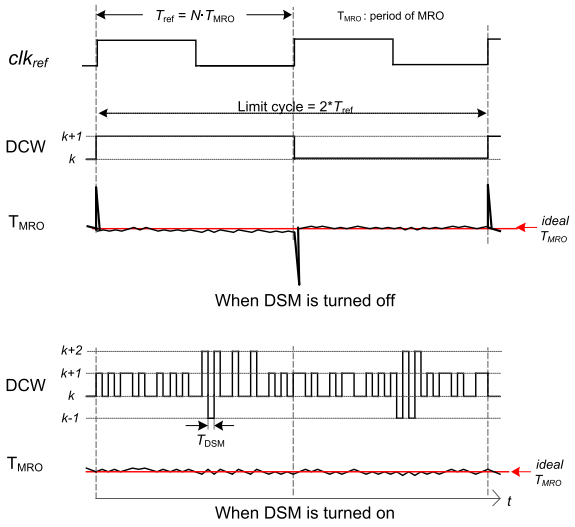


Fig. 4 Conceptual illustration of the proposed dithering jitter reduction scheme

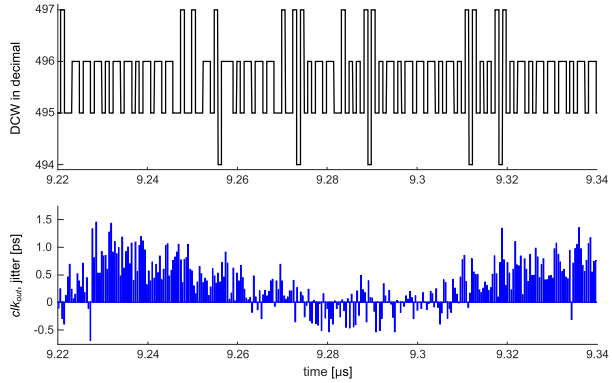


Fig. 5 Simulated MDLL operation using the dithering jitter reduction scheme (N = 256)

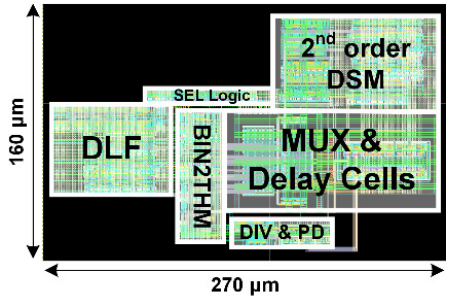


Fig. 6 Layout of the proposed all-digital MDLL core

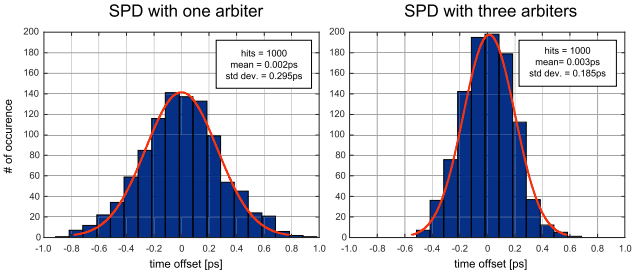


Fig. 7 Monte-Carlo simulation result of the proposed stochastic PD

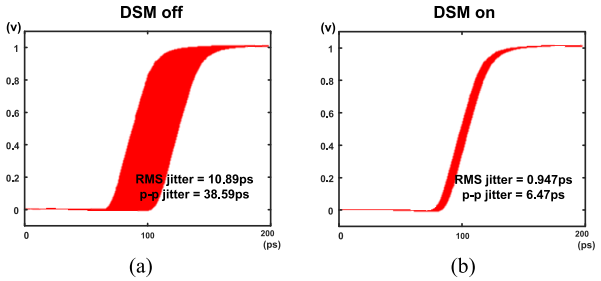


Fig. 8 Simulated output clock jitter of the proposed MDLL (@2.4GHz, N = 256) (a) DSM off (b) DSM on

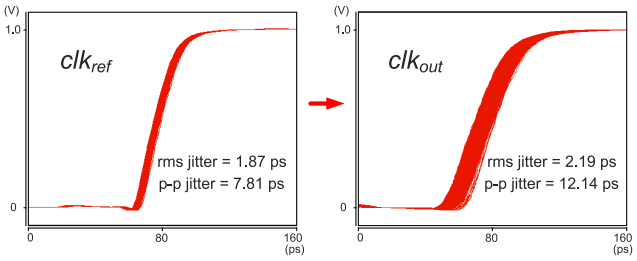
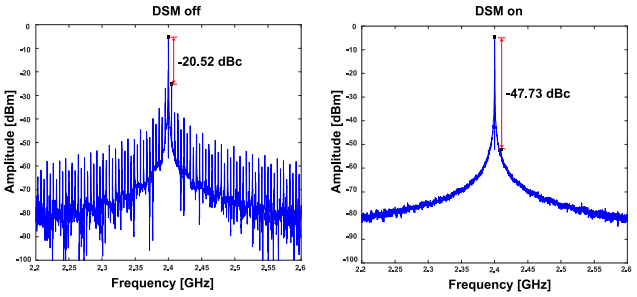


Fig. 9 Simulated output p-p clock jitter with an injected input clock p-p jitter of 7.81 ps



(a) (b)

Fig. 10 Simulated reference spur characteristics of the proposed MDLL (@2.4GHz, N = 256) with (a) DSM turned off and (b) DSM turned on

Table I Performance comparison of state-of-the-art digital MDLLs

	[12] JSSC 17	[14] TCAS17	[16] JSSC 17	[17] JSSC 08	**This Work**
Process & Supply	65 nm 1.2 V	90 nm 1.0 V	28 nm 1.1 V	130 nm 1.2 V	65 nm 1.0 V
Output freq. [GHz]	1.4	0.16	2.4	1.6	2.4
Reference freq. [MHz]	87.5	1.25	75	50	9.375
Multiplication factor N	16	128	32	32	256
p-p / RMS jitter [ps]	– / 2.0	22.1 / 2.4	15.89 / 0.7	11.1 / 0.93	6.47 / 0.947
Power [mW]	8.0	3.6	1.51	9.2	2.1
Power efficiency [mW/GHz]	5.71	22.5	0.63	5.75	0.875
Active area [mm^2]	0.054	0.10**	0.024	0.76	0.032

* Simulated result
** MDLL + PLL area

(RMS jitter = 10.89 ps). In contrast, as shown in Fig. 8(b), when the proposed DSM is turned on, the p-p jitter becomes only 6.47 ps (RMS jitter = 0.947 ps), which is reduced by more than 83%.

Fig. 9 depicts the simulated jitter performance of the MDLL when the reference noise is intentionally applied to the input clock at 2.4 GHz and N = 256. When a 7.81 p-p jitter is injected, the proposed MDLL obtains a p-p jitter of 12.14 ps (RMS jitter = 2.19 ps). This shows that the proposed MDLL operates stably against input jitter noise, and the effective p-p jitter is only about 4.33 ps (= 12.14 ps – 7.81 ps).

Fig. 10 shows the simulated reference spur of the proposed MDLL with an input frequency of 9.375 MHz and a multiplication factor N = 256 for a center frequency of 2.4 GHz. When the DSM is turned off, the spur level is −20.52 dBc. However, when the DSM is turned on, the spur level becomes −47.73 dBc. This result is consistent with the jitter characteristics shown in Fig. 8.

Table I compares the performance of the proposed MDLL with other state-of-the-art digital MDLLs with large *N* factors. The values measured in this work in Table I are the simulation results. Among the compared digital MDLLs, the proposed MDLL achieves the largest N of 256 while consuming relatively low power and showing excellent jitter characteristics.

4. Conclusion

In this Letter, we presented a novel all-digital MDLL frequency multiplier with a high N factor of 256 for low-power SoCs. The proposed MDLL achieves a low DJ by using a new dithering jitter reduction scheme based on a delta-sigma DSM cell. The MDLL also adopts a new stochastic PD that can reduce SPO and improve jitter performance. Implemented in a 65-nm 1.0-V CMOS process, the 2.4 GHz MDLL achieves a low p-p jitter of 6.47 ps with N = 256. In addition, the proposed simple MDLL architecture achieves a high power efficiency of 0.875 mW/GHz.

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References

[1] N.D. Dalt, *et al.*: “A compact triple-band low-jitter digital LC PLL with programmable coil in 130-nm CMOS,” IEEE J. Solid-State Circuits **40** (2005) 1482 (DOI: 10.1109/JSSC.2005.847325).
[2] N.D. Dalt: “A design-oriented study of the nonlinear dynamics of digital bang–bang PLLs,” IEEE Trans. Circuits Syst. I, Reg. Papers **52** (2005) 21 (DOI: 10.1109/TCSI.2004.840089).
[3] R.B. Staszewski, *et al.*: “All-digital PLL and transmitter for mobile phones,” IEEE J. Solid-State Circuits **40** (2005) 2469 (DOI: 10.1109/JSSC.2005.857417).
[4] J. Lin, *et al.*: “A PVT tolerant 0.18 MHz to 600 MHz self-calibrated digital PLL in 90 nm CMOS process,” IEEE ISSCC Dig. Tech. Papers (2004) 488 (DOI: 10.1109/ISSCC.2004.1332807).
[5] S.-Y. Yang, *et al.*: “A 7.1 mW, 10 GHz all-digital frequency synthesizer with dynamically reconfigured digital loop filter in 90 nm CMOS technology,” IEEE J. Solid-State Circuits **45** (2010) 578 (DOI: 10.1109/JSSC.2009.2039530).
[6] J.A. Tierno, *et al.*: “A wide power supply range, wide tuning range, all static CMOS all digital PLL in 65 nm SOI,” IEEE J. Solid-State Circuits **43** (2008) 42 (DOI: 10.1109/JSSC.2007.910966).
[7] E. Alon, *et al.*: “Replica compensated linear regulators for supply-regulated phase-locked loops,” IEEE J. Solid-State Circuits **41** (2006) 413 (DOI: 10.1109/JSSC.2005.862347).
[8] A. Arakali, *et al.*: “Low-power supply-regulation techniques for ring oscillators in phase-locked loops using a split-tuned architec-

ture," IEEE J. Solid-State Circuits **44** (2009) 2169 (DOI: 10.1109/JSSC.2009.2022916).
[9] K.K. Chang, *et al.*: "A 0.44-Gb/s CMOS quad transceiver cell using on-chip regulated dual-loop PLLs," IEEE J. Solid-State Circuits **38** (2003) 747 (DOI: 10.1109/JSSC.2003.810045).
[10] W. Grollitsch, *et al.*: "A 1.4 psrms-period-jitter TDC-less fractional-N digital PLL with digitally controlled ring oscillator in 65 nm CMOS," IEEE ISSCC Dig. Tech. Papers (2010) 478 (DOI: 10.1109/ISSCC.2010.5433839).
[11] A. Elshazly, *et al.*: "Clock multiplication techniques using digital multiplying delay-locked loops," IEEE J. Solid-State Circuits **48** (2013) 1416 (DOI: 10.1109/JSSC.2013.2254552).
[12] S. Kundu, *et al.*: "A 0.2–1.45-GHz subsampling fractional-N digital MDLL with zero-offset aperture PD-based spur cancellation and in situ static phase offset detection," IEEE J. Solid-State Circuits **52** (2017) 799 (DOI: 10.1109/JSSC.2016.2638432).
[13] G. Marucci, *et al.*: "A 1.7 GHz MDLL-based fractional-N frequency synthesizer with 1.4ps RMS integrated jitter and 3 mW power using a 1b TDC," IEEE J. Solid-State Circuits **50** (2015) 2678 (DOI: 10.1109/ISSCC.2014.6757469).
[14] R.K. Nandwana, *et al.*: "A 1-to-2048 fully-integrated cascaded digital frequency synthesizer for low frequency reference clocks using scrambling TDC," IEEE Trans. Circuits Syst. I, Reg. Papers **64** (2017) 283 (DOI: 10.1109/TCSI.2016.2609855).
[15] J. Kim and S. Han: "A fast-locking all-digital Multiplying DLL for fractional-ratio dynamic frequency scaling," IEEE Trans. Circuits Syst. II, Exp. Briefs **65** (2018) 276 (DOI: 10.1109/TCSII.2017.2688369).
[16] H. Kim, *et al.*: "A 2.4-GHz 1.5-mW digital multiplying delay-locked loop using pulsewidth comparator and double injection technique," IEEE J. Solid-State Circuits **52** (2017) 2934 (DOI: 10.1109/JSSC.2017.2734910).
[17] B.M. Helal, *et al.*: "A highly digital MDLL-based clock multiplier that leverages a self-scrambling time-to-digital converter to achieve subpicosecond jitter performance," IEEE J. Solid-State Circuits **43** (2008) 855 (DOI: 10.1109/JSSC.2008.917372).
[18] Y.-K. Chiu and S.-I Liu: "A PVT-tolerant MDLL using a frequency calibrator and a voltage monitor," IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **27** (2019) 2698 (DOI: 10.1109/TVLSI.2019.2925820).
[19] S. Kundu, *et al.*: "A self-Calibrated 1.2-to-3.8GHz 0.0052mm2 synthesized fractional-N MDLL using a 2b time-period comparator in 22nm FinFET CMOS," 2020 IEEE International Solid-State Circuits Conference (2020) 276 (DOI: 10.1109/ISSCC19947.2020.9062939).
[20] S. Levantino, *et al.*: "A 1.7 GHz fractional-N frequency synthesizer based on a multiplying delay-locked loop," IEEE J. Solid-State Circuits **50** (2015) 2678 (DOI: 10.1109/JSSC.2015.2473667).
[21] H. Hwang and J. Kim: "A 100 Gb/s quad-lane SerDes receiver with a PI-based quarter-rate all-digital CDR," Electronics **9** (2020) 1113 (DOI: 10.3390/electronics9071113).
[22] G.-Y. Tak and K. Lee: "A low-reference spur MDLL-based clock multiplier and derivation of discrete-time noise transfer function for phase noise analysis," IEEE Trans. Circuits Syst. I, Reg. Papers **65** (2018) 485 (DOI: 10.1109/TCSI.2017.2719685).
[23] A. Santiccioli, *et al.*: "A 1.6-to-3.0-GHz fractional-N MDLL with a digital-to-time converter range-reduction technique achieving 397fs jitter at 2.5-mW power," 2019 IEEE Custom Integrated Circuits Conference (2019) 1 (DOI: 10.1109/CICC.2019.8780235).
[24] R. Farjad-Rad, *et al.*: "A low-power multiplying DLL for low-jitter multigigahertz clock generation in highly integrated digital chips," IEEE J. Solid-State Circuits **37** (2002) 1804 (DOI: 10.1109/JSSC.2002.804340).
[25] T.A. Ali, *et al.*: "A 4.6GHz MDLL with −46dBc reference spur and aperture position tuning," 2011 IEEE International Solid-State Circuits Conference (2011) 466 (DOI: 10.1109/ISSCC.2011.5746400).
[26] J. Kim and B. Bae: "An anti-harmonic MDLL for phase aligned on-chip clock multiplication," IEICE Electron. Express **15** (2018) 1 (DOI: 10.1587/elex.15.20180042).
[27] J. Kim and B.-H. Bae: "A 2-4 GHz fast-locking frequency multiplying delay-locked loop," IEICE Electron. Express **14** (2017) 1 (DOI: 10.1587/elex.13.20161056).
[28] B. Nikolic, *et al.*: "Improved sense-amplifier-based flip-flop: design and measurements," IEEE J. Solid-State Circuits **35** (2000) 876 (DOI: 10.1109/4.845191).
[29] V. Kratyuk, *et al.*: "A digital PLL with stochastic time-to-digital converter," IEEE Trans. Circuits Syst. I, Reg. Papers **56** (2009) 1612 (DOI: 10.1109/TCSI.2008.2010109).
[30] S. Pellerano, *et al.*: "A 4.75-GHz fractional frequency divider-by-1.25 with TDC-based all-digital spur calibration in 45-nm CMOS," IEEE J. Solid-State Circuits **44** (2009) 3422 (DOI: 10.1109/JSSC.2009.2032276).