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An Implementation of Improved PLL for Control of Grid-Connected Converters Under Grid Perturbations

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Abstract
In this article, a new method is proposed for calculating electric angle using a phase-locked loop (PLL) to perform these calculations correctly under disturbance conditions of the grid voltage. This work is based on using the decoupled double synchronous reference frame PLL (DDSRF-PLL), and this kind of PLL has been expanded to solve its problems in the presence of harmonics and high disturbance in the input voltage. In the DDSRF-PLL, only components with a frequency of double the fundamental frequency will be deleted, but in the expanded PLL all the harmonics will be eliminated. The effect of this method was tested using both simulation and practical experimentation. The simulation of this method was performed in MATLAB software. It has been shown that this method is robust, precise and fast for calculating the electric angle under grid voltage perturbations. Subsequently, the developed PLL was implemented in a FPGA-based experimental setup and its function was studied.

Keywords Unbalanced grid · Grid-connected converters · Phase-locked loop (PLL) · Synchronous reference · Frame (SRF)

1 Introduction

Over the past two decades, wind turbines have been developed. These turbines are usually installed in areas where the distribution grid is weak and there is an unbalanced grid voltage (Valouch et al. 2015; Conlon et al. 2006). Power quality problems are commonly found at the points of the grid where the wind turbines are connected. Voltage imbalance is a power quality problem that negatively affects wind turbine performance. Voltage imbalance can cause asymmetrical currents in the stator of wind generators; as a result, the protection system will trip the turbine (Kearney and Conlon 2007). Different control methods are provided for controlling wind turbine. Most of the wind turbine controllers presented in articles are based on vector control (Leonard 1995). Examples of which are shown in reference (Pena et al. 1996). In most of the methods, it is assumed that the stator voltage is ideal, meaning that the frequency and amplitude of the stator voltage are constant, and the dynamics of the stator magnetizing current is not considered (Buja and Kazmierkowski 2004; Conraths 2001). These systems have a good dynamic response in normal operation, but their performance may be weak during AC voltage disturbances.

In these types of controllers, the grid voltage angle is extracted using PLL. The important thing about these controllers is that the PLL correctly calculates the electric angle. In the case of fault conditions and disturbances in grid voltages, the PLLs used in these controllers have different performances. In recent years, many efforts have been made to design three-phase PLLs with better performance. Most of these efforts have been made on the ability to eliminate the oscillatory components in the tracked frequency in conventional SRF-PLL and its related issues (Bojoi et al. 2005; Carugati et al. 2012; Eren et al. 2009; Meral 2012; Gonzalez-Espin et al. 2012; Donato et al. 2016; Luna et al. 2015; Golestan et al. 2014a, b). An ordinary SRF-PLL was used which performed poorly against grid imbalance and harmonics in another study (Choi et al. 2006). DDSRF-PLL was used in the previous studies (Rodríguez et al. 2002, 2006a, b). DDSRF-PLL solves the weakness of SRF-PLL against asymmetric input by finding a positive sequence of grid

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voltages and negative voltage sequence in Park transformation and using a separator unit to extract the positive and negative net sequences without a destructive effect due to the asymmetric grid voltage, but it behaves poorly against the removal of grid harmonics. A PLL with repetitive learning was used to improve the power quality of DC micro-grids attached to the grid, under a degraded voltage in a weak grid in one study (Sahoo et al. 2017). A dual second-order generalized integrator PLL (DSOGI-PLL) is presented in another study (Rodriguez et al. 2006a, b). Two second-order generalized integrators were used to generate a positive sequence of the grid voltage. In the work of Rodriguez et al. (2009), a similar method is proposed but using the multiple second-order generalized integrator (MSOGI-PLL) to eliminate the harmonic characteristics of the grid voltage. In the work of Xiao et al. (2017), a new frequency-fixed SOGI-based PLL (FFSOGI-PLL) is suggested that ensures stability and simple implementation. In another study (Gude and Chu 2018), multiple delayed signal cancelation (MDSC) filter is proposed and integrated into three-phase enhanced PLL. The effect of grid voltage harmonics, unbalance, and dc offsets can be eliminated with two MDSC filters inside 3P-EPLL loops. In another study (Neves et al. 2010), the delayed signal cancelation PLL (DSC-PLL) is presented, which has the ability to properly filter grid voltage harmonics. The structure of an improved frequency-adaptive DSC-PLL is also proposed in the previous studies (Hamed et al. 2017; Golestan et al. 2017). In this method, the PLL is adapted to the grid frequency variation. In another study (Huang and Rajashekara 2016), a PLL is presented that cascades only one DSC block and one moving average filter (MAF) block in the loop. MAF is discussed in numerous studies (Freijedo et al. 2009; Golestan et al. 2014a, b; Wang et al. 2015). Multi-reference base frame PLL (MRF-PLL) (Xiao et al. 2008) and multiple complex-coefficient-filter-based PLL (MCCF-PLL) (Guo et al. 2011) are examples of pre-filtered PLLs, which remove double-frequency oscillations created by the original frequency of the negative sequence component. These PLLs can also be expanded to reject some of the lower-order harmonics along with the original frequency of negative sequences.

DDSRF-PLL method is used in this paper. This type of PLL is modified to solve its problems in the presence of harmonics and high disturbance in the grid. But in this PLL, only components with double the fundamental frequency will be deleted. In the PLL extended in this paper, all the harmonics will be eliminated. This is accomplished by adding a mean value block in the output of the decoupling network block and eliminating the effect of harmonics with this method. In the second section, how to calculate the electric angle using PLL and the assessment and simulation of conventional PLLs are presented. The third part presents the proposed PLL plan and is compared with the previous ones. The simulation of PLL designed has been conducted in this section, and its results have been analyzed. In the fourth section, the fabrication of the PLL designed in a laboratory setup has been introduced and its function has been examined, and finally, the results of this study were examined in the fifth section.

2 Calculation of θ_e

There are various ways to calculate the electrical angle. Among them, we can mention zero-cross detection of the signal in a period and PLL. The accuracy of the zero-cross detection method is not high, and this method is not efficient enough when the signal is distorted. In this paper, the PLL method was used to calculate the electrical angle.

2.1 Mathematical Fundamentals of PLL

The usual method for calculating the stator electrical angle or grid is PLL. PLL is usually based on a dq synchronous reference frame. As is known, the input three-phase equation is as follows:

$$V_a = V_{\mathrm{m}} \sin(\theta_1) \tag{1}$$

$$V_b = V_{\mathrm{m}} \sin(\theta_1 - 2\pi/3) \tag{2}$$

$$V_c = V_{\mathrm{m}} \sin(\theta_1 - 4\pi/3) \tag{3}$$

where θ_1 is the electrical angle to be tracked.

Using Clarke transformation, v_α, v_β are calculated as follows:

$$V_\alpha = K \cdot V_{\mathrm{m}} \sin(\theta_1) \tag{4}$$

$$V_\beta = K \cdot V_{\mathrm{m}} \cos(\theta_1) \tag{5}$$

The equations above are turned into two DC components using Park transformation:

$$V_d = V_\alpha \sin(\theta_2) + V_\beta \cos(\theta_2) \tag{6}$$

$$V_q = V_\alpha \cos(\theta_2) - V_\beta \sin(\theta_2) \tag{7}$$

where θ_2 is the angle used for the Park transformation.

After simplification using trigonometric equations, v_d, v_q are calculated as follows:

$$V_d = K \cdot V_{\mathrm{m}} \sin(\theta_2) \cdot \sin(\theta_1) + K \cdot V_{\mathrm{m}} \cos(\theta_2) \cdot \cos(\theta_1) \tag{8}$$

$$V_q = K \cdot V_{\mathrm{m}} \sin(\theta_1) \cdot \cos(\theta_2) - K \cdot V_{\mathrm{m}} \sin(\theta_2) \cdot \cos(\theta_1) \tag{9}$$

Therefore:

$$V_d = K_2 \cos(\theta_1 + \theta_2) \tag{10}$$

$$V_q = -K_2 \sin(\theta_1 - \theta_2) \tag{11}$$

The PLL forces v_q into zero, therefore:

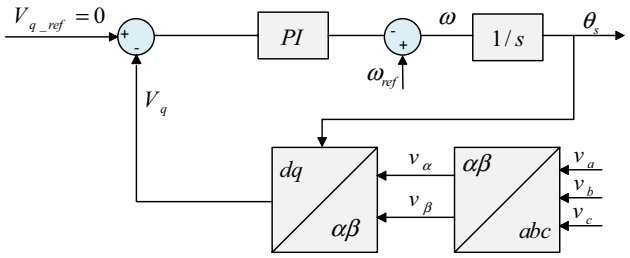


Fig. 1 Block diagram of SRF-PLL

A PI improves system performance by canceling stationary status error. Thus, v_q would be equal to zero, and v_d would have a positive value.

2.1.2 Distributed PLL Considering Voltage Imbalance (DDSRF[2]-PLL)

If an imbalance exists in the input voltage, the k coefficients in Eqs. 4 and 5 will not be equal. Therefore, after applying several trigonometric transformations, a sine term would exist that always appears in the output of the Park transformation. As PLL has a PI loop and the PI controller does not work well for non-DC inputs and does not converge, PLL will not lock on v_q voltage and θ_s will not be calculated accurately. This means that when grid voltage is unbalanced, PLL will not give an accurate electrical angle. DDSRF-PLL has solved the weakness of SRF-PLL against asymmetric inputs by finding the positive sequence of grid voltage and the negative sequence of the voltage in the Park transformation, using a separating unit to extract the positive and negative sequences without the negative side effects of the asymmetry in the grid voltage. DDSRF-PLL is an advanced case of SRF-PLL and is designed for asymmetric three-phase voltage (Rodriguez et al. 2007). In this kind of PLL, the concept of "symmetric component" is used. This PLL is suitable for applications that need to know the positive and negative sequences in the grid voltage. Figure 2 shows this type of PLL. In this figure, ω_{ref} is nominal grid frequency.

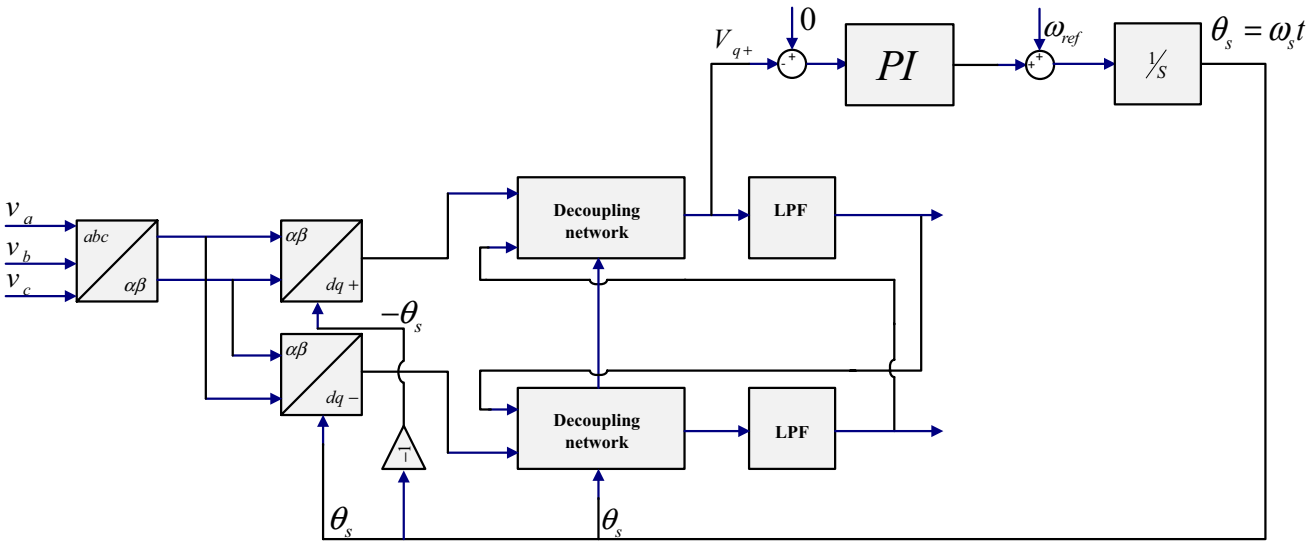


Fig. 2 Block diagram of DDSRF-PLL

$$V_q = 0 \rightarrow \theta_1 = \theta_2 \tag{12}$$

2.1.1 SRF[1]-PLL

The simplest PLL used for calculating the electrical angle is synchronous reference frame (SRF) (Kaura and Blasco 1997; Chung 2000). The schematic of a simple PLL (SRF) is shown in Fig. 1.

The input of PLL is the stator or grid voltage, and its output is the electrical angle tracked by PLL. In this kind of PLL, both Park and Clarke transformations are applied to the input voltage and the q-component of the Park transformation is inserted in the PLL loop. This v_q is compared with the reference v_q which is equal to zero. To use the Park transformation, the input signal electrical angle which is the output of the PLL loop is needed. A PI controller is responsible for controlling the changes in v_q and impelling them to zero, and the output of this regulator is the grid frequency.

[1] Synchronous Reference Frame.

[2] Decoupled Double Synchronous Reference Frame.

In this PLL, a Clarke transformation is first done on the three-phase input voltage. Then, two Park transformations with reverse $\theta's$ are done on the output of the Clarke transformation. The matrices which convert the Clarke transformation to a Park transformation for positive and negative sequences are shown in Eqs. 13 and 14 (Rodriguez et al. 2007).

$$T^{+} = \begin{bmatrix} \cos(\omega_s t) & \sin(\omega_s t) \\ -\sin(\omega_s t) & \cos(\omega_s t) \end{bmatrix} \tag{13}$$

$$T^{-} = \begin{bmatrix} \cos(\omega_s t) & -\sin(\omega_s t) \\ \sin(\omega_s t) & \cos(\omega_s t) \end{bmatrix} \tag{14}$$

From the theory of symmetrical components, it is known that any unbalanced three-phase grid can be reduced to two symmetrical systems and zero component. However, only faults and disturbances including the ground have the zero sequence component. The one rotating in the positive direction is called the positive sequence, and the other rotating in the negative sequence called the negative sequence.

$$v = v^{+}\begin{bmatrix} \cos(\omega_s t + \varphi_{+1}) \\ \cos(\omega_s t - 2\pi/3 + \varphi_{+1}) \\ \cos(\omega_s t - 4\pi/3 + \varphi_{+1}) \end{bmatrix} + v^{-}\begin{bmatrix} \cos(\omega_s t + \varphi_{-1}) \\ \cos(\omega_s t - 4\pi/3 + \varphi_{-1}) \\ \cos(\omega_s t - 2\pi/3 + \varphi_{-1}) \end{bmatrix} + v^{0}\begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{15}$$

In Eq. 15, three-phase asymmetric input voltages are assumed as three positive, negative and sequences. In this equation, v^{+},v^{-} and v^{0} are amplitude of sequences. In Eq. 16, the Clarke transformation is applied to the three-phase input voltage.

$$v_{\alpha\beta} = T_{\alpha\beta} * v = v^{+}\begin{bmatrix} \cos(\omega_s t + \varphi_{+1}) \\ \sin(\omega_s t + \varphi_{+1}) \end{bmatrix} + v^{-}\begin{bmatrix} \cos(-\omega_s t + \varphi_{-1}) \\ \sin(-\omega_s t + \varphi_{-1}) \end{bmatrix} \tag{16}$$

where $T_{\alpha\beta}$ is Clarke transformation and equal to:

$$T_{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{17}$$

By performing a Park transformation in the two cases of positive and negative θ's, the components of $d+$, $d-$, $q+$ and $q-$ are achieved. The asymmetry in the three-phase input voltage reveals itself as sine and cosine equations with arguments twice those of the three-phase input voltage. These arguments are unwanted and must be eliminated. In order to achieve a Park transformation, the Clarke transformation is multiplied by the T^{+} matrix.

$$v_{dq+} = \begin{bmatrix} \cos(\omega_s t) & \sin(\omega_s t) \\ -\sin(\omega_s t) & \cos(\omega_s t) \end{bmatrix} * \left(v^{+}\begin{bmatrix} \cos(\omega t + \varphi_{+1}) \\ \sin(\omega t + \varphi_{+1}) \end{bmatrix} + v^{-}\begin{bmatrix} \cos(-\omega_s t + \varphi_{-1}) \\ \sin(-\omega_s t + \varphi_{-1}) \end{bmatrix} \right) \tag{18}$$

After simplification:

$$\begin{aligned} v_{dq+} = {} & v^{+}\begin{bmatrix} \cos(\varphi_{+1}) \\ \sin(\varphi_{+1}) \end{bmatrix} + v^{-}\cos(\varphi_{-1})\begin{bmatrix} \cos(2\omega_s t) \\ -\sin(2\omega_s t) \end{bmatrix} \\ & + v^{-}\sin(\varphi_{-1})\begin{bmatrix} \sin(2\omega_s t) \\ \cos(2\omega_s t) \end{bmatrix} \end{aligned} \tag{19}$$

In this PLL, these elements are eliminated in the decoupling network block. After periodic simplifications, v_{d+}, v_{q+} are achieved, and their second and third elements are unwanted.

$$v_{d+\_\text{decoupled}} = v^{+}\cos(\varphi_{+1}) = v_{d+} - \underset{d-}{\bar{v}}\cos(2\omega_s t) - \underset{q-}{\bar{v}}\sin(2\omega_s t) \tag{20}$$

$$v_{q+\_\text{decoupled}} = v^{+}\sin(\varphi_{+1}) = v_{q+} + \underset{d-}{\bar{v}}\sin(2\omega_s t) - \underset{q-}{\bar{v}}\cos(2\omega_s t) \tag{21}$$

In these two expressions, the sine and cosine parts in the decoupling network block will be eliminated. To eliminate these elements, they are first passed through a first-order low-pass filter to extract their first element. The cutoff frequency of these filters is $\omega_f = \omega/\sqrt{2}$. In Eqs. 22 to 24, v_{dq-} ,$v_{d-\_\text{decoupled}}$ and $v_{d+\_\text{decoupled}}$ are also shown. These equations are the result of negative turn of the dq axis (Rodriguez et al. 2007).

$$\begin{aligned} v_{dq-} = {} & v^{-}\begin{bmatrix} \cos(\varphi_{-1}) \\ \sin(\varphi_{-1}) \end{bmatrix} + v^{+}\cos(\varphi_{+1})\begin{bmatrix} \cos(2\omega_s t) \\ \sin(2\omega_s t) \end{bmatrix} \\ & + v^{+}\sin(\varphi_{+1})\begin{bmatrix} -\sin(2\omega_s t) \\ \cos(2\omega_s t) \end{bmatrix} \end{aligned} \tag{22}$$

$$v_{d-\_\text{decoupled}} = v^{-}\cos(\varphi_{-1}) = v_{d-} + \underset{d+}{\bar{v}}\cos(2\omega_s t) + \underset{q+}{\bar{v}}\sin(2\omega_s t) \tag{23}$$

$$v_{q-\_\text{decoupled}} = v^{-}\sin(\varphi_{+1}) = v_{q-} - \underset{d+}{\bar{v}}\sin(2\omega_s t) - \underset{q+}{\bar{v}}\cos(2\omega_s t) \tag{24}$$

In Eqs. 23 and 24, considering the second and third elements, it can be seen that their amplitudes are equal to the first elements of Eqs. 20 and 21. According to this fact, the second and third elements in each loop are obtained by multiplying their amplitude by sine and cosine with the frequency $2\omega_s t$, and then these elements are subtracted from v_{dq+}, v_{dq-}.In Fig. 3, decupling block for positive sequence is shown.

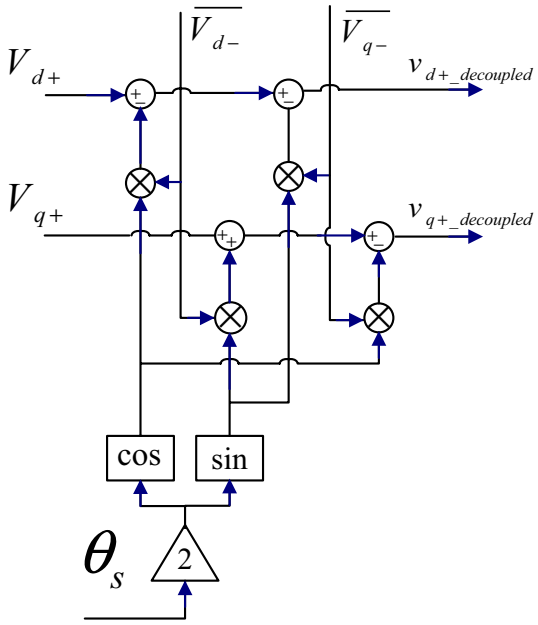


Fig. 3 Decoupling block for canceling the effect of v_- on the dq_+ frame signals

As a result, the effect of asymmetry in the three-phase input voltage is eliminated. In Eqs. 20, 21, 23 and 24, outputs of the decoupling block are shown. Finally, v_{q+} entered to the SRF-PLL and the output frequency is calculated. As a result, the effect of asymmetry in input voltage is eliminated and there will be no destructive effects in the output. In Fig. 4, the three-phase asymmetric voltage is applied to the PLL input, and the output of the PLL block is shown in Figs. 5 and 6. Obviously, the electrical angle at the output has been calculated accurately despite an imbalance in the grid voltage.

DDSRF-PLL shows weak behavior against the elimination of grid harmonics. In the next sections, this issue will be reviewed. These harmonics appear in a different order, and the PI block, in spite of the behavior of a low-pass filter, partially undermines the effects of these harmonics. But if the range of harmonics and their number are high, its effects on θ output and also the tracked frequency will be very devastating. In this article, this type of PLL has been expanded and becomes more resistant to the three-phase input voltage.

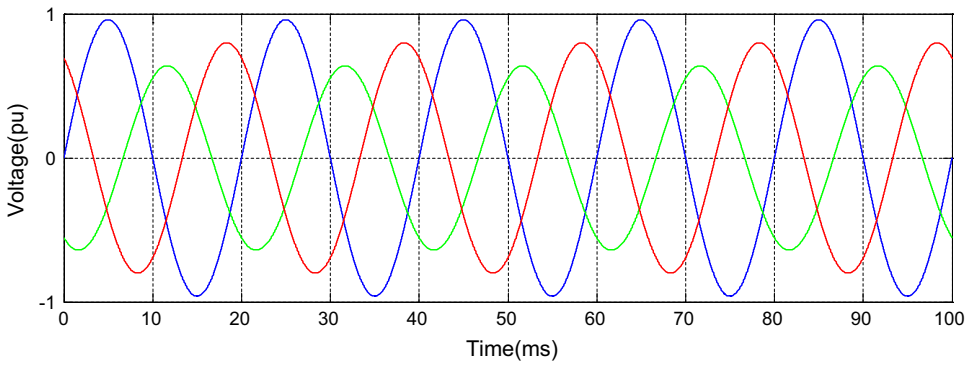


Fig. 4 Grid voltage in the unbalanced condition

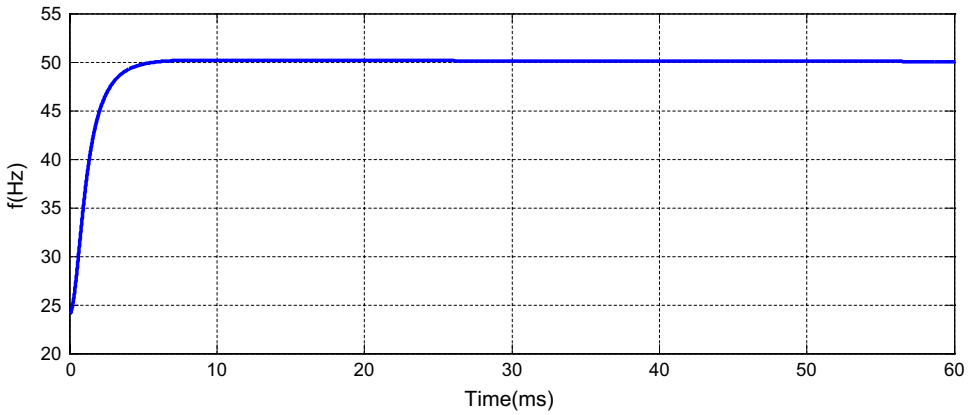


Fig. 5 Frequency tracked by the DDSRF-PLL

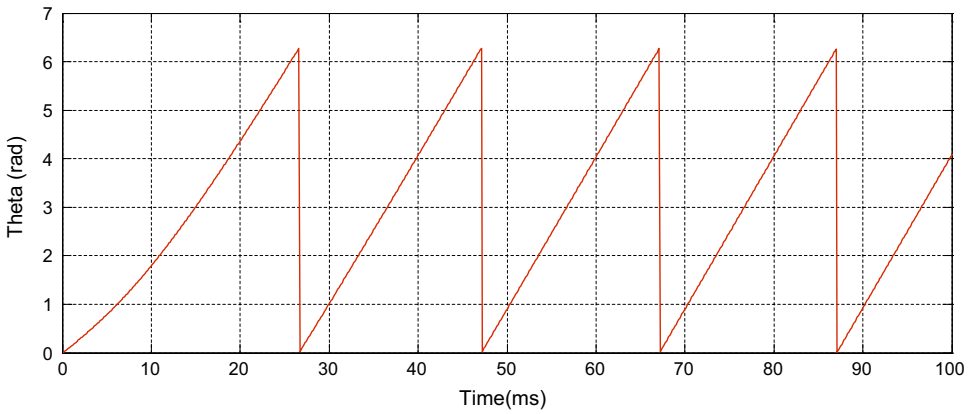


Fig. 6 θ_s, the output of DDSRF-PLL under grid voltage unbalance

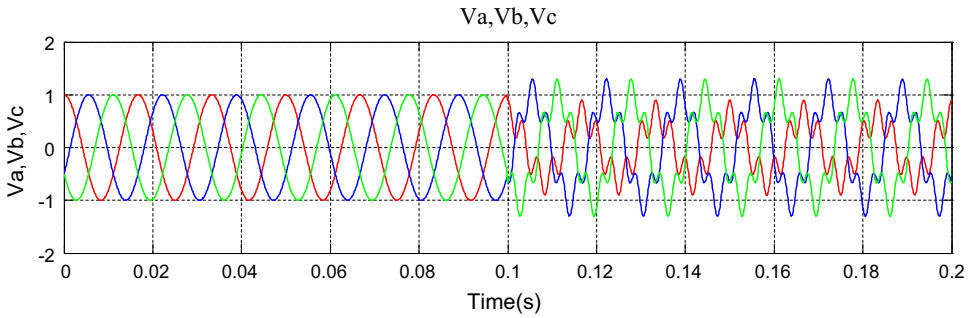


Fig. 7 Grid voltage when both unbalance and fifth harmonics are added in 0.1 s

3 Expanded DDSRF-PLL with Simultaneous Imbalance and Harmonics in the Input Signal

The problem with using DDSRF-PLL appears when the grid voltage has harmonics. These harmonics appear with different orders in $dq+$ and $dq-$. The PI block, due to the behavior of a low-pass filter, slightly undermines the effects of these harmonics. However, if there are a high number of harmonics with high amplitude, their effects in the theta output and frequency will be destructive. The mathematical equations of the harmonic effects are shown as follows:

$$v = v^{+}\begin{bmatrix}\cos(\omega t)\\ \cos(\omega t-2\pi/3)\\ \cos(\omega t-4\pi/3)\end{bmatrix} + v^{+n}\begin{bmatrix}\cos(n\omega t)\\ \cos(n\omega t-2\pi/3)\\ \cos(n\omega t-4\pi/3)\end{bmatrix} + v^{-}\begin{bmatrix}\cos(\omega_s t)\\ \cos(\omega_s t-4\pi/3)\\ \cos(\omega_s t-2\pi/3)\end{bmatrix} + v^{-n}\begin{bmatrix}\cos(n\omega_s t)\\ \cos(n\omega_s t-4\pi/3)\\ \cos(n\omega_s t-2\pi/3)\end{bmatrix} \tag{25}$$

$$\begin{aligned} v_{dq+} = {} & v^{+}\begin{bmatrix}\cos(\varphi_{+1})\\ \sin(\varphi_{+1})\end{bmatrix} + v^{+n}\begin{bmatrix}\cos((n-1)\omega t+\varphi_{+n})\\ \sin((n-1)\omega t+\varphi_{+n})\end{bmatrix} + v^{-}\cos(\varphi_{-1})\begin{bmatrix}\cos(2\omega_s t)\\ -\sin(2\omega_s t)\end{bmatrix} + v^{-}\sin(\varphi_{-1})\begin{bmatrix}\sin(2\omega_s t)\\ \cos(2\omega_s t)\end{bmatrix} \\ & + v^{-n}\cos((n-1)\omega t+\varphi_{-n})\begin{bmatrix}\cos((n+1)\omega t)\\ -\sin((n+1)\omega t)\end{bmatrix} + v^{-n}\cos((n-1)\omega_s t+\varphi_{-n})\begin{bmatrix}\sin((n+1)\omega_s t)\\ \cos((n+1)\omega_s t)\end{bmatrix} \end{aligned} \tag{26}$$

where v^{+n} and v^{-n} are the amplitudes of the positive and negative sequences of harmonic amplitude and n is the order of harmonic. As is seen in Eq. 25, a harmonic with order n is applied to the input voltage of PLL, and it shows itself in the output of v_{dq+}, v_{dq-} as harmonics with orders $n+1$ and $n-1$. In DDSRF-PLL, only the components with phase $2\omega t$ will be eliminated, and these harmonics will remain. If the amplitudes of these harmonics are high, the PI block might not attenuate them sufficiently, and their negative effects will appear in the output. Figures 7 and 8 show the three-phase input voltage with harmonics and the PLL response, respectively. In order to see the effects of harmonics and disturbances in the system, it is assumed that from 0.1 s to the next, harmonics and disturbances were added to the system. Figure 9 shows its phase response. The simulation is performed in steady state, and φ_{+1}, φ_{-1} are considered zero.

As shown in Figs. 8 and 9, the effects of the harmonics appear in the PLL output. In the proposed design, in the

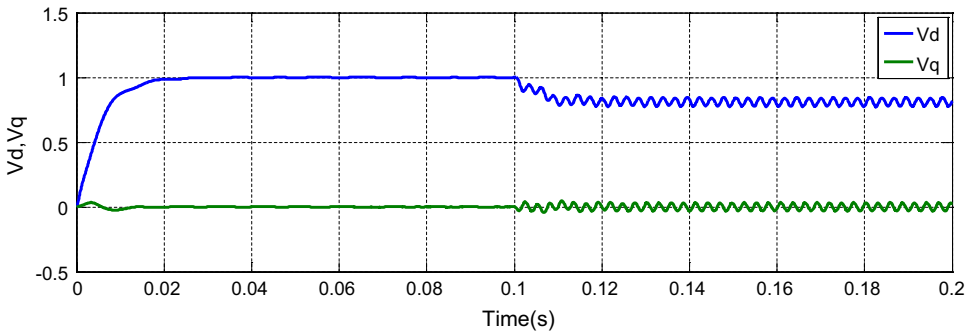


Fig. 8 V_d and V_q of DDSRF-PLL when both unbalance and harmonics are added in 0.1 s

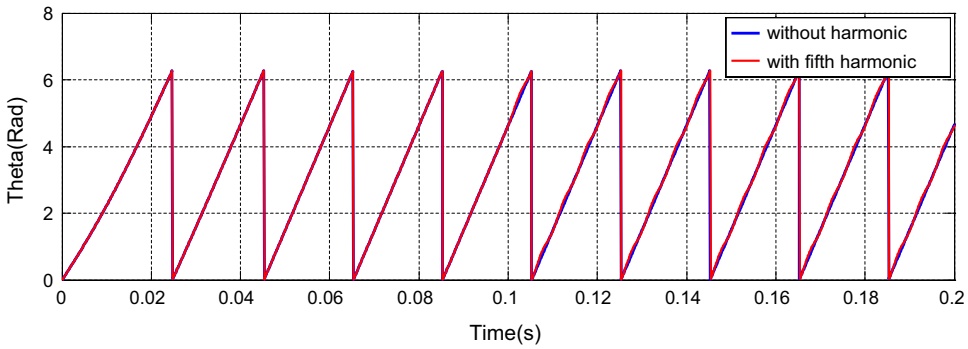


Fig. 9 Output electrical angle of DDSRF-PLL in the presence of fifth-order harmonics in the grid voltage in second 0.1 to the next. The red diagram is the expected value, and the blue diagram is the ideal value (Color figure online)

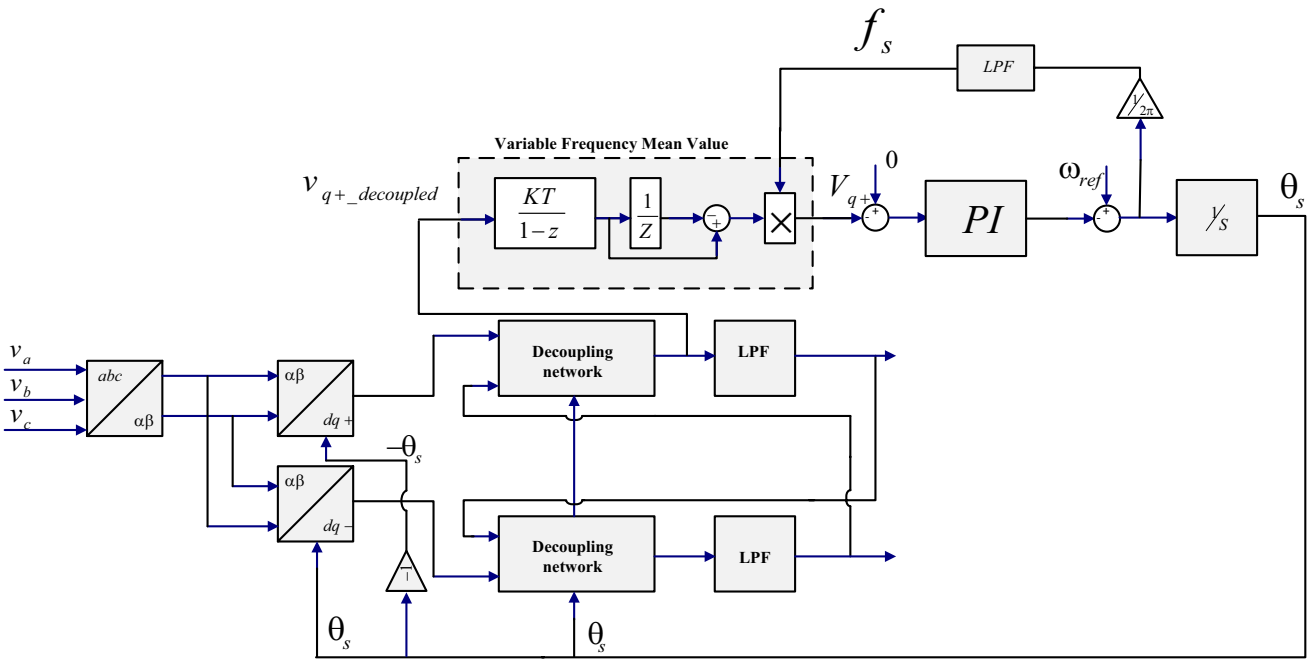


Fig. 10 Block diagram of the enhanced DDSRF-PLL

output of the positive decoupling block, a variable frequency mean value block is used in a cycle (Fig. 10). The mean variable frequency block computes the mean value of the signal. The mean value is computed over a running average window of one cycle of the period of the signal. This block uses a running average window. Therefore, one cycle of simulation must complete before the block outputs the computed mean value. As shown in Fig. 10, the inputs of the mean value block are the frequency calculated by the PLL and the output of the decoupling block. In this method, by integrating at a

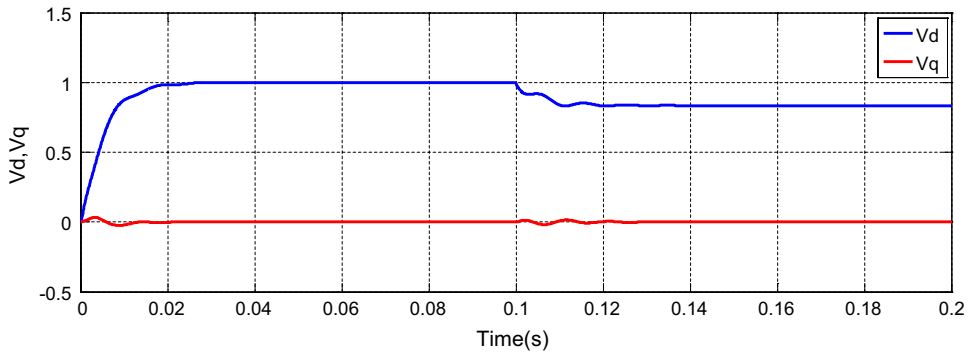


Fig. 11 V_d and V_q of the enhanced DDSRF-PLL. The harmonic distortions started only after 0.1 s

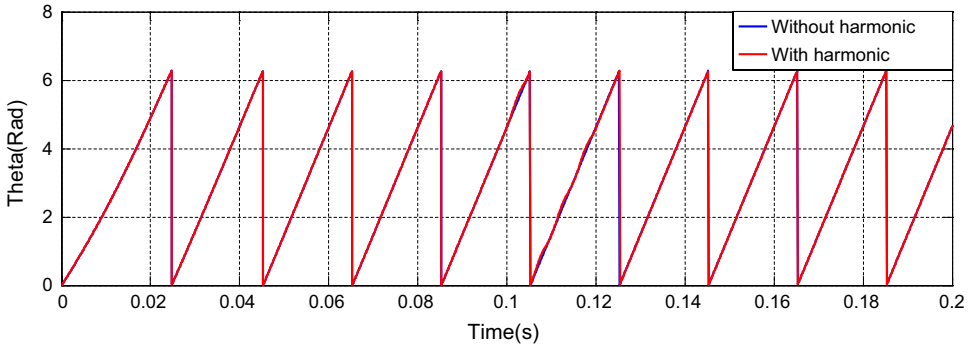


Fig. 12 Calculated electrical angle using enhanced DDSRF-PLL in the presence of fifth-harmonic in the input voltage. The red diagram is the expected value, and the blue diagram is the real value (Color figure online)

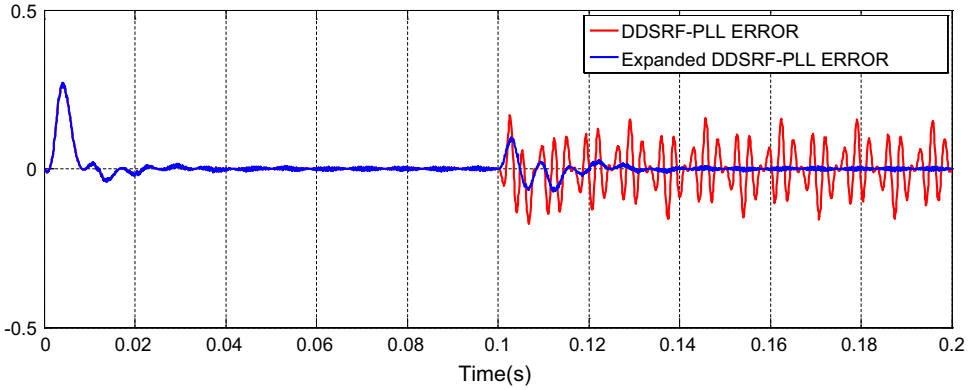


Fig. 13 Comparison of the ideal sine wave with which are generated by DDSRF-PLL and Expanded DDSRF-PLL. The harmonic distortions started only after 0.1 s

period of the input signal with the frequency calculated by the PLL, the signal values that do not have a frequency equal to the original signal are eliminated. With this method, the harmonics can be eliminated.

$$\text{Mean}(f(t)) = \frac{1}{T}\int_{t-T}^{t} f(t)\cdot \mathrm{d}t \tag{27}$$

where $f(t)$ is the input signal and T is the period of input signal equal to $1/f_s$.

In this case, using definite integration in a cycle with the main frequency of the input signal, all integer harmonics of the input signal will be definitely deleted, and their effects will not appear in the output. The output of this integrator block for the positive sequence is as follows:

$$V_{dq+} = V^{+1}\begin{bmatrix}\cos(\varphi_{+1})\\ \sin(\varphi_{+1})\end{bmatrix} \tag{28}$$

In this method, increasing the amplitude of unwanted harmonics has positive effect on performance of proposed PLL. Figures 11 and 12 show the output of this PLL assuming a harmonic input to the system. Figure 13 compares the ideal sine wave with which are generated by DDSRF-PLL and Expanded DDSRF-PLL.

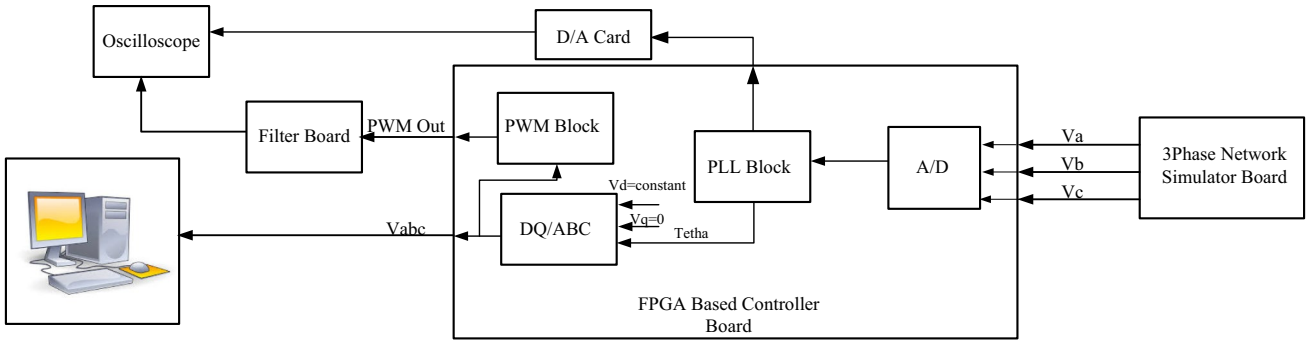


Fig. 14 Laboratory test bench block diagram for PLL examination

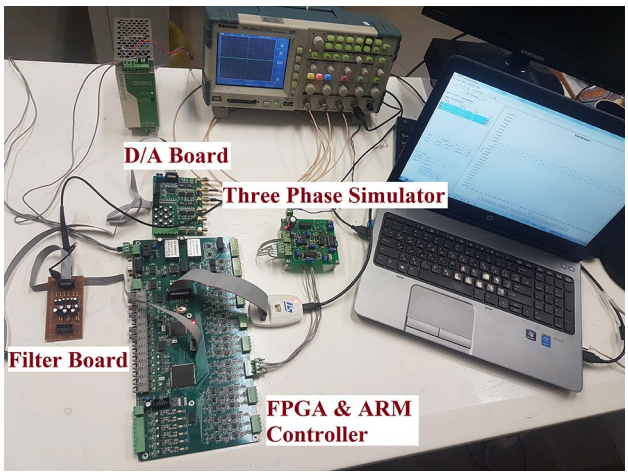


Fig. 15 Experimental setup

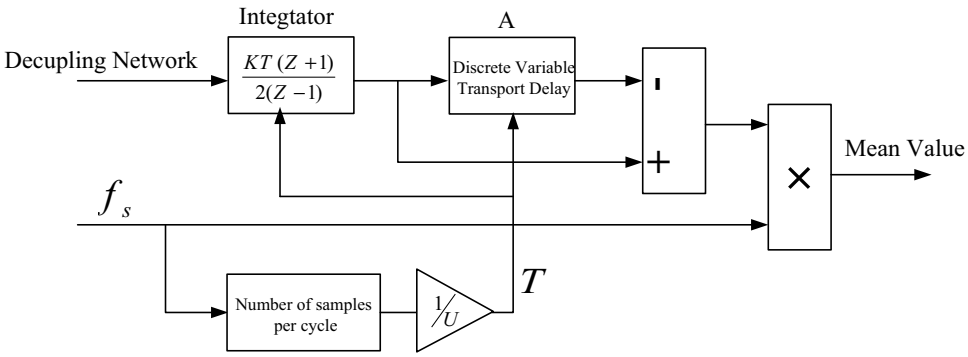
4 Experimental Results

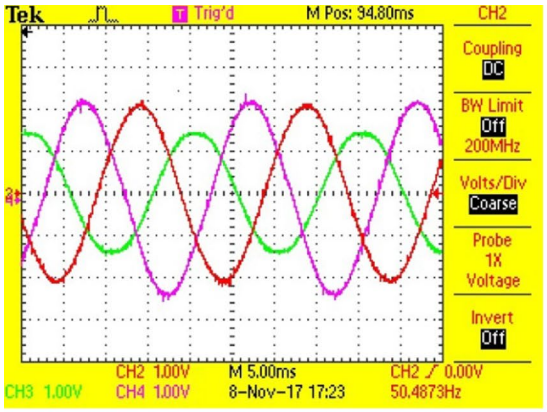
For extended PLL testing, a laboratory setup was used consisting of a three-phase simulation board with the ability to create disturbances and harmonics in three phases and a control board, which included an FPGA_Spartan3 processor and an ARM-Cortexm4 microcontroller. This board was designed to control a 100 KW DFIG system. The block diagram of the test bench is shown in Fig. 14. In this laboratory system, a digital-to-analog board was used to display output signals, so that signals such as d and q values could be seen in the scope (Fig. 15).

4.1 Implementation of Mean Value Block

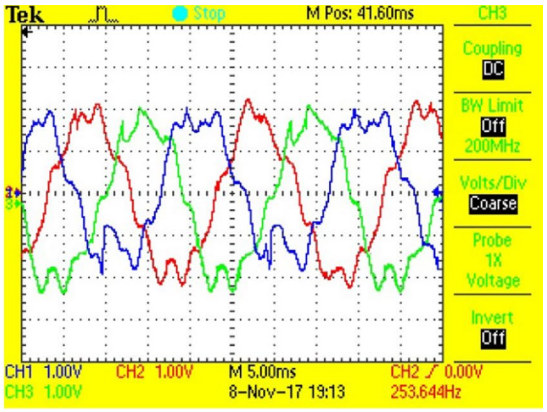
To implement the mean value block in the FPGA, the mean value block was applied in the MATLAB software, which after extracting its VHDL code was implemented onto hardware. Figure 16 presents the mean value block used in the Z domain with a sampling frequency of 10 kHz. As shown in Fig. 16, to obtain the period, the incoming frequency is sampled at the sampling frequency and then calculated. The block A is used to simulate the variable transport delay phenomenon. The variable transport delay can be used to simulate a variable time delay. At each simulation step, the block outputs the signal at the time that corresponds to the current simulation time minus the delay time. Best accuracy is achieved when the delay is larger than the simulation step size. f_s is the input signal frequency, and T is the period of signal.

Fig. 16 Mean value block

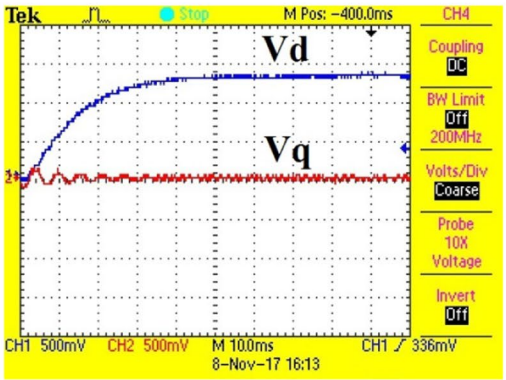




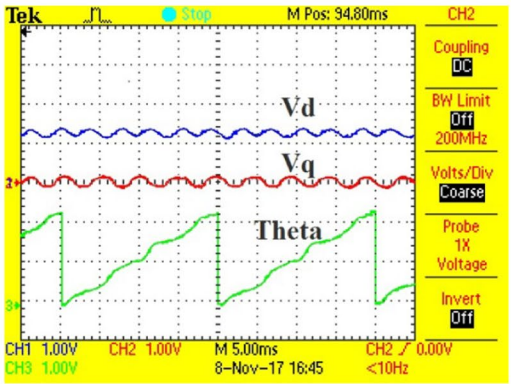
Grid voltage



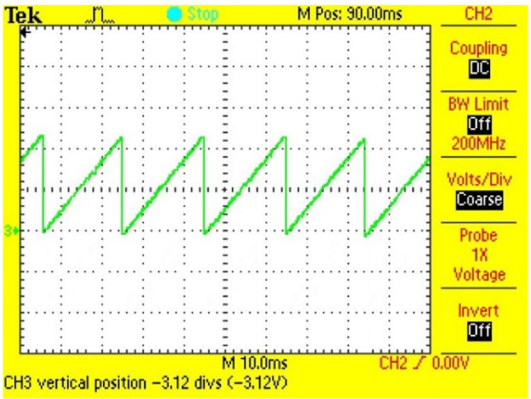
10% unbalanced in phase a and the presence of the third and fifth harmonics in all phases simultaneously



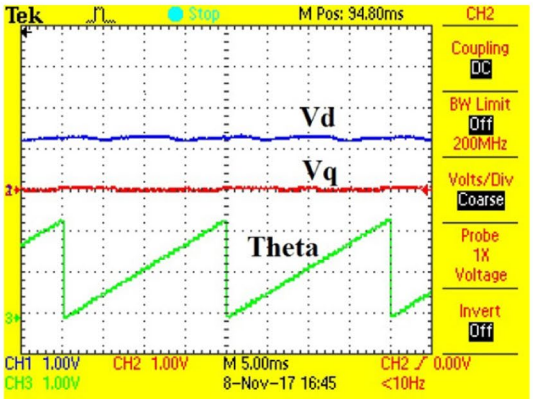
Vd and Vq of the enhanced DDSRF-PLL



Vd , Vq, and theta calculated by DDSRF-PLL



Theta of the enhanced DDSRF-PLL



Vd , Vq, and theta calculated by enhanced DDSRF-PLL

Fig. 17 Characteristic waveforms when **a** grid voltage is in unbalanced condition; **b** the utility voltage is distorted by existence of unbalance and harmonic

4.2 Implementation of LPF in FPGA

The transfer function of a typical low-pass filter is as follows:

$$\mathrm{LPF}(s) = \frac{w_f}{(s + w_f)} \tag{29}$$

In the analog domain and using the bilinear transform:

$$\mathrm{LPF}(z) = \frac{w_f}{2/T\frac{(z-1)}{(z+1)} + w_f} = \frac{\frac{w_f T}{(2+Tw_f)}(z+1)}{z + \frac{(w_f T-2)}{(w_f T+2)}} = \frac{k_1(z+1)}{(z+k_2)} \tag{30}$$

where T is the sampling period and its value is $T = 1/(100\ \text{kHz}) = 0.00001$; and for the steady response of PLL, the value of W_f was considered to be $\omega/\sqrt{2}$. As a result, the values k_1, k_2 were obtained as follows.

$$k_1 = 0.007232,\ k_2 = -0.88356$$

To evaluate the PLL function, after the PLL algorithm performed the calculation of the three-phase input angle, the result was given to a block in the FPGA, whose inputs were V_d and V_q in addition to the calculated angle, which were considered constant. The task of this block was the inverse transform of Park and Clark. The output of the desired block is a three-phase sinusoid. This three-phase sinusoid was given as a reference to the SVM block. The SVM and PWM block outputs were applied to the rotor side converter switches. This PWM was filtered and observed using a low-pass filter. The three phases generated by this method were compared with the three input phases, and the results indicated that the PLL well weakens the harmonics and input disturbances and they have no effect on the signal produced. The results of the experiment in Fig. 17 showed that the extended PLL operated correctly in conditions where the three inputs phases were harmonic and also disturbed, and a three phase was created without disturbances.

4.3 Comparison of Results

In Fig. 17, the results of the investigation of DDSRF-PLL and extended PLL have been presented in this article. The figure shows that when the grid voltage suffers from an imbalance in addition to the third and fifth harmonics, the extended PLL function is better. This issue can be seen at an angle and V_q, calculated by both PLLs in these circumstances. Also, a comparison of the results showed that the transient response of the extended PLL was with fewer deviation of fundamental frequency, the high stability margin. The sensitivity to the voltage amplitude has been reduced and had better performance than DDSRF-PLL in eliminating the harmonics. At the same time, calculations of this type of PLL have become relatively more complicated than the PLLs examined.

5 Conclusion

In this research, to prevent the negative effects of voltage imbalance and harmonics on the control process, expanded DDSRF-PLL was used to calculate the electrical angle. It is shown that under the existence of imbalance and harmonics in the grid voltage, the electrical angle of the grid voltage is calculated correctly. Compared to DDSRF-PLL, the transient response of the extended PLL was with fewer deviation of fundamental frequency. Features of this PLL are the high stability margin and the proper ability to eliminate harmonics. In this PLL, the sensitivity to the voltage amplitude has been reduced. Simulations together with a complete experimental evaluation were presented in order to verify the excellent results obtained by the proposed PLL. The next goal of this paper tests this controller on a 100-KW wind turbine test bench. This system is currently under preparation, and the results of practical tests will be published in the next article.

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