

## Research article

Min Zhang<sup>a</sup>, Zehui Fan<sup>a</sup>, Xixi Jiang, Hao Zhu<sup>\*</sup>, Lin Chen<sup>\*</sup>, Yidong Xia<sup>\*</sup>, Jiang Yin, Xinke Liu, Qingqing Sun and David Wei Zhang

# MoS<sub>2</sub>-based Charge-trapping synaptic device with electrical and optical modulated conductance

<https://doi.org/10.1515/nanoph-2019-0548>

Received December 25, 2019; revised January 31, 2020; accepted January 31, 2020

**Abstract:** The synapse is one of the fundamental elements in human brain performing functions such as learning, memorizing, and visual processing. The implementation of synaptic devices to realize neuromorphic computing and sensing tasks is a key step to artificial intelligence, which, however, has been bottlenecked by the complex circuitry and device integration. We report a high-performance charge-trapping memory synaptic device based on two-dimensional (2D) MoS<sub>2</sub> and high-k Ta<sub>2</sub>O<sub>5</sub>-TiO<sub>2</sub> (TTO) composite to build efficient and reliable neuromorphic system, which can be modulated by both electrical and optical stimuli. Significant and essential synaptic behaviors including short-term plasticity, long-term potentiation, and long-term depression have been emulated. Such excellent synaptic behaviors originated from the good nonvolatile memory performance due to the high density of defect states in the engineered TTO composite. The 2D synaptic device also exhibits effective switching

by incident light tuning, which further enables pattern recognition with accuracy rate reaching 100%. Such experimental demonstration paves a robust way toward a multitask neuromorphic system and opens up potential applications in future artificial intelligence and sensing technology.

**Keywords:** MoS<sub>2</sub>; composite dielectric; nonvolatile memory; synaptic device; ANN.

The rapidly evolving computing science and technology have urged more unexploited data processing modes to be fast tracked for the development and deployment in the field of artificial intelligence [1–4]. Traditional computing systems based on von Neumann architecture have lost the edge and become inefficient when dealing with increasingly complex problems such as speech, image, and video data processing, which often need huge physical resources and enormous energy consumption [5–7]. On the other hand, the human brain, which consists of a highly interconnected and massively parallel network, is an efficient information processing and storage system [8]. The 10<sup>11</sup> neurons in the brain are responsible for the cognition and calculation, and the 10<sup>15</sup> synapses are the critical units in signal delivery and processing [9, 10]. Synaptic behaviors including short-term plasticity (STP), long-term potentiation (LTP), and long-term depression (LTD) function in the biological brain for memory and actions, and the human learning behaviors are achieved by modulating the weight of synapse through spike controlling. Therefore, great efforts have been made to realize an artificial brain-like network based on the biological synaptic plasticity to process tremendous data in various forms with faster speed and lower power consumption [11].

So far, different prototypes of synaptic devices have been developed emulating synaptic dynamics toward the implementation of brain-like computing and data processing systems, such as conductive bridging (CBRAM) [12–14], resistive change memory [15, 16], and phase change memory [17, 18]. Most of the reported synaptic devices are based on passive and two-terminal structures similar to

<sup>a</sup>**Min Zhang and Zehui Fan:** These authors contributed equally to this work.

**\*Corresponding author: Hao Zhu and Lin Chen,** State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University, Shanghai 200433, China, e-mail: hao\_zhu@fudan.edu.cn (H. Zhu); linchen@fudan.edu.cn (L. Chen). <https://orcid.org/0000-0002-7145-7564> (L. Chen); and **Yidong Xia,** College of Engineering and Applied Science, Nanjing University, Nanjing, 210093, China, e-mail: xiayd@nju.edu.cn

**Min Zhang:** State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University, Shanghai 200433, China; and School of Mathematics, Physics and Information Engineering, Jiaxing University, Jiaxing 314001, China

**Zehui Fan, Xixi Jiang, Qingqing Sun and David Wei Zhang:** State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University, Shanghai 200433, China

**Jiang Yin:** College of Engineering and Applied Science, Nanjing University, Nanjing, 210093, China

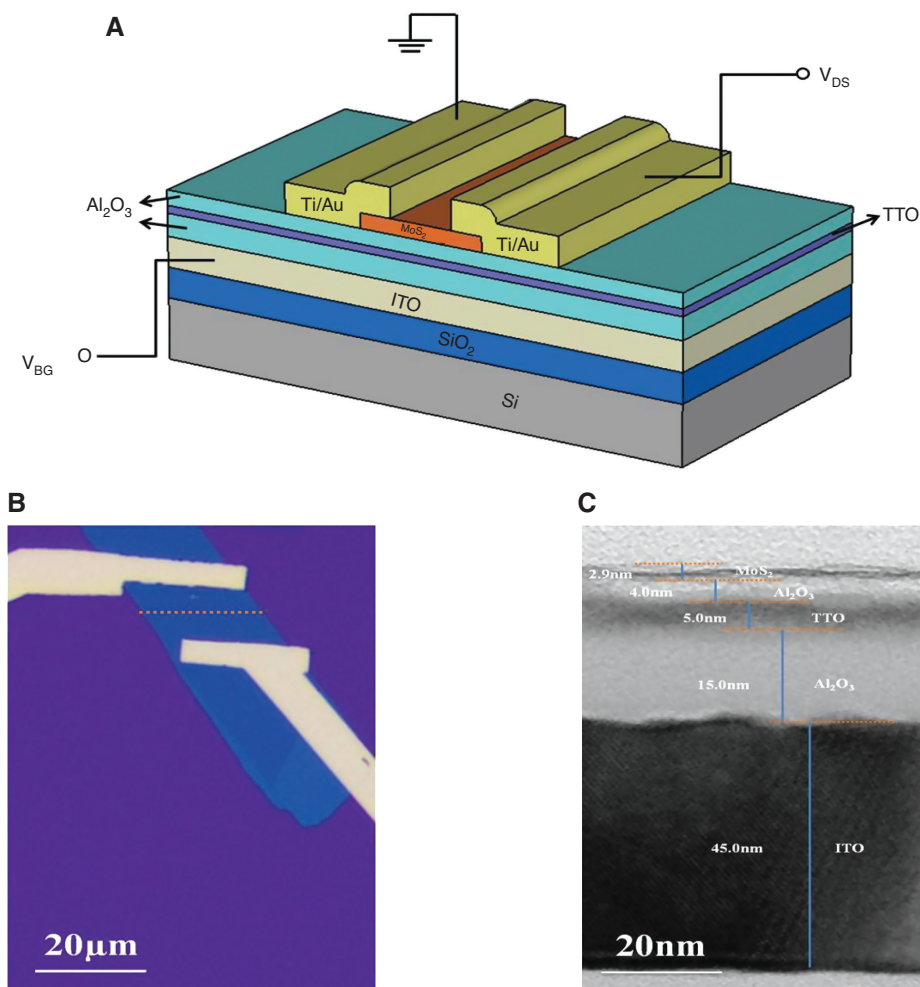
**Xinke Liu:** College of Materials Science and Engineering, Shenzhen University, Shenzhen 518060, China. <https://orcid.org/0000-0002-3472-5945>

that of resistive random access memory (RRAM) due to the difficulty in obtaining multiple and distinguished conductive states in transistor-based architecture [19]. In addition, conventional semiconductors or functional films in the synaptic devices are designed and engineered to perform limited functions. Nevertheless, this has become increasingly incapable of fulfilling multitask with the development of various portable electronic devices such as image/video process and object detection. Therefore, the integration of functional materials with features such as optoelectronic properties as the active component in synaptic device is very attractive because it will leverage the advantages afforded by the new materials with the vast infrastructure of the synaptic electronics.

As a stable and repeatable physical mechanism, charge trapping has been widely applied in building non-volatile memory devices with good data retention. Such memory is based on the trapping and detrapping of electrons/holes in the charge storage medium changing the switching threshold. The charge-trapping memory (CTM) in field-effect transistor (FET)-like three-terminal architecture has also been used in realizing artificial synapses as the amount of trapped charges can be effectively controlled through the operation voltage and device structure engineering to avoid the blurring between conductive states. But in terms of programming speed, conventional charge-trapping synaptic devices are largely limited by the trapping/releasing process of the charges because of the low trapping efficiency and unsuitable band offsets with respect to Si in traditional nitride or oxide films. Exploration focusing on the optimization of trapping mechanism and the engineering of the dielectric stack is critical to improve the trapping efficiency and operation speed while maintaining good reliability. An additional and effective strategy to achieve miniaturized yet performance-enhanced memory is to utilize atomically thin two-dimensional (2D) semiconductors as the active channel, which have been widely used in various fields [20–23]. Two-dimensional materials such as bilayer graphene, anisotropic black phosphorus (BP), and transition metal dichalcogenides (TMDs) have been integrated in FET-based synaptic devices with reinforced gate control and suppressed short-channel effects [24–27]. Tian et al. [28] reported a highly compact BP-based synaptic transistor emulating a biological axon–multisynapse network with connection heterogeneity to demonstrate an artificial anisotropic axon–multisynapse network. Liu et al. [29] reported a quasi-nonvolatile memory based on 2D materials with greatly enhanced writing speed, which is approximately  $10^6$  times faster than other memories. However, a crucial issue lies in the design and processing of the

dielectric/2D material interface, where a large number of defects and traps may exist because of the absence of dangling bonds on most layered semiconductors. This can significantly deteriorate the switching capabilities and the control over the charge-trapping process. Here, we report the fabrication and characterization of an artificial synapse based on the flash-like CTM device using 2D MoS<sub>2</sub>, a typical TMD semiconductor as the channel and (Ta<sub>2</sub>O<sub>5</sub>)<sub>x</sub>(TiO<sub>2</sub>)<sub>1-x</sub> composite charge-trapping dielectric. Back-gate FET geometry with engineered gate stack ensures sufficient optical contrast for the identification of MoS<sub>2</sub> flakes with least dielectric/MoS<sub>2</sub> interface traps. Different from the limited trapping sites with various energy levels in conventional single-material charge-trapping layer, the high density of defect states formed due to the interdiffusion between the two kinds of high-k oxides of Ta<sub>2</sub>O<sub>5</sub> and TiO<sub>2</sub> is responsible for the charge storage. Charge-trapping efficiency, programming/erasing speed, and retention capability have been greatly improved because of the PBCB (potentials at the bottom of conduction band) between MoS<sub>2</sub> and high-k composite. This provides a solid basis for the plasticity study in which the STP, LTP, and LTD behaviors have been successfully emulated. A near-perfect recognition rate has been achieved in the artificial neural network (ANN) built in this work. Furthermore, 2D materials are photosensitive [30–33] and have been explored in many optoelectronic applications [34–36]. Thus, synaptic functions have been effectively modulated by a series of optical operations owing to the robust optoelectronic properties in MoS<sub>2</sub> and the engineered dielectric stack. Such control and tuning of the memory performance and synaptic behaviors pave attractive ways toward the design of new synaptic devices for future neuromorphic computing and advanced sensing applications.

The structure of the back-gate MoS<sub>2</sub> synaptic FET is schematically shown in Figure 1A. The ultrathin MoS<sub>2</sub> channel is mechanically exfoliated from bulk and transferred to the top surface of the back-gate stack. In the most reported experimental work on MoS<sub>2</sub> transistors, the exfoliated 2D flakes are generally transferred onto the relatively thick (~300 nm) SiO<sub>2</sub> surface to gain sufficient contrast for the optical identification of the location, thickness, and lateral size of the flakes. However, such a thick dielectric layer will inevitably degrade the gate control over the channel and require a much higher operation voltage level. Alternatively, we employed an engineered Al<sub>2</sub>O<sub>3</sub>/(Ta<sub>2</sub>O<sub>5</sub>)<sub>x</sub>(TiO<sub>2</sub>)<sub>1-x</sub> (TTO)/Al<sub>2</sub>O<sub>3</sub>/indium tin oxide (ITO)/SiO<sub>2</sub>/Si stack in which the ITO works as the back-gate electrode with Al<sub>2</sub>O<sub>3</sub>/TTO/Al<sub>2</sub>O<sub>3</sub> gate dielectric (see Methods for experimental details). Such engineered back-gate stack



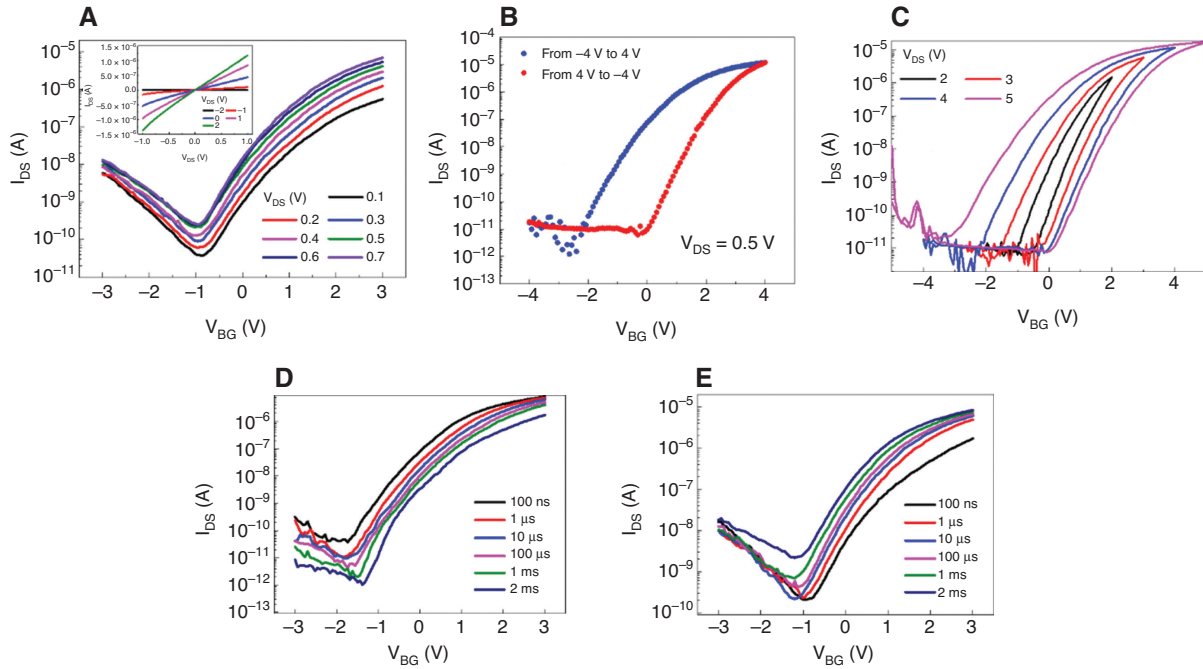
**Figure 1:** Schematic and morphological structure of a MoS<sub>2</sub> CTM device.

(A) Schematic illustration of a MoS<sub>2</sub> CTM device based on a back-gate FET structure. (B) Optical image of the MoS<sub>2</sub> flake on surface of the dielectric stack with Ti/Au source/drain electrodes. The dotted line indicates the cut location in TEM test. (C) Cross-sectional TEM image of the device showing layers of 45-nm ITO, 15-nm Al<sub>2</sub>O<sub>3</sub>, 5-nm TTO, 4-nm Al<sub>2</sub>O<sub>3</sub>, and 2.9-nm MoS<sub>2</sub>. The image was obtained along the cut line shown in (C).

can enable similar optical contrast as that on the 300-nm SiO<sub>2</sub>/Si substrate while significantly enhancing the gate control over the channel because of the thinner dielectric layers. The 4-nm Al<sub>2</sub>O<sub>3</sub>, 5-nm TTO, and 15-nm Al<sub>2</sub>O<sub>3</sub> function as the tunneling layer, charge-trapping layer, and blocking layer, respectively. Figure 1B shows the exfoliated MoS<sub>2</sub> flakes on the top surface of the engineered stack. Good optical contrast between the ultrathin flake and the substrate with clear MoS<sub>2</sub> edges has been achieved. From the cross-sectional transmission electron microscopy (TEM) image shown in Figure 1C, the gate stack has been successfully prepared with sharp interfaces between the MoS<sub>2</sub> and the dielectric layers. The thickness of the MoS<sub>2</sub> flake is ~2.9 nm corresponding to a 4-layer film. As mentioned above, as the MoS<sub>2</sub> channel region is prepared after the formation of gate stack, no dielectric deposition on the

MoS<sub>2</sub> surface is involved, which is favorable to minimize the negative effects originated from the MoS<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> interface traps.

We first measured the current–voltage characteristics of the memory device. As shown in Figure 2A, n-type field-effect behaviors with clear on-state and off-state currents have been observed from the  $I_{DS}$ – $V_{BG}$  transfer curves ( $I_{DS}$  and  $V_{BG}$  refer to the drain-source current and back-gate voltage, respectively). Large on/off current ratio greater than 10<sup>5</sup> has been achieved, which suggests that the interface traps introduced during the fabrication and flake transfer process are very limited as these positively charged traps can easily induce more electrons in the channel, decreasing the on/off ratio. The inset of Figure 2A shows the  $I_{DS}$ – $V_{DS}$  ( $V_{DS}$ : drain-source voltage) curves of the MoS<sub>2</sub> CTM device with  $V_{DS}$  swept from –1 to 1 V. The linear



**Figure 2:** I–V characteristics of the MoS<sub>2</sub> CTM device.

(A) Transfer characteristics of the MoS<sub>2</sub> transistor.  $I_{DS}$  as a function of  $V_{BG}$  with  $V_{DS}$  varying from 0.1 to 0.7 V with 0.1-V step. Inset:  $I_{DS}$  vs.  $V_{DS}$  curves of the device with  $V_{DS}$  swept from -1 to +1 V. (B)  $I_{DS}$ – $V_{BG}$  hysteresis curves of the MoS<sub>2</sub> CTM device under -4 V to +4 V  $V_{BG}$  sweeping range showing sufficiently large memory window. (C)  $I_{DS}$ – $V_{BG}$  hysteresis curves of the MoS<sub>2</sub> CTM device in different  $V_{BG}$  sweeping range of  $\pm 2$ ,  $\pm 3$ ,  $\pm 4$ , and  $\pm 5$  V, respectively. (D) Programming operations on the MoS<sub>2</sub> CTM device in different programming time at +4 V gate voltage pulse. (E) Erasing operations on the MoS<sub>2</sub> CTM device in different erasing time at -4 V gate voltage pulse.

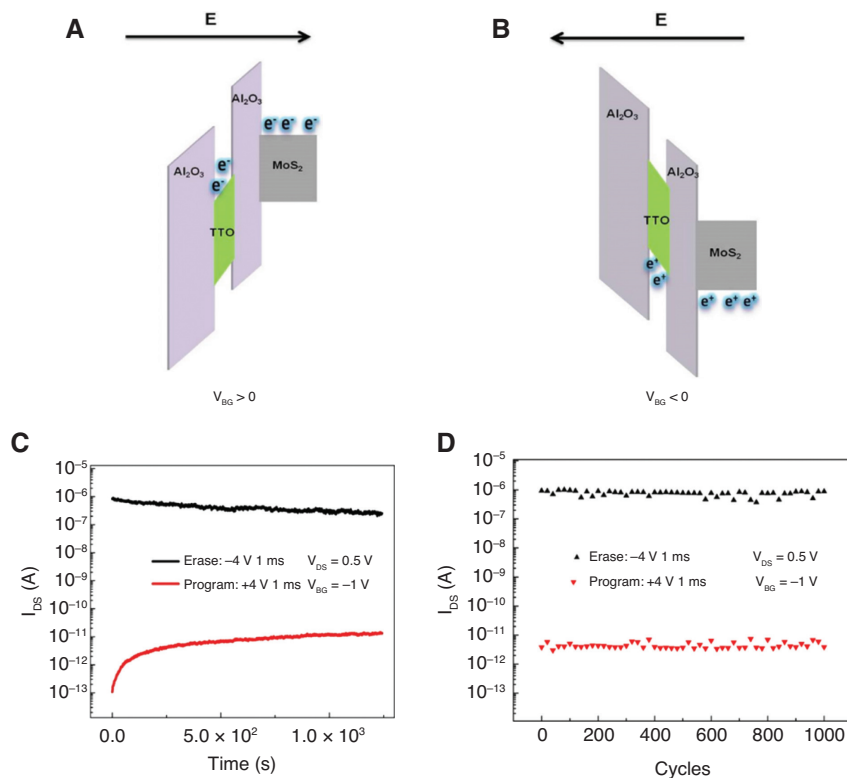
dependence of  $I_{DS}$  on  $V_{DS}$  indicates negligible contact resistance at the source/drain electrodes without significant charge injection barrier. This will enhance the drive capability of the device with higher on-state current.

A stable and sufficient memory window is a prerequisite for a memory device to obtain distinct and repeatable multiple storage states as the basis for the synaptic functions in a neuromorphic system. Figure 2B shows the  $I_{DS}$ – $V_{BG}$  hysteresis curves by sweeping  $V_{BG}$  between -4 and 4 V. Clear clockwise hysteresis loops have been observed, suggesting the charge-trapping mechanism in the TTO layer. The memory is as large as 2 V, which is sufficient for effective multilevel storage applications. Such a high charge-trapping efficiency is ascribed to the high density of the trap states originated from the electron redistribution between the cations with different valence and anion (oxygen) due to the appearance of the dangling bonds formed at the surface of each high-k oxide in the TTO layer [36]. Furthermore, by changing the  $V_{BG}$  sweep range, the charge-trapped states in the device can be effectively tuned and modulated (Figure 2C).

The programming and erasing operations of the MoS<sub>2</sub> CTM device can be understood through the band diagrams shown in Figure 3A and B, respectively. When

a positive  $V_{BG}$  is applied, the electrons tunnel through the 4-nm-thick Al<sub>2</sub>O<sub>3</sub> barrier following the conventional Fowler–Nordheim tunneling mechanism [37] and are trapped in TTO layer screening the back-gate electric field to reach the MoS<sub>2</sub> channel. Such programming operation will result in a shift in the threshold voltage toward positive direction (Figure 2D). When a negative  $V_{BG}$  is applied, on the contrary, electrons are tunneling back from the TTO layer to the MoS<sub>2</sub> channel, and holes tunnel through the Al<sub>2</sub>O<sub>3</sub> barrier and are trapped in the TTO layer at the same time, leading to a threshold shifting to the negative direction (erasing operation in Figure 2E). The different memory states of the MoS<sub>2</sub> device have been achieved by using both electrical and optical approaches. These results are in line with previous studies [33, 38]. The retention and endurance performance of the synaptic device are presented in Figure 3C and D. The device was programmed and erased by  $\pm 4$ -V gate voltage with 1-ms pulse width. The  $I_{DS}$  current level was measured with 0.5 V  $V_{DS}$  and -1 V  $V_{BG}$ . Good charge retention characteristics have been observed, with only a small degradation in memory window after 10<sup>4</sup>-s retention time, but the on/off ratio is still greater than 10<sup>4</sup>. Such good retention is due to the intrinsic charge storage property of the TTO trapping





**Figure 3:** Schematic band diagram and the reliability characterization of the MoS<sub>2</sub> CTM device.

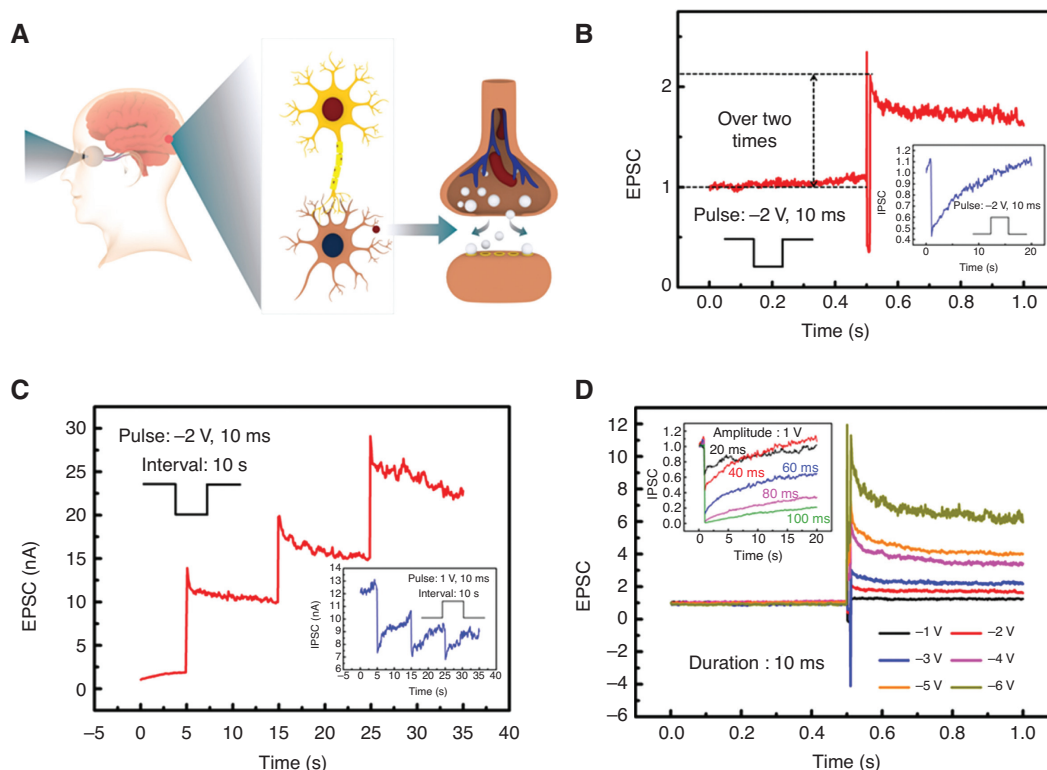
Schematic band diagram and charge transport of the MoS<sub>2</sub> CTM device in (A), programming ( $V_{BG} > 0$ ) and (B) erasing ( $V_{BG} < 0$ ) operations. (C) Retention characteristics of the MoS<sub>2</sub> CTM device with more than  $10^4$  on/off ratio after  $10^4$ -s retention time. (D) Endurance characteristics of the MoS<sub>2</sub> CTM device showing negligible degradation in memory window after  $10^3$  operation cycles.

layer, and it further supports the mechanism that the dominant charge storage locates in the TTO instead of the interface defects because the recovery process of the interface states is typically quite fast, leading to a poor retention. The endurance property of the MoS<sub>2</sub> memory is characterized by applying a sequence of programming/erasing pulses of  $\pm 4$  V, 1 ms. As demonstrated in Figure 3D, the device shows excellent endurance characteristics with negligible memory window degradation after 1000 programming/erasing cycles. Such good endurance property can significantly enhance the stability and the recognition rate of the synaptic device.

Based on the good memory performance exhibited from the TTO CTM device, we further investigated the synaptic characteristics of the memory device including synaptic responses such as STP, LTP, and LTD. It is known that neurons can be classified to axon and dendrite according to different morphology and function. As shown in Figure 4A, a synapse is a specialized structure of the cell membrane of a neuron, and each synapse is formed by presynaptic and postsynaptic structures. Presynaptic is usually the end of the axon of a neuron, whereas postsynaptic is usually located on the dendrite or cell body of a neuron. In our

artificial 2D MoS<sub>2</sub> synaptic device, the ITO back-gate is used as the presynaptic input terminal, and the 2D ultrathin MoS<sub>2</sub> channel with source/drain electrodes is functioning as the postsynaptic output terminal. Synapses connect neurons to themselves or other neurons and transmit information in the form of electrical or chemical signals. The action potential of synapse is generated by neuron impulse behavior, which is the basis of information flow, data processing, and memory in the human brain. When an action potential is transmitted to the end of the axon, a pulse will be emitted from the presynaptic membrane, and the membrane potential on the postsynaptic membrane will change accordingly. Based on the memory performance shown above, it can be expected that our MoS<sub>2</sub> synaptic device can well mimic this transmission process in the neural network.

As shown in Figure 4B, the excitatory synaptic responses to a negative input pulse ( $-2$ -V amplitude, 10-ms width) applied at the gate were observed.  $V_{DS}$  of 0.1 V was applied between the source and drain electrode for excitatory postsynaptic current (EPSC) measurement. The current of the MoS<sub>2</sub> channel increases significantly upon the application of a presynaptic spike and then falls to a steady value. The peak value of EPSC is more than twice



**Figure 4:** Synaptic performance of the MoS<sub>2</sub> device.

(A) Schematic of the human optic nerve system and a biological synapse. (B) The EPSC triggered by the input pulse (-2 V, 10 ms). Inset: the IPSC triggered by a presynaptic spike (2 V, 10 ms). (C) EPSC triggered by three consecutive input pulses (an amplitude of -2 V, a duration of 10 ms, and an interval of 10 s). Inset: IPSC triggered by three consecutive input pulses (an amplitude of 1 V, a duration of 10 ms, and an interval of 10 s). (D) EPSC triggered by six individual pulses with 10-ms pulse width, but with amplitudes varying from -1 to -6 V in 1 V step. Inset: IPSC triggered by six individual pulses with 1-V amplitude but with pulse width changing from 20 to 100 ms in 20-ms steps.

the initial value, and the steady value is significantly higher than the initial value. Clearly, the presynaptic spike triggered the MoS<sub>2</sub> device to a new conductance state. This demonstrates a typical LTP responsible for long-term memory and learning in biological synapse, and the significant change of the conductance state corresponds to the weight value adjustment in biological synapse, which is the basis for complex calculations and thinking. When the negative pulse is applied at the ITO back-gate, electrons from the trapped states in the TTO dielectric layer will gain enough energy to tunnel through the upper Al<sub>2</sub>O<sub>3</sub> dielectric layer into the channel, and the interface between MoS<sub>2</sub> film and Al<sub>2</sub>O<sub>3</sub> dielectric layer also releases a large number of electrons into the channel. These lead to the significant increase in the MoS<sub>2</sub> channel current. After the gate pulse is removed, some injected electrons are generally trapped by the interface between the MoS<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> dielectric layer. Other electrons that are released from the trap sites of the TTO layer are unable to gain enough energy to tunnel back [36]. So, the steady value is higher than the initial value. After applying a positive input pulse (2-V amplitude, 10-ms width) at the ITO back-gate, a typical

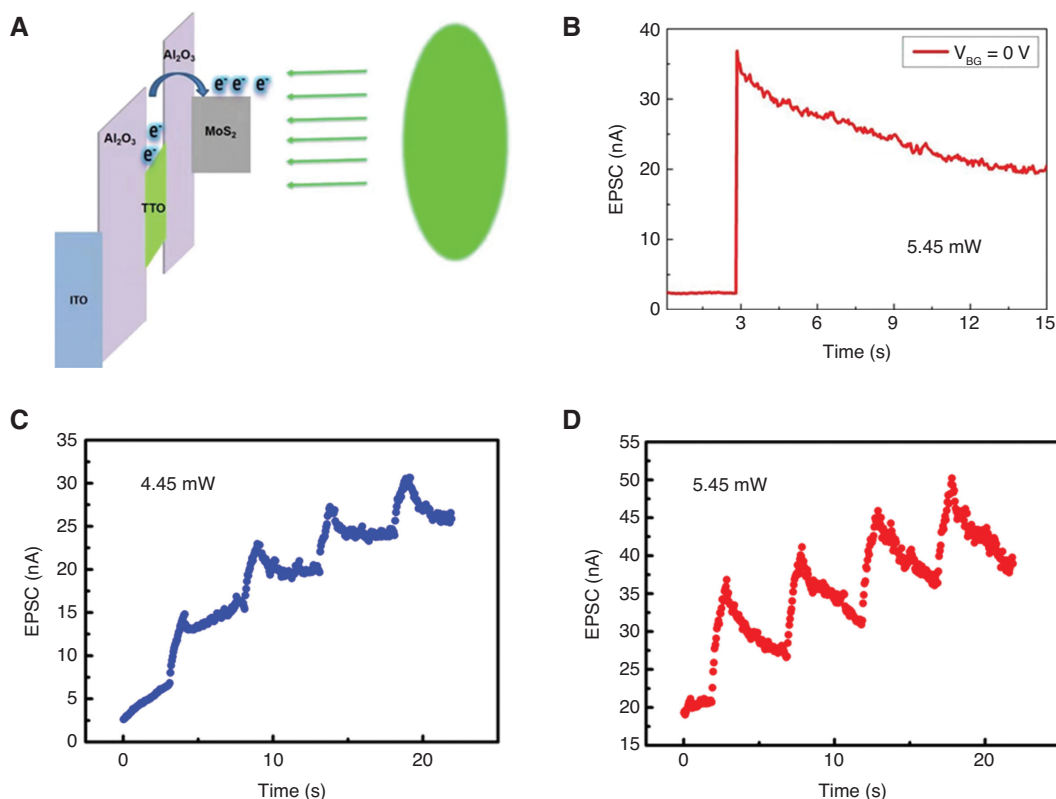
inhibitory postsynaptic current (IPSC) was detected, as shown in the inset of Figure 4B. The peak value of IPSC is approximately 0.4 times of the initial value, and it took approximately 20 s to fall back to the initial level. This phenomenon corresponds to the short-term depression in the biological synapse. When the positive pulse was applied, electrons from the MoS<sub>2</sub> channel tunneled through the upper Al<sub>2</sub>O<sub>3</sub> layer under the attraction of the electric field and were captured by the trap sites in the TTO layer. Thus, the current in the MoS<sub>2</sub> channel becomes lower.

When three negative pulses (-2-V amplitude, 10-ms duration, with 10-s interval) are applied to the ITO gate, as shown in Figure 4C, each presynaptic spike triggered the MoS<sub>2</sub> channel current to a higher level, and the current value can keep steady during the 10-s intervals. This means that each presynaptic spike effectively triggered our device to a different conductance state. The inset of Figure 4C displays current curve triggered by three positive pulses (1-V amplitude, 10-ms duration, with 10-s interval). We have also analyzed the influence of different voltage pulses amplitude and pulses time on the performance of individual synapses. Figure 4D shows EPSC characteristic

responses to different stimulus of six individual pulses with 10-ms width but with the amplitudes varying from  $-1$  to  $-6$  V in 1-V step. Note that the MoS<sub>2</sub> FET was always restored to its initial condition before applying the pulse sequence of a particular amplitude. This is to make a fair and error-free comparison between the changes in the channel current as a function of pulse amplitude. As a higher gate voltage pulse would trigger more electrons to release from the TTO charge-trapping layer and tunnel into the channel, a larger voltage amplitude will trigger a higher current level. This is consistent with the results shown in Figure 4D. After applying a  $-6$ -V gate voltage pulse, the ratio between the maximum current value and the initial value can reach up to 1200%. This is due to the engineered back-gate stack with much thinner gate dielectric enhancing the gate control even under a small voltage level. The inset of Figure 4D shows IPSC characteristic curves when applying six individual pulses with 1-V amplitude but with pulse width changing from 20 to 100 ms in 20-ms steps. It is clear that the IPSC changes greater with the increase of pulse width.

MoS<sub>2</sub> and other TMD semiconductors are attractive in optoelectronics because of their tunable band structure

and proper bandgap, which is promising in photodetection applications. The integration of the few-layer MoS<sub>2</sub> in the functional synaptic device as the active component is thus very intriguing to achieve a multitask purpose by realizing the conventional synaptic activities, as well as the photosensing function. In the measurement setup, the laser pulse with 520-nm wavelength works as the control gate modulating the carrier transport. During the experiment, we used laser with different wavelengths of 90, 450, and 520 nm. The performance of the device is more outstanding and stable under a 520-nm wavelength light source. Therefore, the results presented in the following obtained are obtained under optical stimulus with a 520-nm laser. The band diagram and transport of the electrons under the laser illumination are schematically shown in Figure 5A. Under light illumination, the photons excite the electrons to move from the valence band to the conduction band in the few-layer MoS<sub>2</sub> leaving holes in the valence band. The trapped electrons in the TTO layer will be de-trapped and released into the MoS<sub>2</sub> channel to recombine with the holes which further causes a change in the channel current, namely the PSC as shown in Figure 5B. The EPSC was triggered by a single laser pulse



**Figure 5:** Synaptic performance under laser illumination.

(A) Schematic band diagram under laser illumination. (B) EPSC triggered by single laser pulse (5.45 mW, 2 s). (C) EPSC triggered by four consecutive laser pulses (4.45 mW, 2 s, and an interval of 3 s). (D) EPSC triggered by four consecutive laser pulses (5.45 mW, 2 s, and an interval of 3 s).

with 2-s width and 5.45-mW power intensity. Similar to the performance obtained by electrical gating, continuous EPSC can be observed when applying consecutive laser pulses, as shown in Figure 5C and D. Each laser pulse triggered the MoS<sub>2</sub> channel current to a different level, and laser illumination with higher power intensity will trigger higher current. Table 1 lists and compares the typical performance of the recently reported TMD-based CTM devices and synapses incorporating high-k dielectrics or organics such as perylene-3,4,9,10-tetracarboxylic dianhydride (PTCDA) and Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS). Such photosensing capability and the optical modulation over the conduction states in the channel have paved a solid pathway for synaptic functions such as visual processing in future multi-functional neuromorphic systems.

Unlike many previous studies of synaptic devices, which focus only on the synaptic levels [40, 43, 44], we have built an ANN for face recognition after obtaining some effective and highly stable conductance states in order to demonstrate the feasibility of building large-scale neural network by using our 2D composite charge-trapping synaptic device. We have used the effective conductance values obtained under electrical (300 values) and optical (100 values) stimuli separately to substitute the weight values in the ANN to achieve the face recognition test. As shown in Figure 6A, the impulse response current continues to rise when applying 300 consecutive excitatory back-gate pulses (−2 V, 10 ms, and 10-s interval). Different current values correspond to

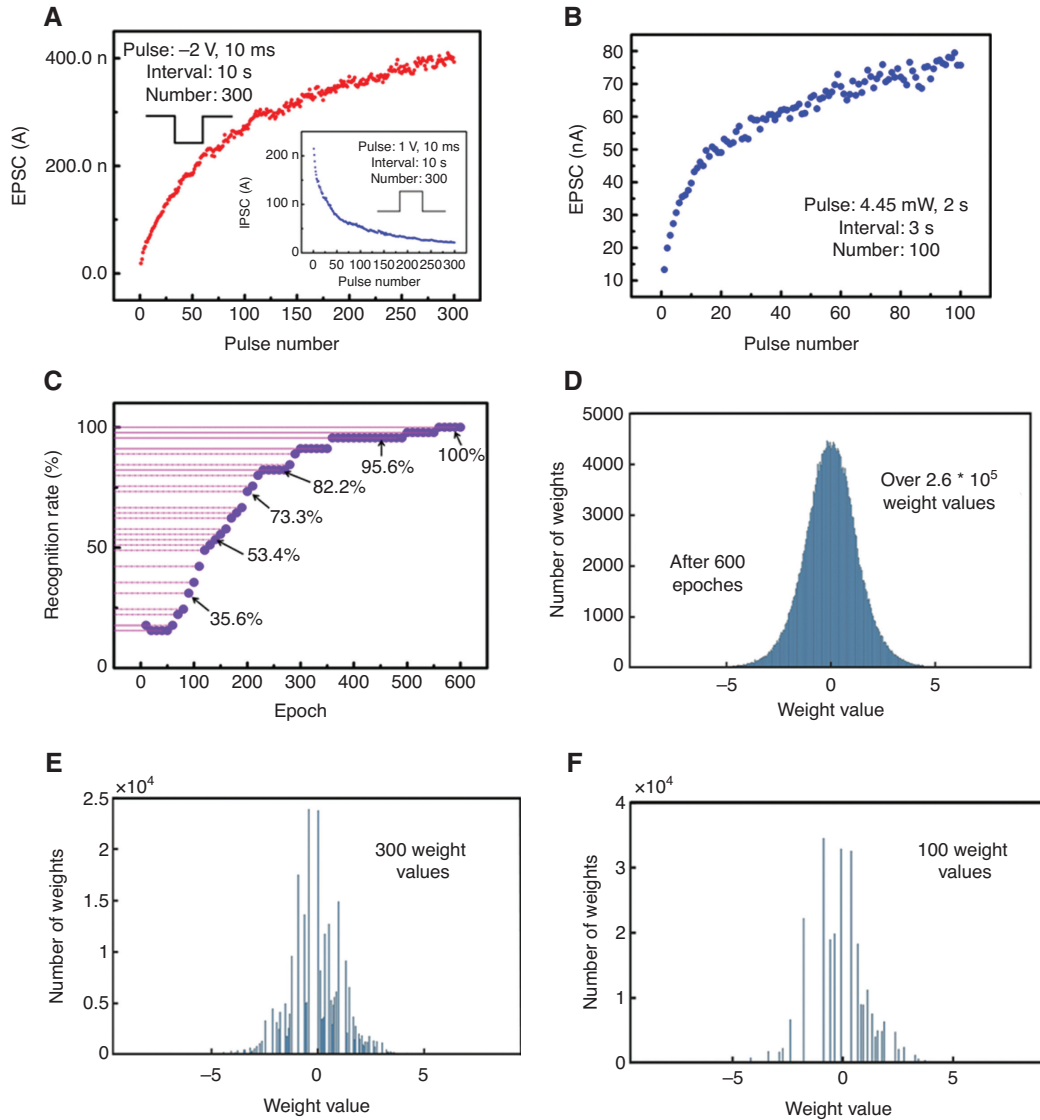
different conductance states, and each conductance state has high stability. By contrast, a continuously decreasing current was observed when 300 consecutive inhibitory pulses were applied (1 V, 10 ms, and 10-s interval), as shown in the inset of Figure 6A. In summary, a total of 600 effective conductance states have been obtained. Every single conductance state corresponds to a specific weight value in an ANN. We use the 300 conductance values, which generated by 300 consecutive excitatory pulses, as the weight values for ANN testing. In general, the current curve is nonlinear, but it can be regarded as a combination of two linear curves (Supplementary Figure S1). In each linear region, a voltage pulse induces a significant difference between conductance states, and therefore, we can effectively control the conductance state by changing the number of input pulses. Alternatively, upon the application of continuous incident light pulses (4.45 mW, 2 s with an interval of 3 s), we have obtained 100 effective conductance values (Figure 6B), which can be utilized for ANN testing.

We then built a three-layer ANN for face recognition (Supplementary Figure S2), including input layer, middle (hidden) layer, and output layer consisting of 1024, 256, and 15 neurons, respectively. One hundred sixty-five photographs (from Yale Face database) from 15 different human faces are used for ANN training and testing (Supplementary Figure S3). For each human face, eight images are used for ANN training, and the remaining three images are used for ANN testing. Thus, we have 120 images for training and 45 for recognition test. Each image has 1024 features

**Table 1:** Comparison of CTM and synapse device performance.

Device structure	Memory's performance		Corresponding synaptic device	Reference	
	Retention				Endurance
	Pulse	$\frac{I_{\text{on}}}{I_{\text{off}}}$ , Time (s)			Cycles or time
MoS <sub>2</sub> /high k CTM	+26 V, 200 ms −26 V, 200 ms	10 <sup>2</sup> , 2000 s	120 Cycles	–	Zhang et al. [39]
MoS <sub>2</sub> /high k CTM	+12 V, 100 μs −10 V, 10 μs	10 <sup>4</sup> , 10000 s	8000 Cycles	–	He et al. [40]
WSe <sub>2</sub> /high k CTM	+18 V, 1 s −18 V, 8 s	10 <sup>4</sup> , 500 s	500 Cycles	–	Hou et al. [38]
MoS <sub>2</sub> /PTCDA RRAM	−12 V, 25 ms	–	–	Good	Wang et al. [41]
Al/PEDOT:PSS RRAM	+1 V, 50 ms −1.5 V, 50 ms	–	–	Good	Wang et al. [42]
Pd/MoO <sub>x</sub>	365-nm UV light −4.5 V, 100 ms	–	–	Excellent	Zhou et al. [43]
MoS <sub>2</sub> /high k	±4 V, 1 ms ±2 V, 10 ms 520-nm light	10 <sup>4</sup> , 1000 s	1000 Cycles	Excellent	Our work





**Figure 6:** Synaptic performance of the MoS<sub>2</sub> synaptic devices.

(A) Three hundred conductance states after 300 negative pulses were applied (−2 V, 10 ms, and 10-s interval). Inset: 300 conductance states after 300 positive pulses (1 V, 10 ms, and 10-s interval). (B) One hundred conductance states after 100 consecutive laser pulses were applied (4.45 mW, 2 s, and an interval of 3 s). (C) Recognition rate curve with increasing training–testing cycles. (D) The distribution of weight values after 600 training–testing cycles. (E) The distribution of weight values that are replaced by 300 device conductance values. (F) The distribution of weight values that are replaced by 100 device conductance values.

corresponding to 1024 input neurons, and the input value of a hidden neuron can be expressed as follows:

$$Y_{in} = \sum_{m=1}^{1024} X_m V_{mn}$$

where  $X_m$  represents an input neuron. Then, a nonlinear transfer function was used to activate the result, and the output value of a hidden neuron is given by

$$Y_{on} = \frac{1}{1 + e^{-Y_{in}}}$$

The output of the hidden neurons was transferred to the output neurons as the input, and with the same summation and activation processes, the final output  $Z_{ok}$  can be obtained and expressed as

$$Z_{ik} = \sum_{n=1}^{256} Y_{on} W_{nk}$$

$$Z_{ok} = \frac{1}{1 + e^{-Z_{ik}}}$$

So far, we have completed the forward propagation of the neural network. In order to train the network, we need to calculate the output error and modify the weight value through back-propagation. Comparing the above-calculated output with the correct output, the total output error can be obtained, and it is expressed as

$$E = \frac{1}{2} \sum_{k=1}^{15} (O_k - Z_k)^2$$

where  $O_k$  is the correct output value. Then, the weight value is updated based on the derivative of the error during the back-propagation process. After updating the weights, a new image is fed to the ANN, and the weight update process is repeated until all 120 images have been used for training. Next, we use the trained network to identify the remaining 45 images and calculate the recognition rate. Generally, the recognition rate of the first recognition is very low, and in our ANN with 256 hidden neurons, the first recognition rate is only 17.78%. The face recognition rate keeps rising as the ANN learning proceeds deeper (Figure 6C), and the recognition rate can reach up to near 100% after 550 training-testing cycles. This proves that our ANN has excellent learning and recognition ability compared to previously published face recognition works [42]. Figure 6D shows the distribution of weight values after 600 training cycles (iterations), in which our ANN can achieve a near 100% recognition rate. Obviously, the weight distribution is very concentrated, and the weights became more scattered after more cycles (Supplementary Figure S4). To better demonstrate that our MoS<sub>2</sub> device is suitable to be applied to ANNs, all weight values in the ANN network were replaced by 300 device conductance values, the distribution of replaced weight values is represented in Figure 6E. Similarly, the 100 conductance states achieved by incident light pulses are also used to replace the weight values following the rules that the conductance values and the ANN weight values are normalized within the same interval and that each weight value is substituted by the closest conductance value. The distribution of replaced weight values (light) is represented in Figure 6F. It can be clearly seen that the shape of the statistical graph is basically the same as that in Figure 6C. Then, the replaced weight values were used in ANN for testing, and the recognition rate perfectly reached 100%. So, our devices can be used to build large-scale neural networks that can be modulated by using both electrical and optical approaches. In the reported similar face recognition work [42], the highest recognition rate is approximately only 95%,

which proves the excellent electrical properties of our MoS<sub>2</sub> synaptic device and the optimal ANN design.

In summary, by combining a CTM architecture and engineered dielectric stack, a high-performance MoS<sub>2</sub>-based artificial synapse device has been demonstrated. The device exhibited excellent and steady synaptic characteristics and perfect recognition in our ANN. The results indicated that the intriguing synapses based on 2D materials are very promising for large-scale neuromorphic systems and future artificial intelligence applications.

## Methods

Before fabricating the device, a 200-nm SiO<sub>2</sub>/Si substrate was first cleaned. Then, a 45-nm ITO film was sputtered on the substrate followed by a rapid annealing process at 400°C for 10 s in N<sub>2</sub> as the back-gate electrode. A 15-nm Al<sub>2</sub>O<sub>3</sub> was then deposited by atomic layer deposition (ALD) with the precursors of trimethylaluminum and H<sub>2</sub>O at 200°C as a blocking layer. And a 5-nm Ta<sub>2</sub>O<sub>5</sub>-TiO<sub>2</sub> (TTO) mixture film composed of Ta<sub>2</sub>O<sub>5</sub> and TiO<sub>2</sub> (1:1) was sputtered by using Ta<sub>2</sub>O<sub>5</sub> and TiO<sub>2</sub> ceramic targets as a charge-trapped layer [17]. After that, another layer of 4-nm Al<sub>2</sub>O<sub>3</sub> was deposited by ALD as the tunneling layer. The MoS<sub>2</sub> flake was mechanically exfoliated from a bulk material and selected with the thickness ranging from three to six layers, which is confirmed by TEM with a thickness of 2.9 nm (approximately four layers) (shown in Figure 1C). The Ti/Au electrodes were patterned by electron-beam lithography and deposited by electron-beam evaporation with the thickness 10/70 nm. Finally, the fabrication ends with a lift-off process. Figure 1B shows an optical image of the MoS<sub>2</sub> channel with the source and drain electrodes. The width and length of the MoS<sub>2</sub> channel were 20 and 10 μm, respectively. In order to accurately demonstrate the thickness of all components in our device, we cut the device along the dotted line, shown in Figure 1B, and analyzed it by TEM. The TEM photograph shows the thickness of the MoS<sub>2</sub> channel is approximately 2.9 nm, which indicates that the MoS<sub>2</sub> flake is approximately four layers thick. And the thickness of the engineered Al<sub>2</sub>O<sub>3</sub>/TTO/Al<sub>2</sub>O<sub>3</sub> stack is 4/5/15 nm.

**Acknowledgment:** This research was supported by the National Key Research and Development Program of China (grant no. 2018YFB2202800), the Shanghai Municipal Science and Technology Commission (18JC1410300), the National Natural Science Foundation of China (61904033, 61522404, 61704030, and 61974144, Funder Id: <http://>

dx.doi.org/10.13039/501100001809), the Shanghai Rising-Star Program (19QA1400600, Funder Id: <http://dx.doi.org/10.13039/5011000013105>), and the Basic Research Project of Shanghai Science and Technology Innovation Action (grant no. 17JC1400300).

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**Supplementary Material:** The online version of this article offers supplementary material (<https://doi.org/10.1515/nanoph-2019-0548>).