Performance analysis of single-walled carbon nanotube bundle interconnects for three-dimensional integration applications

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Compact equivalent circuit models for single-walled carbon nanotube (SWCNT) bundles are described, and the performance of SWCNT bundle interconnects is evaluated and compared with traditional Cu interconnects at different interconnect levels for through-silicon-via-based three-dimensional integration. It is shown that at local level, carbon nanotube bundle interconnects exhibit lower signal delay and smaller optimal wire size. At intermediate and global levels, delay improvement becomes more significant with technology scaling and increasing wire lengths. For 1 mm intermediate and 10 mm global level interconnects, the delay of SWCNT bundles can reach 45.49 and 51.84% of that of Cu wires, respectively.

1. Introduction: Through-silicon-via (TSV)-based three-dimensional (3D) integration is a promising design paradigm for interconnect-centric circuits [1]. However, a potential problem in 3D integration is the creation of reliable and low resistance horizontal interconnects and vertical TSVs. Carbon nanotubes (CNTs) have been proposed as a promising alternative to Cu interconnects in future ICs for their remarkable conductive, mechanical and thermal properties [2—4]. Although there has been a lot of interest in CNT-based interconnects for planar IC applications in recent years [5—9], there are unfortunately few studies that compare CNT interconnects with Cu interconnects in 3D integration. As 3D integration becomes an exciting path to boost the performance of modern ICs, it is critical to evaluate the impact of promising new interconnect paradigms such as CNTs on such systems. Such an analysis allows designers to understand the potential benefits and limitations of CNT bundle technology. It also gives them a true insight into realistic gains that can be achieved by switching to CNT-based horizontal interconnects and vertical TSVs. In this Letter, compact equivalent circuit models for single-walled carbon nanotube (SWCNT) bundle interconnects are described, which can serve as the basis for the performance analysis. Furthermore, a comparative performance analysis of traditional Cu interconnects with the CNT interconnects at different interconnect levels for 3D integration is presented.

2. Circuit model for SWCNT bundle interconnects: Owing to higher electrical conductivity, bundles of SWCNT interconnects are proposed instead of an isolated SWCNT to outperform their traditional Cu counterparts. The resistance of a CNT bundle R_{bundle} depends on the total wire cross-sectional area and its metallic density P_{m}, and it has a linear dependence on its length l for low-bias interconnect applications [2]

$$R_{\text{bundle}} = R_{\text{s}}/n_{\text{CNT}}\left(1 + l/l_0\right) \tag{1}$$

where the fundamental quantum resistance of SWCNT R_{s} is 6.45 kΩ [2], n_{CNT} is the number of metallic SWCNTs in a bundle, and l_0 is the electron mean-free path (MFP) with theoretically and experimentally derived constants of 2.8 and 0.9 μm/nm for a typical SWCNT diameter of 1 nm [3].

The effective value of kinetic inductance L_{kin} in a single tube is about 4 nH/μm, which is about four orders of magnitude higher than magnetic inductance L_{mag} (< 0.5 nH/mm) [4]. However, in a bundle, the kinetic component dramatically reduces, because CNTs are in parallel. The magnetic component remains relatively constant with the wire dimensions. The total inductance of a CNT bundle is the sum of the parallel combination of n_{CNT} kinetic inductances L_{kin} and magnetic inductance L_{mag}.

The equivalent capacitance of a CNT is a series combination of quantum capacitance C_{Q} and electrostatic capacitance C_{E}. A C_{Q} of 100 aF/μm is of the same order of magnitude as its electrostatic counterpart [4]. However, in a bundle, the quantum components add in series, making the bundle's total C_{Q} negligible compared with its C_{E}. Some reports have shown that the effective capacitance of a CNT bundle is equal to that of Cu with the same cross-sectional dimensions [5, 6].

3. SWCNT bundles against Cu interconnects: Based on the aforementioned analysis, the delay of SWCNT bundle interconnects is estimated and compared with Cu interconnects. A typical interconnect structure used for performance evaluation is shown in Fig. 1; where V_i is a step signal, k and s are the number and size of repeaters. R_0, C_0 and C_{p} are, respectively, the output resistance, the input capacitance and the output capacitance of a minimum-sized repeater. For local interconnects routed in the lowest metal level with minimum width, the driver and load are assumed to be five times larger than the minimum-sized repeaters. Different from planer ICs, intermediate and global interconnects in 3D integration consist of horizontal interconnects and vertical TSVs. Repeaters are used to increase the drive capability. All interconnect parameters used in Spice simulations are obtained from ITRS 2009 [7], as shown in Table 1. The effect of scattering on Cu resistivity ($\rho_0 = 2.2$ μm—cm) is considered with a surface-scattering coefficient p of 0.6 and grain reflection coefficient R of 0.5. The capacitance and inductance of Cu are calculated using the Berkeley Predict Technology Model [8]. The

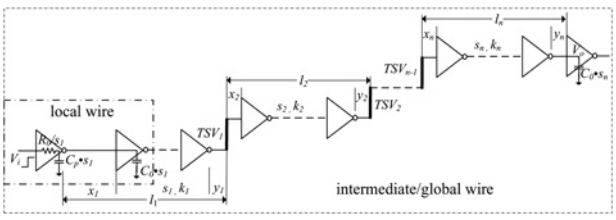

Figure 1 *3D wire used for performance evaluation*

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Table 1 ITRS 2009-based simulation parameters

Technology node		14 nm	22 nm
local and intermediate	Width W, nm	14	22
	AR	2	2
	ILD thickness T_{ox}, nm	25.2	39.6
	ε_r	2.15	2.3
	TSV diameter, μm	0.8	1.0
	TSV depth, μm	10	10
global	Width, W, nm	21	33
	AR	3	3
	ILD thickness T_{ox}, nm	52.5	76.8
	ε_r	2.15	2.3
	TSV diameter, μm	2	4
	TSV depth, μm	20	20
minimum-sized-gate	R_o, kΩ	18.33	16.67
	C_p, fF	0.03	0.049
	C_o, fF	0.065	0.14

value of $P_m = 1/3$ with todays fabrication techniques, which implies that only 1/3 of the SWCNTs in a bundle are conducting. The inter-plane TSV is equivalent to a distributed resistance—inductance—capacitance model and the related parasitic parameters are extracted with the compact expressions in [9].

Fig. 2*a* shows the interconnect delay against wire AR (height-to-width ratio) at the local level. It is observed that the CNT bundle exhibits a lower delay than Cu at all ARs. The minimum delay is obtained by optimising AR. For larger AR, signal delay is determined by the wire capacitance C_w and driver resistance R_{tr} product; an initial reduction in AR lowers the C_w, and further lowers the delay. However, below a certain AR, the delay is dominated by C_w and wire resistance R_w product. R_w rises with smaller AR, and C_w cannot reduce as fast as the increase in R_w because of the limitation of constant inter-level dielectrics and fringe components; thus the delay increases with smaller AR. Benefiting from a longer MFP and hence lower resistivity, the optimal AR and signal delay of longer MFP CNTs ($l_0 = 2.8$ μm) are both lower than that of the shorter case ($l_0 = 0.9$ μm).

Optimal AR design also significantly increases the wire current density. As shown in Fig. 2*a* (right *y*-axis), the current density at Cu optimal AR is about 30.2×10^6 A/cm^2, which is two times higher than that allowed of 14.7×10^6 A/cm^2. To eliminate electromigration (EM) concerns, the minimum AR in Cu is limited to about 1.5 for the ITRS-dictated minimum widths, whereas a single CNT can carry a current density up to 10^9 A/cm^2; thus only CNT can be operated at the optimal AR. A smaller optimal AR for CNT bundles would bring a dramatic power reduction because of a lower capacitance.

In addition, the optimal signal-delay ratio of the two technologies is also explicitly plotted in Fig. 2*b*. It is observed that the performance of SWCNT bundles is much better than that of Cu, and the improvement in delay increases with increasing length, longer MFP and technology scaling. For 100 μm length, the minimum delay of SWCNT bundle interconnects can reach 47.68 and 59.68 ps, respectively, at 22 and 14 nm technology nodes, which is as low as 34.48 and 19.85% of that of Cu wires.

Using the repeaters insertion methodology for 3D wires [10], the impact of TSV impedance on the signal delay of each segment is introduced, and the repeaters location, each segment minimum delay and further the total wire near-optimal delay are obtained by numerical iterative methods. The optimal number k_{opti} and size of repeaters for inter-plane 3D wire i are given by

$$k_{opti} = \left((l_i - x_i - y_i) \sqrt{\frac{R_i C_i}{2R_0 (C_0 + C_p)}} + 1 \right) \times \left[1 + \beta \left(T_{L/R} \right)^3 \right]^{-0.3} \quad (2)$$

$$s_{opti} = \sqrt{\frac{R_0 (C_{L\_i} + (l_i - x_i) C_i)}{(C_0 + C_p)(R_{in\_i} + (l_i - y_i) R_i)}} \left[1 + 0.18 \left(T_{L/R} \right)^3 \right]^{-0.24} \quad (3)$$

where the repeater size is s_{opti} times larger than a minimum gate size. R_i, L_i and C_i are the resistance, inductance and capacitance per unit length of segment i on the ith plane, respectively. l_i is the length of segment i, x_i and y_i represent the optimal locations of repeaters. R_{in_i} and C_{L_i} are the input resistance and load capacitance, respectively, of segment i. $T_{L/R}$ is employed to account for the effect of inductance $T_{L/R} = \sqrt{L_i / R_i / \left(R_0 \left(C_0 + C_p \right) \right)}$ [11]. The fitting coefficient β is unique and taken as 0.21 for the Cu interconnects [12]. Since SWCNT resistivity is length dependent, the fitting value of β is not unique and in the range of 0.21—0.28 for different length SWCNT bundles, and assumed to be 0.25 for simplicity.

Based on the aforementioned analysis, Fig. 3 shows the signal-delay ratio of the two technologies at the intermediate and global levels for a typical three planes stack. Four design configurations, in which CNTs with longer MFP ($l_0 = 2.8$ μm) are used as wiring and as TSVs, are used to investigate the feasibility of CNTs for inter-plane interconnects in 3D integrations. The homogeneous horizontal interconnects are assumed to be uniformly distributed on each plane. The widths of intermediate interconnects and global interconnects are three times and five times larger than the minimum width predicted by ITRS to improve wire delay. It is

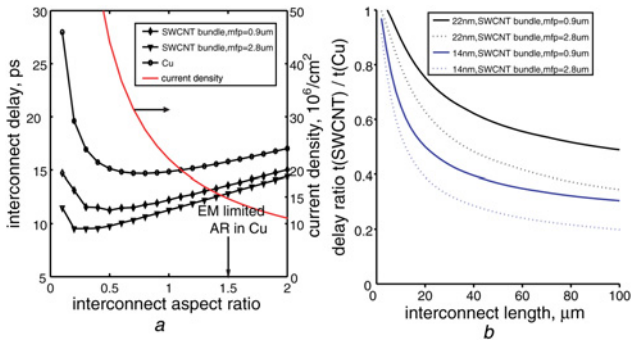

Figure 2 *Local interconnects delay (left y-axis) and current density (right y-axis) against AR for 20 μm wire length at 22 nm node (Fig. 2a); delay ratio of SWCNT bundle interconnects with respect to Cu interconnects at local level*

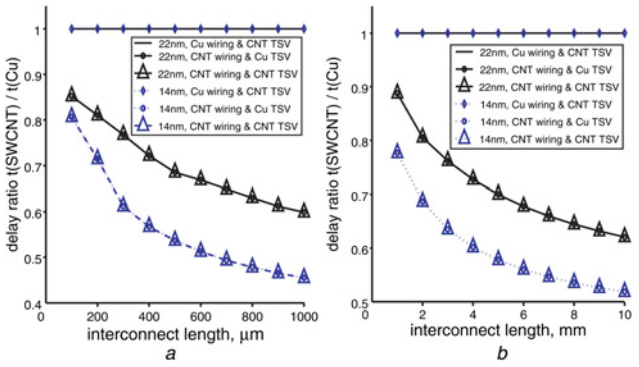

Figure 3 *Signal-delay ratio of SWCNT bundle interconnects with respect to Cu interconnects*
a Intermediate level
b Global level

Table 2 Comparison of optimal number and size of repeaters in the intermediate and global interconnects for different technology nodes

Length		14 nm				22 nm			
		Cu wiring Cu TSV	Cu wiring CNT TSV	CNT wiring Cu TSV	CNT wiring CNT TSV	Cu Wiring Cu TSV	Cu wiring CNT TSV	CNT wiring Cu TSV	CNT wiring CNT TSV
					Intermediate				
1 mm	k_{opt}	24	24	9	9	11	11	6	6
	s_{opt}	57.04	57.05	111.43	111.47	58.83	58.81	86.7	86.72
	area	1369	1369.1	1002.9	1003.2	647.11	646.83	520.22	520.34
					Global				
10 mm	k_{opt}	71	71	34	34	32	32	17	17
	s_{opt}	235.37	235.37	424.64	424.68	244.71	244.71	383.8	383.81
	area	16711	16711	14438	14439	7830.7	7830.8	6524.6	6524.8

observed that the signal delay of SWCNT bundle interconnects is smaller than that of Cu and the improvement in delay increases with increasing length and technology scaling. At 1 mm intermediate and 10 mm global level interconnects, the delay of SWCNT bundle interconnects can reach 93.82 and 314.1 ps, respectively, which is as low as 45.49 and 51.84% of that of Cu. Such improvement ratio seems higher than the ratio of 40% for SWCNT bundles in [6]. This is mainly caused by the different widths of wires used for simulation. The performance enhancement of SWCNT bundles decreases with increasing wire width. In addition, even for shorter intermediate level interconnects in which TSV height may account for a maximum 20% of the whole wire length, TSV materials still have shown minor impact on the performance enhancement. This is because of the fact that for long inter-plane interconnects, the effect of TSV resistance on signal delay is negligible compared with the resistances of repeaters and horizontal interconnects. Such results are also consistent with the conclusions in [13].

Since the optimal number and size of repeaters for inter-plane interconnects are wire resistances dependent as (2) and (3), CNT bundle designs have an important impact on the repeater insertion. As shown in Table 2, the repeater size in SWCNT bundles is slightly larger than that in Cu, but the optimal number of repeaters for SWCNT bundles is much less than that for Cu for the same length; hence, the total insertion area and power dissipation of repeaters in a SWCNT bundle are much lower than that in the Cu counterparts. Here, the repeater area is defined as the product of the repeater number and size. Similar to the delay case, TSV materials show little impact on the repeater insertion.

4. Conclusions: The performance of SWCNT bundle interconnects is evaluated and compared with traditional Cu interconnects at local, intermediate and global levels for TSV-based 3D integration. It is demonstrated that at all levels, CNT bundle interconnects exhibit lower signal delay and the improvement in delay becomes more significant with technology scaling and increasing wire lengths. Owing to smaller local wire AR and fewer repeater numbers, CNT bundle-based interconnects can have a lower power density than the Cu counterparts.

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