Role of mask patterns in fabrication of Si nanotip arrays

Si-Hyeong Cho[1], *Jung-Hwan Lee*[1], *Jin-Goo Park*[1,2]

[1]*Department of Bionano Technology, Hanyang University, Ansan 426-791, Republic of Korea*
[2]*Department of Materials Engineering, Hanyang University, Ansan 426-791, Republic of Korea*
E-mail: jgpark@hanyang.ac.kr

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Different shapes of silicon (Si) nanotip arrays using reactive ion etching with various mask patterns were fabricated, and the surface profile, surface roughness and quantitative etch characteristics of the Si nanotip were characterised. It was found that the geometry as well as etch characteristics of Si nanotip arrays could be modified by changing the initial mask patterns. Pyramidal and conical shaped Si nanotips could be obtained from square and circular mask patterns, respectively. The alternate square array pattern resulted in a Si nanotip with a wavy array whereas the honeycomb mask pattern resulted in a Si nanotip in a hexagonal array. In terms of etch rate, the circular pattern mask showed faster etching than the square patterns. Also, the parallel pattern showed faster etching than the alternate pattern under the same conditions. The tip size and height of Si nanotip structures determined by atomic force microscopy measurement were in the range of 50—80 and 450—750 nm, respectively.

1. Introduction: Since the development of plasma etching technologies such as reactive ion etching (RIE), isotropic etching, ashing and plasma cleaning, nanostructures with different shapes such as nanowires, nanotubes, nanorods, nanocones and nanotips have been widely investigated [1—13]. In particular, vertical and well-oriented Si nanotip array structures are becoming increasingly important for use not only in electronic devices such as field effect transistors, field emission devices and solar cells but are also suitable for use in applications such as biosensors, antireflection surfaces and microelectro-mechanical-systems [5—11, 14—19]. The applications of this structure may be chosen based on the requirements for a specific function.

Si nanotip array structures can be fabricated by various etching processes such as electrochemical etching, anisotropic chemical wet etching and plasma dry etching after patterning to define the micro or nanoscale patterns [20—24]. Kim *et al.* [11] and Alves *et al.* [21] proposed a simple method involving the combination of conventional lithography with chemical wet etching and RIE processes. Chen [8] reported that Si nanotip arrays could be fabricated by a synergetic approach of E-beam lithography and an RIE process. Also, Carvalho *et al.* [10] and Choi and Kim [22] used interference lithography and RIE to fabricate large area arrays of Si nanotips. Recently, some researchers combined self-assembly techniques by including colloidal lithography or diblock copolymer as patterning methods for submicron patterns with RIE etching to fabricate Si nanotip arrays [5, 23, 24]. Most previous works have concentrated on developing Si nanotip array structures, but controlling shape, size and interspacing between the tips still remains a challenging issue. There is no comprehensive work reporting the initial mask pattern's effect on nanotip fabrication in the literature.

In the work reported in this Letter, we fabricated various types of Si nanotip arrays from different mask patterns and investigated the influence of initial mask patterns on the etch results after the RIE process. Mask pattern type can affect the etching behaviour, so it should be controlled precisely during the fabrication of Si nanotip arrays. It was found that the shape, size and array type of Si nanotips could be optimised by the initial mask pattern design. The results of this study could serve as a useful guideline for fabricating various Si tip structures.

2. Experimental: Four types of mask patterns such as parallel square, circular, alternate square and honeycomb, were prepared as shown in Fig. 1 to investigate their effect on Si nanotip array fabrication. Each pattern has array features ranging from 500 nm to 1 μm lines with spacing from 500 nm to 1 μm in a 500 μm^2 area. Fig. 2 shows a schematic of the process sequence used for fabricating Si nanotip arrays. A *p*-type Si (100) substrate was used for the experiment. Thermal oxide (300 nm) was grown on a Si wafer at 1000°C as a masking layer because of its good adhesion on Si, as well as high etching selectivity to Si [8]. Bottom antireflective coating (BARC) and photoresist (PR) coating were performed to construct the oxide mask patterns using a KrF stepper (PAS 5500/300C, ASML, The Netherlands).

A dry etcher (SRT 600, Sorona, Korea) was used for the RIE process. The first RIE process was performed to etch SiO_2 by supplying 30 sccm of tetrafluoromethane at a working pressure of 150 mTorr and a plasma power of 150 W. The aforementioned condition is an optimised one and has an etch rate of 150 nm/min for SiO_2. Subsequently, the residual PR and BARC layer were removed by using a microwave asher (Enviro II, ULVAC, USA). In the second RIE process, sulphur-hexafluoride (SF_6) in combination with oxygen (O_2) was used for isotopic Si etching. SF_6 gas is conventionally used for isotropic etching of the Si layer, but it introduces a rough surface on the etched Si substrate [9, 11, 25]. Therefore O_2 gas was blended with SF_6 to improve surface

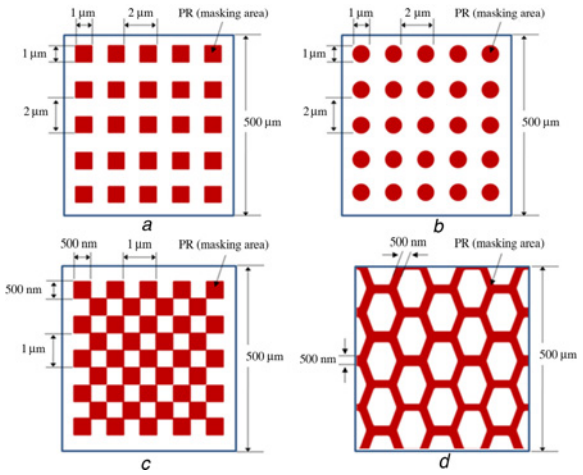

Figure 1 *Initial mask patterns used for fabricating Si nanotip arrays*
a 1 μm square array
b 1 μm circular array
c 500 nm alternate square array
d 500 nm honeycomb array

Table 1 Etch rates and ratios of various Si nanotips against mask pattern types

Size	Mask pattern type	R_H, nm/min	R_V, nm/min	Etch ratio	Si nanotip type
1 μm	parallel square	309.5	410.5	0.75	pyramidal tip array
	alternate square	221.5	253.8	0.87	wavy pyramidal tip array
	parallel circular	460	450	1.02	conical tip array
	alternate circular	261.8	272.7	0.96	conical tip array
500 nm	alternate square	712.5	750	0.95	wavy pyramidal tip array
	honeycomb	810	840	0.96	hexagonal array

R_H: horizontal etch rate, R_V: vertical etch rate, etch ratio = R_H/R_V.
The etch rate is sensitive to mask pattern's size, shape and array type.

roughness [10, 26]. RIE of Si was carried out by providing 30 sccm of SF_6 and 5 sccm of O_2 at a working pressure of 150 mTorr and a plasma power of 50 W. This is also the optimised condition, and its etch rate depended on the mask pattern types as listed in Table 1. The remaining SiO_2 mask on top of the Si nanotip arrays was removed by wet etching in dilute HF (deionised water: hydrofluoric acid = 10:1) solution. The initial mask patterns and Si nanotip arrays fabricated by RIE were observed using an optical microscope (OM, L-150A, Nikon, Japan) and field emission scanning electron microscopy (FESEM, S-4800, Hitachi), respectively, to compare the etching behaviours. The topography and structural dimensions were determined by atomic force microscopy (AFM, XE-100, Park Systems, Korea).

3. Results and discussion: Fig. 3 shows FESEM images of the patterned SiO_2 layer after PR removal. Four kinds of mask patterns — a square array with a line width and interspacing of 1 μm as shown in Fig. 3*a*, a circular array with a diameter and interspacing of 1 μm as revealed in Fig. 3*b*, an alternate square array with a line width and interspacing of 500 nm as shown in Fig. 3*c*, and a honeycomb array with a line width of 500 nm as shown in Fig. 3*d* — were used to define the SiO_2 layer to fabricate the Si nanotip arrays. It is important to note that the pattern accuracy varies with lithography conditions because of the differences in configuration. The shape of the SiO_2 layer was defined to compare the patterns of the photomask on top of the Si nanotip arrays. The desired thickness of SiO_2 as a masking layer can be controlled by the dimensions of the Si tip. A thick mask layer can be used to obtain a microscaled Si tip structure. On the other hand, a thin mask layer would be sufficient for nanoscaled Si tip fabrication.

To fabricate Si nanotip arrays, RIE plasma with a mixture of SF_6 and O_2 gases was used as an etchant with patterned SiO_2 as a

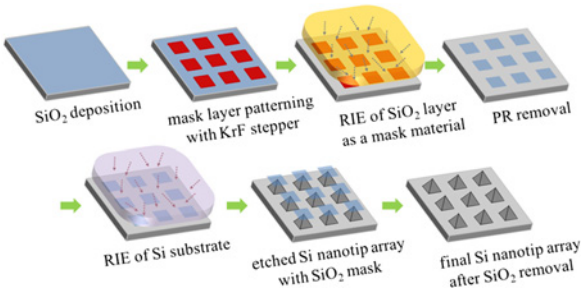

Figure 2 *Schematic representation of the Si nanotip array fabrication process*

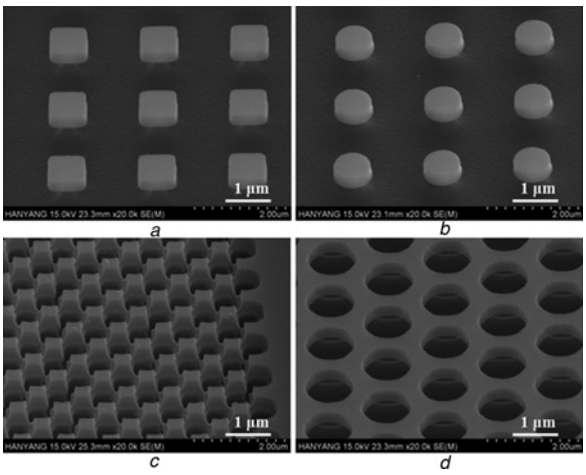

Figure 3 *FESEM images after RIE of SiO_2 and Si substrate with an etch mask layer*
a 1 μm square array
b 1 μm circular array
c 500 nm alternate square array
d 500 nm honeycomb array

masking layer. The role of oxygen in the gas mixture is to change the isotropy of etching [27]. During the etching process using SF_6 and O_2 plasma, the active fluorine (F) ions etch the Si by forming volatile SiF_4, whereas the oxygen (O) ions passivate the Si surface with SiO_xF_y [25, 28]. F and O atoms compete to react with active Si surface sites during Si etching. This suggests that the shape of the nanostructures can be tailored by adjusting the flow ratio between SF_6 and O_2 to reach an optimum balance between etching and passivation [5].

SF_6 and O_2 gases were mixed at a ratio of 6:1 by volume inside the chamber and used for etching Si. A suitable amount of O_2 addition is more efficient to form a smoother surface because of the intensive reaction between Si and F, which may result in a rough surface and affect the nanotip array's final applications [26]. For this reason, researchers have used a combination method that includes both thermal oxidation and the removal of the oxide layer by wet etching, called sharpening oxidation, to improve surface roughness [29, 30]. Also, the pressure in the reactor during RIE of Si by SF_6 and O_2 plasma affects the topography of nanotips and affects the etching behaviour [8, 9]. At high pressures the density of the F radical increases, causing increased isotropic chemical etching. However, at low pressures, because of the reduced density of the F radicals, the etching tends to be more anisotropic, causing the etched structures to be vertical pillars rather than cones or pyramids. In the present work, the pressure and plasma power were fixed at optimum conditions; a working pressure of 150 mTorr and a plasma power of 50 W, since we were focused only on the effect of the initial mask patterns.

Etch results such as horizontal etch rate (R_H), vertical etch rate (R_V) and etch ratio during the RIE process are shown in Table 1. Etch ratio is defined as the ratio of R_H to R_V. From the etching results, the etch rates of Si were found to be significantly different for each type of nanoarray patterns and might be influenced by the shape, size and layout of the mask patterns under the same RIE process conditions. The mask patterns with a parallel array showed almost two times larger etch rate than the alternate arrays. Moreover, in terms of the mask shape, the etch rate of circular patterns was larger than that of square patterns. The etch ratios were slightly different with various types of mask patterns. It seemed that the mask types might importantly affect plasma balance for the isotropic etching process, however the reason for the etching mechanism will be continuously studied in the near future. Fig. 4 shows different etching behaviours of Si nanotip arrays fabricated

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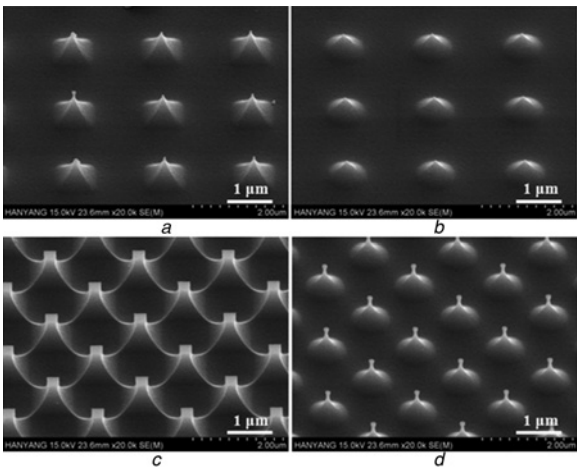

Figure 4 *FESEM images of various Si nanotip arrays which have different etch behaviours after the isotropic RIE process and subsequent removal of the SiO_2 mask layer using dilute HF*
a 1 μm square array
b 1 μm circular array
c 1 μm alternate square array
d 1 μm alternate circular array

from four kinds of mask patterns with a fixed line width or diameter of 1 μm while varying only the layout and shape of the mask

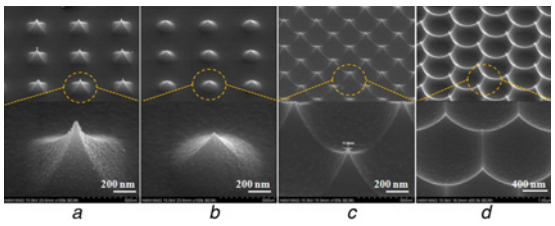

Figure 5 *FESEM images of various Si nanotip arrays after the isotropic RIE process and subsequent removal of the SiO_2 mask layer using dilute HF*
a Pyramidal Si nanotip array
b Conical Si nanotip array
c Si nanotips with wavy array
d Si nanotips with hexagonal array

patterns. Interestingly, the etching behaviour of the circular patterns seen in Fig. 4*b* was relatively more intensive than that of the square patterns found in Fig. 6*a*, and the etching behaviour of the parallel array patterns shown in Figs. 4*a* and *b* was more intensive than that of the alternate array patterns shown in Figs. 4*c* and *d*. This may be because of the difference in the fraction of exposed area of each pattern during the RIE process. It is desirable for etching to be independent of feature size, aspect ratio, fraction of exposed material and mask material. The difference in the etching behaviour may also be explained based on the loading effect. The local or microscopic loading effect occurs when there is sensitivity of etch rate to pattern density, and thus etch rates may change over distances

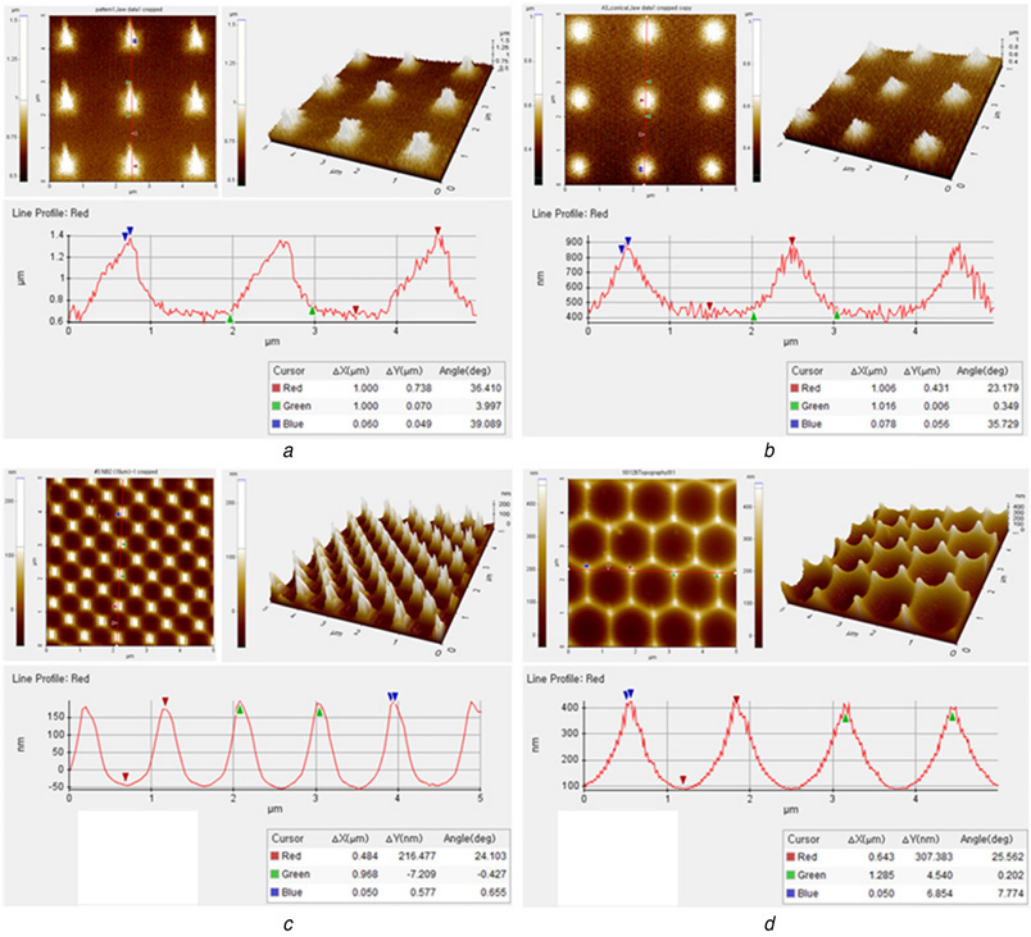

Figure 6 *AFM images of the Si nanotip arrays fabricated by the RIE process with different mask patterns*
a 1 μm square array
b 1 μm circular array
c 500 nm alternate square array
d 500 nm honeycomb array

of microns [31]. The reactant concentration may vary locally because of consumption by a reactive material and non-consumption by a non-reactive material. The parallel array pattern had a larger fraction of open area than the alternate array pattern. A dense mask patterned area requires an enormous amount of fluorine for etching when compared with a dispersive mask patterned area. In other words, etching is limited by the availability of reactant species. Hence, a dispersive mask patterned area shows less etching behaviour when compared with a dense mask patterned area.

Moreover, the shape and layout of SiO_2 patterns as a mask layer were found to be one of the important parameters in determining the morphology of Si nanotip arrays. As shown in Fig. 5, various shapes of Si nanotip arrays were fabricated by the RIE process and the morphological characteristics of the tips were strongly influenced by the initial mask patterns. A pyramidal Si nanotip array was fabricated from a square mask while a conical Si nanotip array arose from a circular mask. With an alternate square array pattern, a Si nanotip array was produced in the form of waves, whereas the honeycomb-shaped mask generated a hexagonal array of Si nanotips.

Fig. 6 shows the AFM results for various Si nanotip arrays after RIE with different mask patterns. An increase in the size of the mask patterns resulted in a larger Si nanotip. In the case of a pyramidal Si nanotip shown in Fig. 6*a*, the height and the size of the tip were found to be 750 and 60 nm, respectively. The conical Si nanotip shown in Fig. 6*b* measured a height of 450 nm and a tip size of about 80 nm. On the other hand, the Si nanotip with a wavy array possessed a height of 500 nm and tip size of 50 nm as shown in Fig. 6*c*. Also, the Si nanotip with a hexagonal array had a height of 700 nm and a tip size of 50 nm as indicated in Fig. 6*d*. Under the proposed conditions, the sharpest fabricated tip presents a curvature radius of about 50 nm and a height of <1 μm.

4. Conclusions: We have explored a simple approach for manufacturing different shapes of Si nanotip arrays using an isotropic RIE process with different types of mask patterns. Generally, the dimensions of the Si nanotips can be adjusted by changing the RIE process conditions. It was found that the size, shape and layout of Si nanotips could be easily controlled by using initial mask patterns with a predetermined size, shape and layout. Pyramidal and conical Si nanotips with wavy and hexagonal arrays, respectively, were fabricated with a tip size of 50 nm and a height <1 μm. This approach is sufficiently flexible to enable the production of various Si nanotip shapes using different creative mask designs. This work illustrates how initial mask pattern influences dry etching during Si nanotip fabrication.

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