Development of phase shift lithography for the production of metal-oxide-metal diodes

Linzi E. Dodd[1], *Mark C. Rosamond*[1,2], *Andrew J. Gallant*[1], *David Wood*[1]

[1]*School of Engineering and Computing Sciences, Durham University, South Road, Durham, DH1 3LE, United Kingdom*
[2]*Faculty of Engineering, School of Electronic and Electrical Engineering, University of Leeds, Leeds, LS2 9JT, United Kingdom*
E-mail: david.wood@durham.ac.uk

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Metal-oxide-metal (MOM) diodes have been produced by combining two novel techniques: a reactive ion etche and subsequent plasma oxidation, and a phase shift lithography process. This has resulted in a significant reduction in device feature sizes, down to sub-micron dimensions and with an improved zero voltage curvature coefficient of up to 2.8 V^{-1} for the associated diodes. Given the use of MOM diodes in high speed rectification applications, the combination of the reduction in diode area as well as the controlled oxide growth aims to assist in the improved cutoff frequency of the devices, thus ensuring the potential for high speed applications.

1. Introduction: Metal-oxide-metal (MOM) diodes have the potential to rectify terahertz radiation collected by micron-scaled antennas from waste heat sources and convert this into a useful DC current [1–3]. The antennas themselves are comparatively straightforward to make, with micron-scale dimensions. However, the diodes must be much smaller than this, which leads to production and characterisation issues.

The MOM diode structure consists of two dissimilar metals separated by a native oxide layer, which is sufficiently thin to allow electron tunnelling to occur, that is, 5 nm or thinner [4]. A functional diode is best achieved by using one metal which will oxidise readily and another which is inert. By choosing two metals with a maximum difference in work function, we can increase the asymmetry of the resulting diode. Many metal combinations have been tried, for example, Ni–Au [5] and Al–Pt [6]; here we have chosen titanium, which oxidises readily, and maximised the work function difference by using inert platinum as the other metal.

Initial diodes were produced using furnace oxidation, which gave excellent results with respect to a universal figure of merit, the curvature coefficient (CC) [7, 8]. However, more control was required over the thickness and uniformity of the oxide layer, and an alternative method of oxidation was investigated; this involved a reactive ion etch (RIE) of the native titanium oxide and plasma oxidation regrowth [9]. In [9], diodes with a uniform oxide of known stoichiometry were produced and the thickness of this oxide was controlled as a function of the oxygen plasma power used to create it. Having such a level of control on the oxide is vital as even small oxide changes have a significant impact on diode performance.

As well as oxide thickness and uniformity considerations, the diodes must be sufficiently small for high speed rectification to occur. Other groups have produced diodes using electron beam lithography, for example, [10], which allows very small features to be produced. However, this is a serial writing process, resulting in very slow processing times. If these diodes and their associated antenna are ever likely to be used in energy recovery, there needs to be a way of mass producing large volumes of devices at high speed. A novel, batch scalable process is required which can also produce sub-micron features. Nanoimprint lithography (NIL) is an interesting field for such demands [11], but NIL is a direct copying process and a master stamp is still required. Therefore phase shift lithography (PSL) has been used as an important step towards demonstrating mass manufacturability, with novel PDMS stamps made from master SiO_2 patterns on silicon substrates.

1.1. Phase shift lithography: Work in [12] describes the production of feature sizes in the region of 90 nm using an elastomeric phase mask and incoherent, polychromatic ultraviolet light. The structures add a phase element to masks which would usually just provide binary amplitude information. By using thick and thin regions in a mask, the phase of two adjacent paths of light can be shifted by an odd multiple of π, resulting in an intensity of zero at every edge by destructive interference, as shown in Fig. 1 [13].

The profile of a phase shift mask can be seen, with the theoretical intensity profile below it (Fig. 1*a*) and the resultant photoresist patterns which result from such a phase mask; positive photoresist (Fig. 1*b*) and negative photoresist (Fig. 1*c*), assuming an intensity which corresponds to the orange line in (Fig. 1*a*). To ensure a repeatable process, regardless of metal choice, lift-off is the preferred method for this technique. However, the contrast of the negative photoresists is insufficient to provide a suitable lift-off profile. By underexposing the photoresist, the intensity of light on the

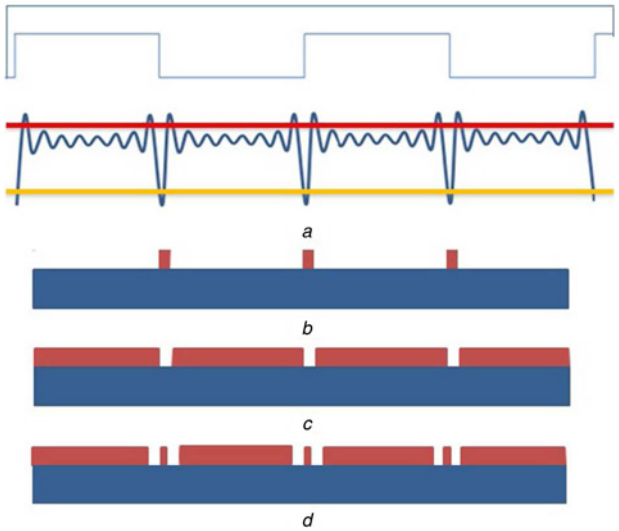

Figure 1 *Phase shift process*
a Profile of a phase shift mask with the ideal intensity profile
b Ideal effect of this intensity on positive photoresist (orange line)
c Ideal effect of this intensity on negative photoresist (orange line)
d On an intensity inversion in positive photoresist (red line)

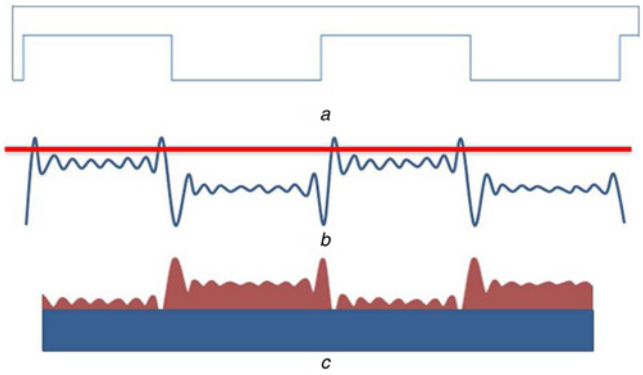

Figure 2 *Profile of a phase shift mask, actual intensity profile, and intensity inversion pattern produced in positive photoresist*
a Profile of a phase shift mask
b Actual intensity profile
c Intensity inversion pattern produced in positive photoresist

photoresist can be altered, which corresponds to the intersection with the red line in (Fig. 1*a*). The photoresist profile in (Fig. 1*d*) is the ideal pattern produced in positive photoresist as a result of underexposure.

Process trials indicated that an additional effect was taking place, resulting in a photoresist profile that did not match that in (Fig. 1*a*), but instead appeared to be a superposition of the step height of the phase mask and the original intensity profile, which can be seen in Fig. 2*b*. This could be because of the different transmission coefficients in different regions at the stamp–substrate interface, because of the presence of air gaps in one of the polarities. This equates to a transmission coefficient of 0.999 in the direct contact regions, compared with a transmission coefficient of 0.898 in the regions separated by an air gap. As a result, the actual photoresist profile, which is an inversion of the intensity profile, can be shown in Fig. 2*c*. This profile has been confirmed experimentally, with Fig. 3 showing a typical atomic force microscopy (AFM) image.

To produce a PSL stamp, an *N*-type ⟨100⟩ silicon of 10–30 Ωcm resistivity was chosen as the substrate material (2-inch diameter wafers). The depth of the features (also known as surface relief) was calculated for the average wavelength of the UV light used for exposure (330–460 nm). The substrate was oxidised to provide an insulating 456 nm film, calculated to provide the correct step height for the average wavelength of light used to successfully invert the phase at the interface. Using standard lithographic techniques, a pattern was then transferred onto the substrate in Microposit SPR-350 photoresist. An Oxford Instruments combined RIE/plasma etch system was then used to etch this pattern into the silicon dioxide layer (25 sccm CHF_3, 25 sccm Ar, 40 mT, 200 W and 15 min), thus providing a three-dimensional master stamp. PDMS (Sylgard 184, 6:1 ratio) was then cast onto the patterned SiO_2 substrate and cured to form an UV transparent elastomeric stamp.

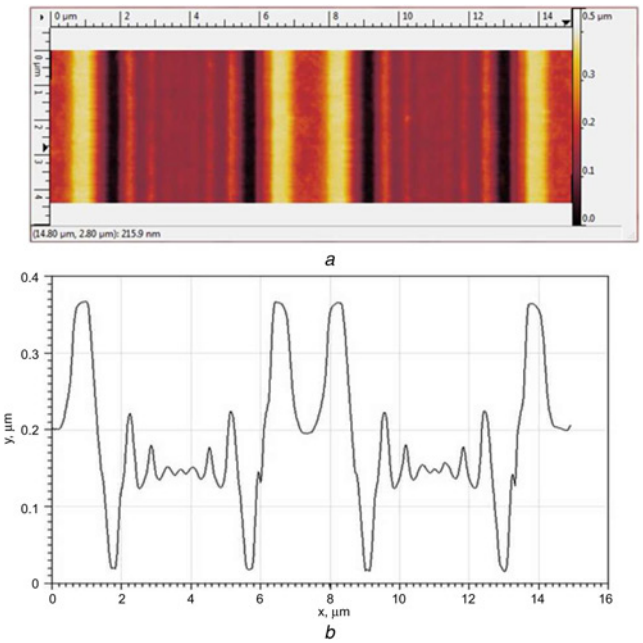

Figure 3 *AFM image of phase shift lines and their profiles in positive photoresist*
a AFM image of phase shift lines
b Their profiles in positive photoresist

2. Fabrication: Borosilicate glass wafers were used as a substrate for the fabrication of diodes. A bi-layer lift-off process, using PMGI SF9 and SPR-350 photoresists and MF-319 developer, was used to produce a base layer pattern on the wafer, on top of which 25 nm of titanium and 50 nm of gold were deposited in the same e-beam evaporation process. The photoresist was removed using Microposit 1165. The resulting pattern included all contact pads and a common connection for final testing, as shown in Figs. 4*a* and *b*.

The lift-off process was repeated twice; first with a design which allows all but the rectangular contact pad region to be coated with a thin layer of chromium (Fig. 4*b*), and secondly with a mask design the leaves only the common connection exposed (the horizontal line seen running through (Figs. 4*b–e*). An etchant (4:1:8 KI:I_2:H_2O) was used to remove the uncovered gold, leaving a region of titanium exposed only on the common connection, which can be seen as a horizontal grey line in (Fig. 4*d*), with the vertical contact pads remaining covered in gold to ensure a good electrical connection with the phase shifted lines. The exposed titanium was then

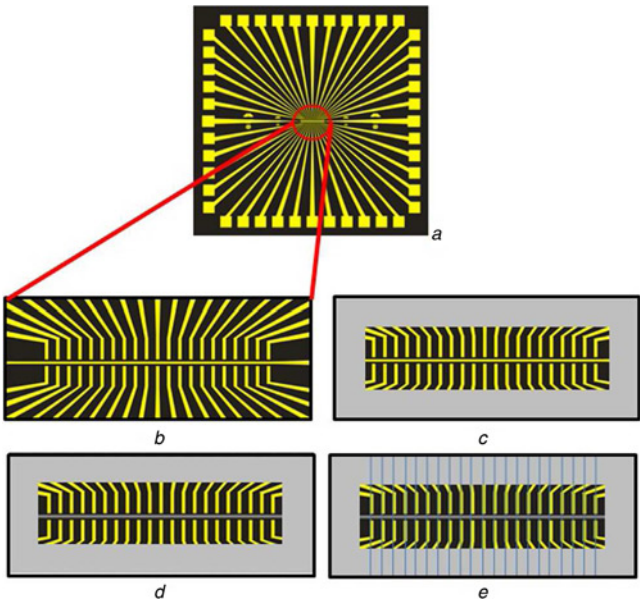

Figure 4 *Diode base layer in titanium and gold (Fig. 4a); close up of connectors for each diode (vertical lines) and common connection (horizontal line) (Fig. 4b); entire wafer covered in chromium (grey) leaving only the diode contact pad region exposed (Fig. 4c); common connector has the gold etched away leaving titanium exposed (dark grey), the vertical gold contact pads are protected here by photoresist, and are therefore not etched away (Fig. 4d); phase shifted lines over contacts and chromium (blue lines) (Fig. 4e). Chromium is then removed leaving vertical platinum PS lines in contact region only, preventing short circuits between the contact pads as they diverge*

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oxidised using a controlled reactive ion etch and plasma regrowth step, discussed in [9].

The PSL process was then used to provide vertical troughs in photoresist. SPR-350 photoresist, diluted to a 50% concentration with Microposit EC solvent, was then spun on the substrate (~400 nm thick) and the PDMS mask brought into conformal contact with the surface. Exposure to a low UV dose, followed by post-exposure bake and development resulted in narrow trough regions in the photoresist at every point where a height transition had occurred in the PDMS stamp. A dry etch (100 sccm O_2, 50 mT, 70 W for 10 s – RIE mode) was used to ensure any unwanted photoresist was fully removed from these regions. A 40 nm of platinum was then evaporated, resulting in a small Ti/TiOx/Pt region being produced (Fig. 4*e*). Finally, the chromium was removed, which also removed unwanted platinum, completing the diode fabrication process.

The phase shifted lines are positioned on the substrate only visually, which means the detailed alignment cannot occur. However, the design of the phase shifted line mask is such that the distance between each phase shift line is equal to the width of each contact pad, therefore there are multiple vertical phase shifted lines within the distance between consecutive vertical contact pads, and each contact pad must make contact with a phase shifted line. This ensures a connection between the phase shifted lines and the contact pads, despite having only visual alignment capabilities.

3. Results and discussion

3.1. Phase shift diodes – physical analysis: Using this technique, line widths in the range 200–400 nm can be achieved routinely. Fig. 5 shows images of PSL lines incorporated into diodes, with a 10 µm common connection (top left to bottom right) overlapped by PSL platinum lines (top right to bottom left), which have been shortened via the etching of a sacrificial chromium layer to prevent shorting. These images combined with electrical results show the process to be robust, with phase shifting still occurring at the interface of the existing steps' height for the contact pads.

Owing to the lift-off process, the edge roughness of the phase shifted lines would result in reduced yield if used as a base layer in diode production, which is why the PSL lines were used as the top layer, as then the edge profile of the platinum layer does not affect the functionality of the diodes. The yield of the diodes is limited by the ability to align the sub-micron lines with the contact pad and by the number of defects in those lines, neither of which have posed significant issues.

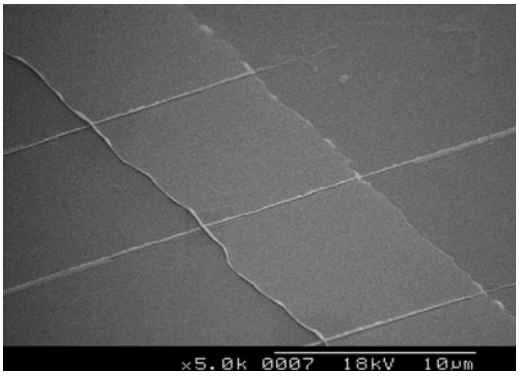

Figure 5 *Crossover of phase shift Ti–TiOx–Pt diode, with the wide common Ti/TiOx connection (top left to bottom right, seen as horizontal dark grey line in Figs. 4d and e) and the PSL Pt lines (top right to bottom left, thin vertical blue lines in Fig. 4e)*
Diode region is the crossover between the two

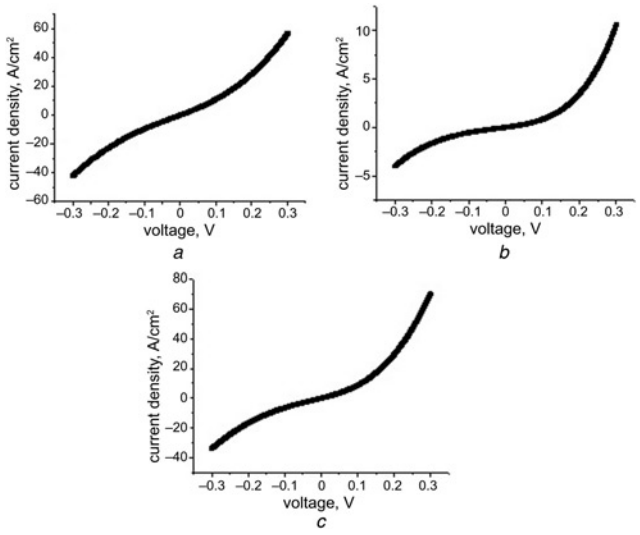

Figure 6 *Current density–voltage (J–V) characteristics of MOM diodes prepared with the following techniques and dimensions*
a Furnace oxidation, PSL, 0.4 µm × 9 µm
b Plasma oxidation, PSL, 0.4 µm × 9 µm
c Plasma oxidation, standard lithography, 9 µm × 9 µm

For future devices, a NIL tool could be used to align these imprint stamps more accurately, allowing multiple layers of PSL lines to be used in a single device. Control contact between the stamp and substrate could also be accurately controlled, thus improving the quality of the phase shift process and therefore the yield of the devices. Furthermore, this process could be used to produce sub-micron master stamps for standard NIL processing, which would provide a low cost, high speed method of fabricating sub-micron devices.

3.2. PSL furnace diodes: These devices were also successful electrically as diodes, as can be seen from a typical *J–V* graph in Fig. 6*a*. These diodes have a typical zero bias CC (CC_{ZB}) of 0.7 V^{-1}, a peak value of 1.34 V^{-1} and a forward to reverse current ratio of 1.4:1. These values compare favourably with results published by others [6, 10].

3.3. PSL plasma oxidation diodes: To improve yield as well as electrical characteristics, plasma oxidation of the titanium was applied to the phase shift diodes. Fig. 6*b* shows a typical *J–V* characteristic of a diode fabricated this way, with asymmetry and nonlinearity comparable with previous, larger diodes [8]. It has been found that a peak current density of 100 Acm^{-2} or smaller is consistent with a diode with good rectifying capabilities, as confirmed by the CC and forward to reverse current ratio. These diodes have a typical CC_{ZB} of 2.8 V^{-1}, a peak value of 4.1 V^{-1} and a forward to reverse current ratio of 2.6:1; all these values are improvements on the furnace oxidised diodes. The shrinkage of the device dimensions has not led to

Table 1 Summary of diode results

Oxide preparation	Size, µm	CC_{ZB}, V^{-1}	Oxide thickness, nm
4 h furnace 100% O_2	0.4 × 9	1.3	6.7
plasma 120 W 100% O_2	9 × 9	3.2	5.0
plasma 150 W 50% O_2	9 × 9	2.9	5.0
plasma 300 W 50% O_2	9 × 9	4.6	4.0
plasma 300 W	0.4 × 9	4.1	4.0

any noticeable degradation in diode performance. Fig. 6*c* shows a typical *J–V* of a plasma oxidised diode with larger dimensions prepared by standard lithography, and the corresponding diode performance figures are a typical CC_{ZB} of 3.3 V^{-1}, a peak value of 4.6 V^{-1} and a forward to reverse current ratio of 2.1:1. A summary of electrical results, together with the oxide thickness (measured by both TEM and ToFSIMS) and fabrication process, is given in Table 1.

A comparison of the current densities between the different diodes in Fig. 6 is worthy of note. Although the oxide thickness range is where competing conduction mechanisms could occur, the change in current density between diodes is unlikely to be because of this. The values in Fig. 6*a* (furnace oxide – 6.7 nm) and Fig. 6*c* (plasma oxide – 4.0 nm) are similar, yet the current density in Fig. 6*b* (also plasma oxide – 4.0 nm) is a factor 8 down in value. The reasons for this are still being investigated.

4. Conclusions: MOM diodes with sub-micron features and a controllable uniform oxide have been produced using novel plasma oxidation and PSL processes. The results have a high yield of high performance diodes, and this represents a significant step towards a mass manufacturable process for MOM diodes. The factor of 23 reduction in size from initial diode results will ensure an improved cutoff frequency, thus ensuring the potential for high speed operation. Furthermore, these diodes show competitive electrical results, confirming their asymmetry and nonlinearity.

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