Size-controllable fabrication of nano-to-microstructures on silicon surface using high-density ion etching with pulsed bias

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A 'black silicon' (BS) surface with low reflectance was fabricated by a standard pulsed deep reactive etching technology at room temperature. Aiming for a better understanding, a systematic experiment was conducted by varying the etching window size and bias power duty cycle. The samples were measured and analysed by a scanning electron microscope, the Bruker Optical Profiler and a UV-3400 spectrometer. It was observed that a broad scale range of the surface structures formed on the surface. With the duty cycle at 0.5, only about 100 nanometre scale replicable silicon cones formed on the surface, but as the duty cycle decreased to 0.25, the height of the silicon forest sharply increased to about 10 μm, leading to a low reflectance of 0.9% in the visible range for the surface. To clarify the reason for this trend, the bias effective voltage (BEV) was measured and it was confirmed that the BEV would decrease from 100 to 47 V with the duty cycle adjusted from 1 to 0.25. This suggested that this decrease in BEV leads to a reduction of ion energy and ion flux, and then modifies the fabricated structures. Besides, it was found that the broad etching window area only had a maximum promotion of 20% to the scale of the BS, indicating this method was almost free of loading effect.

1. Introduction: Nano-to-microstructures on silicon surfaces can bring about high specific surface areas [1] and low light reflectivity [2–7]. Thus, the surface morphology has become an important issue in the fabrication process of many optical, optoelectronic and biochemical devices, such as MEMS (micro-electromechanical systems) capacitors [3], solar cells [2, 4, 5] and infrared sensors [8]. In addition, an appropriate surface morphology is very important when the silicon acts as the feed layer for other materials [9]. Moreover, it is well accepted that devices with different sizes would have variable preferences over the fabricated surface structure scale and also demand huge diversity in the modification area. All this results in the need for an easy method to fabricate surface structures with a broad scale range and such a method needs to be free of size effect.

Three traditional approaches have been developed to fabricate nano-to-microstructures on a silicon surface: the femtosecond laser pulse [10–12], metal-assisted wet etching [6, 13] and inductively coupled plasma-reactive ion etching (ICP-RIE) [1, 3, 14]. ICP-RIE has a greater advantage in practical applications, in that it is free of metal ionic contamination and the control scheme is relatively easy, compared with the first two methods. In fact, the etching in ICP-RIE is mainly composed of physical sputtering and chemical reaction, which are directly determined by ionic energy and the density of ion flux into the substrate. In a Bosch process, under a certain ionic energy and flux density level, most of the silicon in the etching window would be removed, while few micromasks (SiO_2/Si) would be left on the surface after one etch cycle. Then these micromasks would be protected in the following passivation cycle and gradually accumulated through the whole process, finally leading to the 'black silicon' (BS) surface. Based on this fundamental mechanism, many previous studies have focused on the fabrication of the BS surface by ICP-RIE: Nguyen *et al.* [14] have investigated the influence of the flow ratio, substrate temperature and bias power on surface structures, whereas only a structure scale range of 500 nm–2 μm and a reflectance of about 1.5% in the visible range was obtained; Sainiemi *et al.* [7] have fabricated silicon surface structures with only a scale range of 500 nm–2 μm and a reflectance of about 0.1% in the wavelength of 200–500 nm at −120°C; Yue *et al.* [2] have introduced a mixed method of deep reactive-ion etching (DRIE) and wet chemical etching to fabricate BS surface structures with a scale range of 500 nm–1 μm and a reflectance of 5% in the visible range. These methods were in one-step; however, some extreme conditions, such as reverse bias power, cryogenic temperature and combination with wet chemical etching were required. In addition, it should be noted that the surface structure scale range is too narrow to meet the demands for all devices, such as MEMS capacitors and infrared sensors. Besides, most previous work only focused on applications in large-size devices, such as solar cells and the research process area was usually at mm^2. It is well known that the etching surface profile has a strong relationship with the amount of silicon exposed to the plasma (the so-called loading effect [15]), so the previous method is unlikely to have an efficient modification as the process area is narrowed to μm^2. Recently, some assumptions and simulations of bias pulsing in inductively coupled plasma etching have been carried out, proving an obvious advantage over decreasing plasma-induced damage and strengthening the control of surface profiles [16, 17]. However, only practical experiments about the influence of bias pulse duty cycle on etching rate were carried out, while the effect on specific surface profiles is still unknown.

The aim of the work reported in this Letter was to develop a novel method to fabricate the nano-to-microstructures on a silicon surface for application in small-to-large size devices. A commercial STS DRIE system was used to etch the monocrystal silicon wafers, to investigate the effect of bias pulse duty cycle and the etching area on the silicon surface profile. Through adjusting the experimental parameters, the fabricated BS surface scale can be easily varied from nano-to-micro. Moreover, the effect of the etching window area on the surface morphology has been revealed. Among the samples of this study, one with a low reflectance of about 0.9% in the visible range is obtained.

2. Experiment procedure: The side polished and (100)-oriented p-type monocrystalline silicon wafers with a size of 4 inches, thickness of 400 μm and resistivity of 2 Ω cm were used in our experiment. Initially, the wafers were cleaned with ethanol and deionised water and dried by nitrogen to remove adsorbed surface contamination. Then, the native oxide on the wafers was

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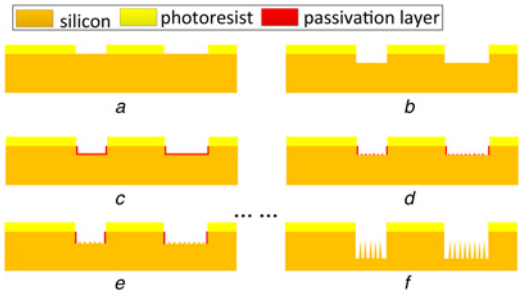

Figure 1 *Process scheme*
a Lithography to form etching window
b Shallow etching
c Passivation cycle
d Etching cycle with floated bias
e Etching cycle with full-power bias
f Final BS

eliminated by immersing into the HF solution (5 wt%) for 20 s. After that, all wafer samples were rinsed in deionised water and dried by nitrogen. Next, using lithography masks, the silicon wafers would form three different-scale etching windows on the surface. Thereafter, a standard Bosch DRIE process, with SF_6/O_2 etch gas and C_4F_8 passivation gas, was conducted at room temperature using a pulsed bias in the etching cycle on the sample wafers. The process scheme is illustrated in Fig. 1. Among the samples, the process parameters were kept the same in the passivation cycles. There were many process parameters in our experiments, but we only focus on the bias pulse duty cycle and etching window size. The fixed parameters for all samples were an etching time of 15 min, an ICP power of 600 W, a bias power of 140 W, a gas pressure of 15 mTorr, an O_2 gas flow rate of 19.5 sccm, an SF_6 gas flow rate of 130 sccm, a C_4F_8 gas flow rate of 100 sccm, bias pulse cycle duty at 1 in the passivation cycles, an etching period of 7 s and a passivation period of 2 s. The variable parameters are the bias pulse cycle duty in the etching cycles and the etching window size. These parameters are summarised in Table 1.

Surface morphological studies of the etched samples were performed using a scanning electron microscope (SEM). The precise surface roughness mean square (RMS) and particle scale were measured by the Bruker Optical Profiler. Besides, using a standard UV-3400 spectrometer with an integrating Ulbrich sphere, the reflectance of the samples was measured with nearly normal light incidence.

3. Results and discussion

3.1. Impact of etching window size on surface RMS and particle scale: It is well known that there is a strong relationship between the etching profile and etching window area in plasma etching. In our study, the effect of etching window size on the surface RMS

Table 1 Parameter scheme of DRIE process

Sample	Etching window area, μm^2	Duty cycle	Sample	Etching window area, μm^2	Duty cycle
1	100 × 100	1	9	25 × 25	0.5
2	50 × 50	1	10	100 × 100	0.35
3	25 × 25	1	11	50 × 50	0.35
4	100 × 100	0.75	12	25 × 25	0.35
5	50 × 50	0.75	13	100 × 100	0.25
6	25 × 25	0.75	14	50 × 50	0.25
7	100 × 100	0.5	15	25 × 25	0.25
8	50 × 50	0.5			

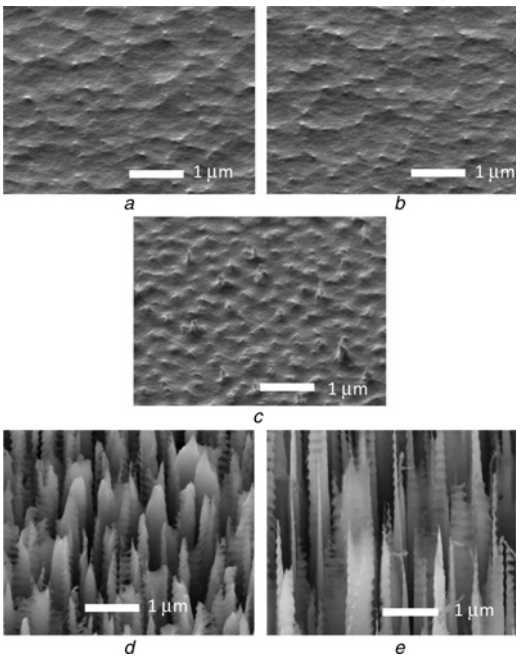

Figure 2 *Scanning electron micrographs for duty cycles of 1, 0.75, 0.5, 0.35 and 0.25*
a Duty cycle = 1
b Duty cycle = 0.75
c Duty cycle = 0.5
d Duty cycle = 0.35
e Duty cycle = 0.25
Etching window area is 100 μm × 100 μm for all above samples

and particle scale were investigated. Figs. 2–4 show the surface morphologies of mc-Si under different etching conditions. It is noted that no obvious difference could be observed among the surface textures when the etching window size varied from 25 μm × 25 μm to 100 μm × 100 μm. However, it can be seen from Figs. 4 and 5 that in most cases when the etching window broadened, the surface RMS slightly increased and the etching depth decreased. This increase of the RMS is explained as follows. When the etching window area increases, more silicon areas were exposed to the plasma and this results in quicker depletion of both bombardment ions and active radicals. As the etching window area broadens, the depletion rate increases to an

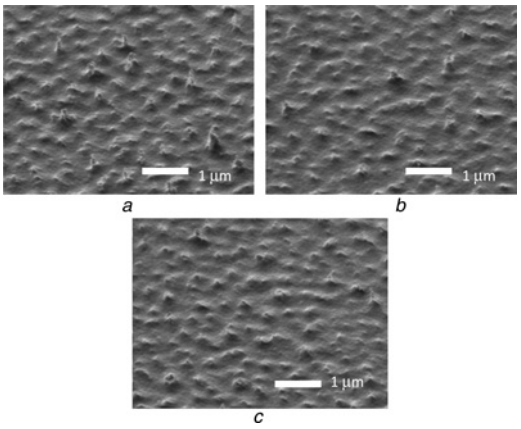

Figure 3 *SEM images showing morphological evolution of silicon wafer when duty cycle is 0.5 for etching window area at 100 μm × 100 μm, 50 μm × 50 μm and 25 μm × 25 μm*
a 100 μm × 100 μm
b 50 μm × 50 μm
c 25 μm × 25 μm

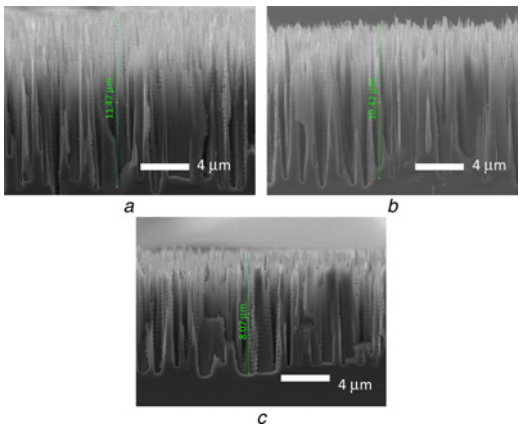

Figure 4 *SEM images with cross-sectional view of samples with etching window area at 100 μm × 100 μm, 50 μm × 50 μm and 25 μm × 25 μm when duty cycle is 0.25*
a 100 μm × 100 μm
b 50 μm × 50 μm
c 25 μm × 25 μm

extent, in which the depletion of ions and radicals would exceed the supply from the plasma source. Then, the number of ions that causes physical sputtering and the radicals which lead to chemical etching will decrease, both of which induced an increase of the micromasks. As a result, the surface will be rougher as the etching window broadens. Whereas, in all cases, the variation ratio did not exceed more than 20%, indicating that the etching window size is not a determinant in surface modification. On the basis of the experimental trend and theoretical analysis, it can be deduced that the BS surface will form when the etching window areas broaden to mm^2. This strongly supports this method being fit for multi-size device fabrication, since the scale effect is not crucial.

3.2. Impact of bias power cycle duty on surface RMS and particle scale: It is obvious from Figs. 2, 5 and 6 that the bias power duty cycle plays a key role in determining the surface morphology. When the cycle duty is adjusted from 1 to 0.5, the etching depth decreases from 20.42 to 13.99 μm and the surface RMS increases from 11.94 to 40.07 nm. Besides, the particle size increases from 33.9 to 141.3 nm. Moreover, with the cycle duty further decreasing from 0.5 to 0.25, the etching depth diminishes slightly from 13.99 to 9.75 μm, while the particle scale increases sharply from 141.3 nm to 10.42 μm. This phenomenon can be explained as follows: because the duty cycle determines the actual working time of the bias power, as can be seen from Fig. 5*b* the bias effective voltage (BEV) decreases with the reduction of the duty cycle. As in a previous study [18], a lower BEV would result in lower bombardment energy and a smaller ion flux density.

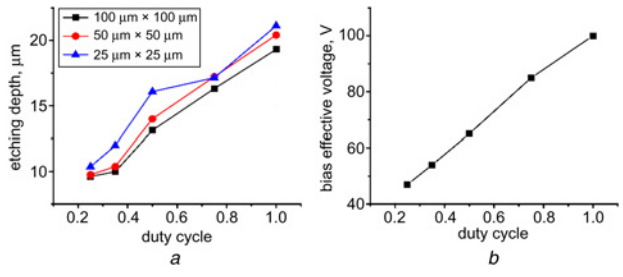

Figure 5 *Etching depth of samples for different window areas against duty cycle (Fig. 5a), and relationship between effective voltage and duty cycle (Fig. 5b)*

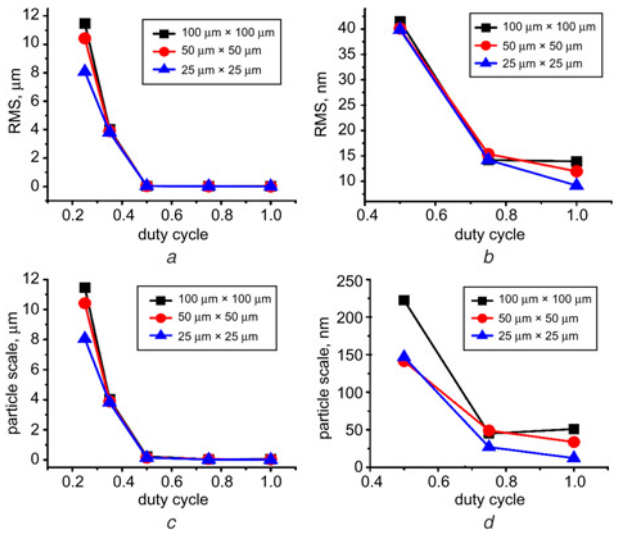

Figure 6 *Measured RMS (whole duty cycle range, Fig. 6a; details in range of 0.5–1, Fig. 6b) and variation between particle scale (whole duty cycle range, Fig. 6c; details in range of 0.5–1, Fig. 6d) of modified sample surfaces, measured by Bruker Optical Profiler when duty cycle above 0.5 and equal to particle height measured in SEM images when duty cycle below 0.5*

During the plasma etching process, the silicon surface reaction is mainly composed of physical sputtering (ion bombardment) and chemical etching (neutral radical reaction). First, the lower ion bombardment energy and smaller ion flux density would directly reduce the physical sputtering. Then, for the chemical etching, the collision between the ions and neutral molecules near the silicon surface would help to dissociate the molecules from the reactive radicals. Since the ion energy is reduced, the production of radicals near the surface would be also lowered. Besides, the lower ion bombardment energy would keep the silicon surface more integrated, leading to a decrease in the average radical incident angle. Thus, less reactive radicals could combine with the substrate to produce an etching reaction. In summary, the chemical etch would be decreased as well. The reduction of the etching capacity would decrease the smoothing rate for the surface relief and increase the surface micromask. Thus, the small bias power cycle duty results in a large surface RMS and particle scale. Besides, the dramatic changes of particle scale with the duty cycle passing 0.5 is because under this condition the effective bias power voltage has decreased to some degree that the quantity of micromasks left after one etch cycle is almost equal to the quantity of removed polymers and silicon. The density of the micromasks will be enough to trap reactive ions and the reaction product. That is, the transport will be limited and this will protect the BS structures from physical sputtering and chemical etching, while the formation of the BS will intensify the restriction of the transport in the feedback. As a result, when the duty cycle is past below 0.5, the particle scale will increase sharply.

3.3. Impact of surface profiles on optical reflectance: Fig. 7*a* summarises the major optical reflectance of samples with different bias duty cycles. Fig. 7*b* illustrates the reflectance of the samples with different etching window areas, while the duty cycle is fixed at 0.25. Although in the ultraviolet region from 0 to 500 nm there is almost no difference in the reflectance between the polished silicon and the etching samples with the duty cycle from 1 to 0.5, it is noted that in the visible and infrared region from 500 to 1050 nm all the treated samples have a decrease in reflectance compared with the polished silicon and the reflectance

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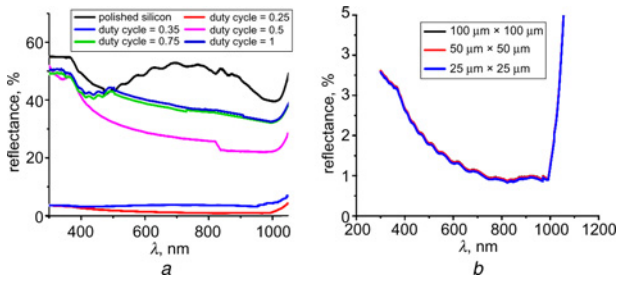

Figure 7 *Reflection spectra of modified Si surface with etching window area of 100 μm × 100 μm for different duty cycles (Fig. 7a), and reflection spectra of samples with duty cycle of 0.25 for different etching window areas (Fig. 7b)*

goes down with the decrease of the bias power duty cycle. In the visible range, the reflectance of the treated sample with the duty cycle at 0.25 is only about 0.9%. When the wavelength approaches 1050 nm the reflectance of all samples has a dramatic increase. It is observed that there is little difference among the reflectance as the etching window area ranges from 25 μm × 25 μm to 100 μm × 100 μm. Two mechanisms are employed to explain this which are that in the wavelength range of 300–1000 nm the reflectance deduction is mainly because of the intrinsic absorption by the substrate, and because of the formation of silicon spikes. The latter leads to multiple reflections of the incident light, resulting in a geometric light trapping. When the duty cycle drops, the size and density of the silicon spikes increase, intensifying light trapping, while the etching window size has a limited influence on these morphologies. In the wavelength range of 1000–1050 nm (close to the optical band gap of single-crystal silicon), the intrinsic absorption by the material, once constant in the wavelength range of 300–1000 nm, gradually weakened to zero. This is responsible for the dramatic increase of the reflectance.

4. Conclusion: The nano-to-microstructure can be easily controlled to form on the silicon surface in the DRIE process by adjusting only one parameter (the bias power pulse duty cycle). The size of the silicon cones created by our technique is in the nanometre range when the duty cycle is above 0.5 and will increase to the micrometre range when the duty cycle is below 0.5. The scale range, which would satisfy the requirement of most devices is amazing and is the broadest to the best of our knowledge. The nanosize surface modification, which is hardly fabricated in previous research, with a more solid relief, has the potential to be the feed layer for the 'forest' formation of other materials, such as carbon nanotubes. The microsize surface modification, with an approximate reflectance of 0.9% throughout the visible region, is promising for opto-biomedical applications. Besides, the influence of the etching area in our method is also revealed, indicating it is free of size limitation and has great potential in the application of small-size devices.

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