

Metallic tube-tolerant ternary dynamic content-addressable memory based on carbon nanotube transistors

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The design of a dynamic content-addressable memory (DCAM) cell using carbon nanotube (CNT) field effect transistors is explored. A four CNTFET design is presented and the functionality of a ternary DCAM cell using SPICE simulation is verified. Using an array of asymmetrically correlated tube technique, it is demonstrated how the presented design could be made functional even in the presence of metallic CNTs.

1. Introduction and related work: Transistors built using carbon nanotube field effect transistors (CNTFETs) have been demonstrated by a number of researchers to have electrical properties that make them particularly attractive to be the replacement of current silicon-based devices. Researchers have demonstrated that CNTFETs can be designed with metal-oxide-semiconductor (MOS) transistor type characteristics, where a doped nanotube forms the channel through which the majority carriers move from drain to source under the influence of an electric field from the gate [1]. Researchers have also shown that CNTFETs can be manufactured to have tunable properties such that they can be configured to work as n-type or p-type at runtime by modulating the thickness of the Schottky barrier [2]. Using these two styles of CNTFETs, a number of designers have proposed circuits for memory elements [3–5], as well as for multi-valued computations [6]. In this Letter, we explore further how dynamic content addressable memory (DCAM) can be created for both binary/ternary storage of data using CNTFETs.

Unlike other memory architectures (e.g. random access memory (RAM), read only memory etc.), the content-addressable memory accesses the memory stack based on the data rather than the address [7]. It allows for a parallel search operation on the memory stack in addition to the read/write operations. This ability to perform searches in parallel makes it popular in applications ranging from pattern matching to cache controllers, among many others. Each memory cell or bit of the content-addressable memory (CAM) storage includes a comparison logic providing the user with the ability to read, write or search for a data word in the memory and generate a match/mismatch signal and/or the address of the matching data. If the data store/compare involves strictly logic 0 and 1, then the cell is called a binary CAM (BCAM). If an additional storage of ‘don’t care’ value is allowed to enable masking of partial search data then the cell is called a ternary CAM (TCAM). A traditional CAM structure is shown in Fig. 1.

Data are written to the storage cell consisting of the cross-coupled inverter pair through the access transistors N1, N2. During search operation, the matchline (ML) is first pre-charged high to logic 1 and then allowed to be evaluated. During the evaluation phase, based on the arrangement of transistors N3–N6, if the data stored at node D matches the data on the search line (SL), there is no direct path for the ML to discharge to ground, causing the line to stay in the high logic state indicating a match. A mismatch is indicated by the ML falling to logic low. If a TCAM cell is desired, the same configuration as shown in Fig. 1 is used for the search operation but the data is stored in two distinct cells resulting in a larger 16-transistor design.

Although the static storage-based cell shown in Fig. 1 has numerous advantages such as larger noise margins and better data retention, dynamic storage of data would significantly reduce the number of transistors needed and hence make the cells suitable for large datatable applications [8].

In [9], the authors demonstrated a ternary dynamic CAM cell design using four N-type transistors. The design is shown in Fig. 2. The design consists of two access transistors (N1, N2) gated by a Write signal. When Write = 1, the value from the bitlines (BL and $\overline{\text{BL}}$) are passed onto storage nodes D1 and D0, respectively. D1 and D0 are dynamic nodes created from the gate capacitance of transistors N3 and N4. A storage of {0, 1} on {D1, D0} indicates a storage of ‘logic 0’ in the cell. Similarly, {1, 0} indicates a storage of ‘logic 1’ and {0, 0} indicates the ‘don’t care’ logic. When a search for data is performed, the Write signal is set to 0, and the data is compared between the BL and the storage node. As in a traditional BCAM cell, the ML is first pre-charged high and then allowed to evaluate. A match causes the ML to stay at logic 1, while a mismatch changes the state of the line to logic 0.

The four-transistor design shown in Fig. 2 is a huge improvement in terms of area over a traditional 16-transistor TCAM design. However, a direct connection of the ML to the node between transistors N3 and N4 introduced ML coupling causing larger leakage and incorrect mismatches. The MLs could be decoupled by introducing a transistor-implemented diode [8] or using the numerous techniques presented in [10]. The numerous designs presented in [10] require a total of 6–11 transistors, thereby shrinking the advantage of using a dynamic over a static one. The authors of [11] presented a DCAM design with a decoupled ML and presented a modified sensing scheme to address inherent data retention problems suffered by DCAMs in general. However, the design focuses on a binary DCAM cell, thereby limiting the type of data that can be searched for in the CAM array.

2. Ternary DCAM – design and simulations: In this Section, we present a ternary DCAM design inspired by the BCAM design with the decoupled ML scheme of [11]. Consider the circuit shown in Fig. 3. The circuit consists of four CNTFETs (three n-type and one p-type). The Wordline is connected to the gate of CNTFET N2 allowing the storage of data from the data line (DL) to the internal node DATA when Wordline = 1. Similar to the circuit of Fig. 2, the search operation takes place when Wordline = 0. To place logic 0 on the DATA node of the cell, the Wordline is set to 1, and the DL is pulled low to ground; similarly, to place logic 1 on the node, the DL is pulled to VDD (high) when the Wordline is 1. The DCAM also stores a ‘don’t care’ state (‘logic X’) in the form of a voltage equivalent to half of VDD. To

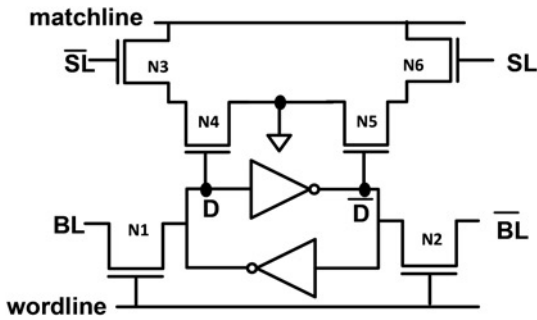


Figure 1 Traditional ten-transistor binary CAM cell

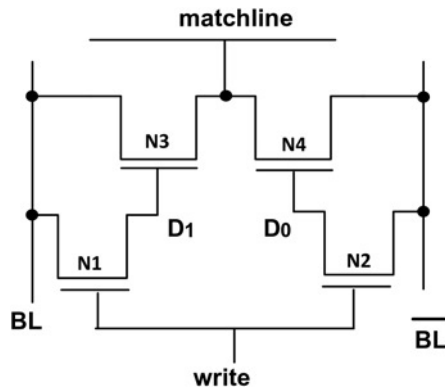


Figure 2 Four-transistor ternary DCAM cell design from [9]

accomplish this, the DL is held at half of VDD and the Wordline is set to 1. During all Write cycles, the \overline{DL} signal is held low.

Transistors N1 and P1 have a threshold voltage of 0.55 V and -0.55 V, respectively, and are created with tubes with chiral vector (10, 0) while N2 and N3 have threshold voltages of 0.29 V and are created with tubes with chiral vector (19, 0). The higher threshold voltage of P1 and N1 is important to ensure that when a 'don't care' value is stored at data in the form of half of VDD (0.45 V), both P1 and N1 are off, leaving node $t2$ floating at a low value and thereby preventing the ML from falling low. This ensures that regardless of what is being searched ('logic 1' or 'logic 0') on the data lines (DL and \overline{DL}), the DCAM cell will always indicate a match when a 'don't care' logic is stored in the cell. Recall that a high value on the ML signifies a match while a low value indicates a mismatch. The overall functionality of the circuit can be as summarised in Table 1.

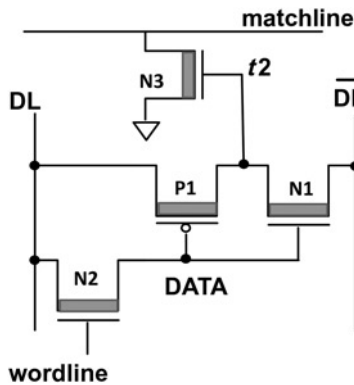


Figure 3 Decoupled ML ternary DCAM

Table 1 Logical operation of the proposed DCAM cell

	WL	DL	\overline{DL}	Stored data	ML	Event
write data	1	0	0	0	not used	write 0 to cell
	1	1	0	1	not used	write 1 to cell
	1	X	0	X	not used	write 'don't care' to cell
search data	0	0	1	0	1	data searched matches with stored data
	0	1	0	0	0	mismatch
	0	0	1	1	0	mismatch
	0	1	0	1	1	data searched matches with stored data
	0	0	1	X	1	data searched matches stored value of 'don't care'
	0	1	0	X	1	data searched matches stored value of 'don't care'
	0	1	0	X	1	data searched matches stored value of 'don't care'

Using SPICE models presented in [12], the DCAM circuit was simulated at room temperature with a power supply (VDD) of 0.9 V. Fig. 4 shows the SPICE simulation results for the DCAM; the ML pre-charge clock (CLK), Wordline, input data lines (DL and \overline{DL}) and the ML are shown. The ML pre-charge CLK is a signal that gates a p-type transistor whose source is connected to VDD and the drain to the ML. When the CLK is low, the ML is pulled or pre-charged to 0.9 V. When the CLK is high, the pre-charge transistor is OFF and the ML is allowed to evaluate. In Fig. 4, during the first 4 ns, the CLK signal is high pre-charging the ML to logic 1; the WL is high and the DL is 0 allowing for the storage of logic 0 on the DATA node. From 4 to 9 ns, a data search for logic 0 is performed by placing 0 V on DL and 0.9 V on \overline{DL} ; since the data being searched matches the data stored at node DATA, the ML stays high. The data are refreshed from 9 to 10 ns and the CLK is held low to pre-charge the ML before its next evaluation between 10 and 14 ns. During this timeframe, the data being searched is a logic 1 ((DL = 0.9 V and \overline{DL} = 0 V). This causes the ML to fall to logic 0 since the searched value (0.9 V) does not match the stored value on DATA (0.0 V). We

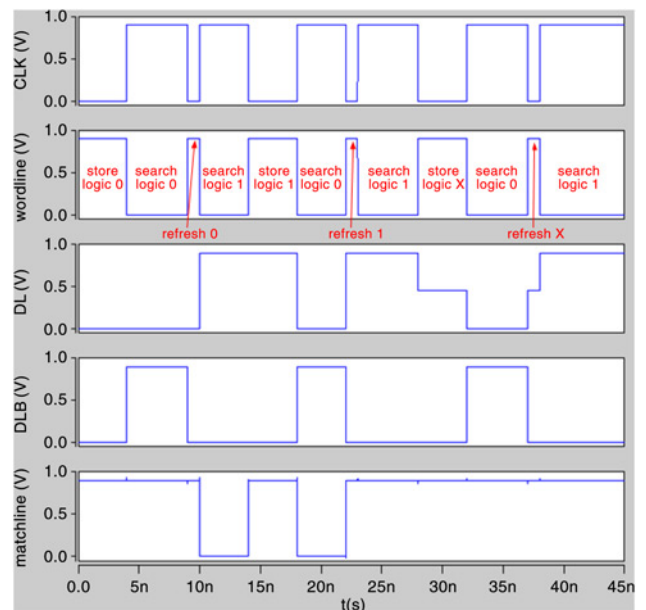


Figure 4 Simulation results for the DCAM cell

Table 2 Comparison with 16 nm CMOS ternary CAM cell

	Proposed DCAM	16 nm CMOS TCAM
number of cells per bit	1	16
number of transistors	4	10
search operation, ps	17.5	23.6
average power, μW	0.24	1.14

repeat this process with the storage of logic 1 in the DATA node followed by a search of logic 0 and 1, respectively, between 14 and 28 ns. At 28 ns, a ‘don’t care’ is stored by placing 0.45 V on the DL. Since a don’t care is stored on the node, we expect that the search for a logic 0 (32–37 ns) or logic 1 (38–45 ns) will result in a match. This is accomplished by using higher threshold transistors for P1 and N1 as mentioned earlier. Fig. 4 confirms that the DCAM cell is fully functional as a ‘ternary’ cell.

On the basis of the simulation, the total time taken for the ML to completely discharge during a mismatch is 6.8 ps and the total time for a data search is 17.5 ps. The average power consumption for the cell including the pre-charge and the keeper transistors for ML leakage prevention was found to be 0.24 μW and the total energy consumption for the cell was 1.76 fJ.

Table 2 compares the search time and average power with a design based on 16 nm CMOS process. The CMOS TCAM uses the traditional design where two SRAM cells are used for storage of each ternary bit. We can see that the proposed DCAM is small, fast and power efficient compared with the CMOS design.

Process variation (e.g. threshold, diameter, tube alignment etc.) is an important consideration for circuits and architectures based on CNTFETs. Since this Letter deals with the circuit and architecture of the memory cell, we have assumed that the parallel alignment of carbon nanotubes (CNTs) can be achieved during manufacturing as described in previous works [13–15]. We also simulated the circuit of Fig. 3 to see how it would behave with a $\pm 10\%$ variation of the threshold voltages (due to variation in chiral vectors). Similar to the results described in [3–5], we found that the circuit was able to tolerate the $\pm 10\%$ process variation.

3. DCAM cells in the presence of metallic tubes: A typical batch of CNTs was reported to contain about 33% metallic tubes [16]. While excellent for use as interconnects, a metallic tube is undesirable in a CNTFET circuit since it acts as a short between two nodes causing excessive leakage and severe noise margin degradation. A number of approaches exist that have been suggested for improvements in the yield of semiconducting tubes. Using a preferential growth technique that favours semiconducting tubes, fast heating and plasma-enhanced chemical vapour depositions, the metallic tubes can be reduced to about 4% of the batch [17].

The presence of metallic tubes can cause significant deterioration of the noise margin or match failures in a CAM. Using an array of asymmetrically correlated carbon nanotubes (ACCNT) technique described in [18] our design can be made tolerant to the remaining metallic tubes. Using the ACCNT approach, we utilise statistically ‘uncorrelated’ CNTs in series to lower the probability of non-functional transistors and statistically ‘correlated’ tubes in parallel to improve the current drive.

Consider a design where the probability that the CNT is semiconducting is given by P_{semi} . One or more tubes (N tubes) are used to create a CNTFET, so the probability of getting a semiconducting CNTFET is $P_{\text{FET}} = (P_{\text{semi}})^N$. Let us place J number of statistically uncorrelated tubes in series whose gates are all connected to the same input signal. Since all of these uncorrelated transistors are connected to the same gate, the series network will behave as a semiconducting transistor as long as at least one of the CNTs is

Table 3 Probability of producing a functional DCAM cell using the design of Fig. 3 given the probability of producing a semiconducting tube (P_{semi}) and using an array of J correlated CNTs in series

		P_{semi}				
		0.80	0.90	0.95	0.98	0.99
number of uncorrelated series CNTFETs, J	1	0.410	0.656	0.815	0.922	0.961
	2	0.849	0.961	0.990	0.998	1.000
	3	0.968	0.996	1.000	1.000	1.000
	4	0.994	1.000	1.000	1.000	1.000
	5	0.999	1.000	1.000	1.000	1.000
	6	1.000	1.000	1.000	1.000	1.000

semiconducting; this probability is represented as

$$P_{\text{series}} = 1 - (1 - P_{\text{FET}})^J = 1 - (1 - (P_{\text{semi}})^N)^J$$

To maintain the current drive, we need to have a number of these ‘series’ CNTs in parallel; let us place K number of series CNTs in parallel. If the parallel CNTFETs were uncorrelated we would get the probability that the CNTFET is fully functional even in the presence of metallic nanotubes ($P_{\text{ACCNT_CNTFET}}$) as

$$P_{\text{ACCNT_CNTFET}} = (P_{\text{series}})^K$$

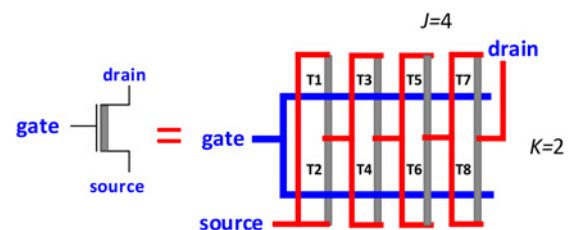
The overall probability remains unaffected when the transistors placed in parallel are statistically correlated [17] and we obtain $P_{\text{ACCNT_CNTFET}}$ as

$$P_{\text{ACCNT_CNTFET}} = (P_{\text{series}})^1 = 1 - (1 - (P_{\text{semi}})^N)^J$$

Using this approach, we can evaluate our design of Fig. 3 and compute the overall probability that the DCAM cell is functional given a certain probability of finding a metallic tube in a batch of tubes used to create an individual transistor. The DCAM design involves the use of a total of four CNTFETs. The overall probability of a fully functional DCAM cell can then be written as the product of each of these probabilities

$$P_{\text{ACCNT_DCAM}} = P_{\text{FET}}(P1) \times P_{\text{FET}}(N1) \times P_{\text{FET}}(N2) \times P_{\text{FET}}(N3)$$

Table 3 shows the probability of a functional DCAM ($P_{\text{ACCNT_DCAM}}$) cell given a specific value of P_{semi} as we increase the number of uncorrelated transistors in series from 1 to 6. For this analysis, we kept the number of parallel sections (K) to 2. We can see that as the CNTFET manufacturing gets better and is able to yield lower metallic tubes in a batch, the number of series connections (J) can be reduced. Until then, a design with 3 or 4 ‘uncorrelated series tubes’ for each transistor shown in Fig. 3 can be used to provide high yield.

**Figure 5** Functional transistor using the ACCNT technique with four series uncorrelated ($J = 4$) and two sets of parallel rows ($K = 2$)

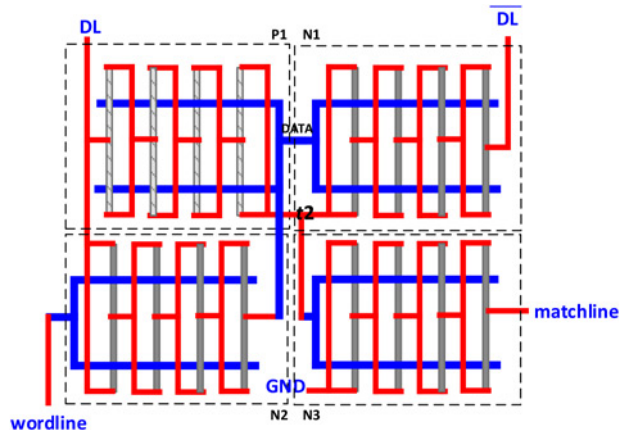


Figure 6 Layout of metallic-CNT-tolerant DCAM cell using ACCNT approach

Here the number of uncorrelated series tubes (J)=4 and the number of correlated parallel tubes (K)=2

Fig. 5 illustrates one possible ACCNT-based series/parallel stack of a single ACCNT transistor. The Figure shows four tubes in series set in a parallel configuration of two sets. In Fig. 5, T1 and T2 are in parallel. Similarly, other parallel pairs are: T3 and T4, T5 and T6, T7 and T8. The pair {T1–T2} is in series with {T3–T4}, {T5–T6} and {T7–T8}. As per the ACCNT approach, the parallel tubes are correlated (they are made from the same tube) while the series ones are uncorrelated creating a single metallic tube-tolerant functional ACCNT transistor. Using this general scheme, we show one possible layout for the DCAM circuit in Fig. 6. Each transistor that makes up the DCAM circuit of Fig. 3 is represented by four uncorrelated series tubes and two parallel groups of correlated tubes. In the layout, CNTs (grey) are shown in a vertical configuration gated by a metallic gate (blue). The same tube is used to form the two parallel transistors making the formation of correlated transistors easier. This approach to designing with ACCNT transistors has been shown by the authors of [16] to be tolerant to any metallic tubes on the transistor.

4. Conclusion: In this Letter, we have presented a DCAM cell capable of ternary logic storage using four CNT transistors (CNTFETs). We have shown using SPICE simulation that our design is functional. We have also shown a possible layout to make our design reliable in the presence of metallic tubes using an array of the ACCNT approach. On the basis of our analysis, using four series uncorrelated transistors and a set of two parallel correlated tubes to form the transistor we can achieve a fully functional DCAM with 99.4% confidence even in the presence of

20% metallic tubes and can achieve 100% functionality if only 10% of the tubes are metallic.

5 References

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