High-accuracy silicon-on-insulator accelerometer with an increased yield rate

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This Letter presents a high accuracy silicon-on-insulator (SOI) capacitive accelerometer using a backside dry release process. To increase the yield rate of the process, the deep reactive iron etching (DRIE) process was improved using a grooved accompany wafer to balance the pressure inside the back cavity of the SOI devices. By using this method, almost all the devices after the DRIE will not crack. Thus, the yield rate is significantly increased. Furthermore, the DRIE process was improved by dividing the DRIE process into four stages to decrease the tilt angle of DRIE. It is experimentally demonstrated that the tilt angle of the side wall was decreased from 0.81° to 0.27° and the loss of the capacitive sensitivity caused by the error was decreased from 28 to 8%. Test results show that sensitivity, bias stability, and noise floor of the accelerometer is 3.1 V/g, 16 μg, and 3.1 μg/$\sqrt{\text{Hz}}$, respectively.

1. Introduction: In recent years, microaccelerometers are widely used in various fields such as automobiles, consumer electronics, navigation, and guidance systems due to their small size, low cost, and low power consumption advantages [1–3]. However, how to realise the high accuracy using the common processes still remains as a big challenge. To obtain the high accuracy, the sensitivity should be enhanced and the noise should be lowered. The most straightforward way is to increase the inertial mass by either increasing the thickness or area of the proof mass. However, such methods will increase the difficulty of the fabrication and sharply decrease the yield rate.

For example, by significantly increasing the mass to 38 mg via keeping the full thickness of the silicon-on-insulator (SOI) wafer including the handle layer and the device layer [4], the noise floor can be reduced to 213 ng/$\sqrt{\text{Hz}}$ and the sensitivity is increased to 105 V/g. However, in such a 100 μm-thick device, to ensure the capacitance large enough, a thin low-pressure chemical vapour deposition oxide layer and a polysilicon layer are deposited to narrow the gap of the capacitors. It makes the fabrication process complex and hard to be realised. On the contrary, for a 40 μm-thick device, the gap of the capacitors can be fabricated small enough without complex process, for example 1.6–2.0 μm [5]. However, the noise floor is only 20 μg/$\sqrt{\text{Hz}}$ and the sensitivity is 0.5 V/g due to its small mass of 1.2 mg. From these two examples, it becomes obvious that for a large proof mass design the gap of the capacitors is a key design parameter and the corresponding etching process becomes very important.

In our previous work, we set the thickness of the device layer to 60 μm and the area to 5600 μm × 3800 μm, thus the mass is increased to 3 mg. A noise floor of 20 μg/$\sqrt{\text{Hz}}$ and a sensitivity of 2.5 V/g are obtained using a closed-loop analogue circuit [6]. However, the yield rate is only around 19.2% based on the standard SOI process. The major cause of the low-yield rate lies in that the device layer is easily cracked during the deep reactive iron etching (DRIE) process. The device layer may be cracked at a certain point because the stress in the proof mass increases with the enlarged mass area. Moreover, there is a pressure difference between the inside and outside of the device chamber during the DRIE process which makes the device layer much easier to be cracked.

We presented an improved DRIE process using a grooved accompany wafer (GAW) to balance the pressure difference, and the mass can be increased to 3.5 mg [7]. However, another serious problem will appear in the long-time DRIE process. That is the side wall of the comb fingers is not strictly in parallel with each other. Therefore, a tilt angle of the side wall is generated in DRIE process. In recent years, many studies have already been performed to realise a small tilt angle of microstructure via adjusting DRIE operational parameters, including etch cycle time, passivation cycle time, platen power, coil power, temperature of substrate cooling, and chamber pressure [8–11]. However, they involve a large number of experiments to optimise DRIE process recipes for specific structure. Therefore, such processes are time consuming. In this Letter, in addition to a detailed description of the improved DRIE process [7], we furthermore present a simple but effective optimisation of the DRIE process by sectioning it into four stages to reduce the tilt angle. The small tilt angle will bring more capacitance, which is very helpful to increase the accuracy of the accelerometer. The tilt angle of the side wall can be reduced from 0.81° to 0.27°. The noise floor is successfully reduced to 3.1 μg/$\sqrt{\text{Hz}}$.

2. Accelerometer design: The schematic of the presented in-plane SOI capacitive differential accelerometer is shown in Fig. 1. It consists of sensing capacitors, feedback capacitors, proof mass, and supporting folded beams. The fixed comb fingers, fabricated on device layer of the SOI wafer, are anchored to the substrate layer, while the movable comb fingers rest on the proof mass. The proof mass implemented on the device layer of the SOI wafer is anchored to the substrate layer by four-folded elastic beams. There are two sets of sensing capacitors (C_{sa+} and C_{sb+}, C_{sa-} and C_{sb-}) and two sets of feedback capacitors (C_{fa+} and C_{fb+}, C_{fa-} and C_{fb-}), respectively. The nominal gap of the capacitors C_{sa+}, C_{sa-}, C_{fa+}, and C_{fa-} is 4.2 μm while the gap of the capacitors C_{sb+}, C_{sb-}, C_{fb+}, and C_{fb-} is 21 μm.

The proof mass will move along the sensing direction (y-direction) with external acceleration applied, which leads to a change in the sensing and feedback capacitors combs' gap. Therefore, the displacement of proof mass is converted into a capacitance change by the differential parallel capacitors C_s top (C_{sa+}, C_{sb+}) and C_s bottom (C_{sa-}, C_{sb-}). The feedback excitation voltage acts on the differential feedback capacitors C_f top (C_{fa-}, C_{fb-}) and C_f bottom (C_{fa+}, C_{fb+}), which causes a feedback electrostatic force to balance inertial force of the proof mass.

The sensitivity (S) is a key design parameter of the differential accelerometer. If the actual cross-section of comb fingers is the same as the ideal cross-section (Fig. 2*b*), the sensitivity can be

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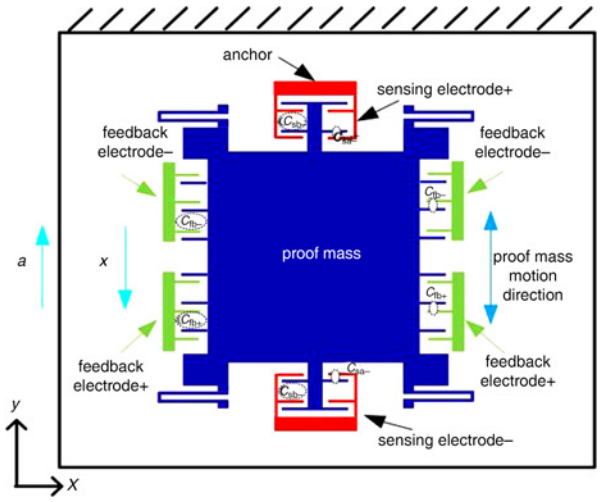


Fig. 1 *Schematic of the SOI differential accelerometer*

expressed by

$$S = \frac{\Delta C}{a} = \frac{N_s \varepsilon l h}{d_a^2 \omega_n^2} - \frac{N_s \varepsilon l h}{d_b^2 \omega_n^2} = \frac{N_s C_{sa}}{d_a \omega_n^2} - \frac{N_s C_{sb}}{d_b \omega_n^2} = \frac{N_s C_{sa}}{d_a \omega_n^2}\left(1 - \frac{1}{\eta^2}\right) \tag{1}$$

where N_S is the total number of the sensing electrodes, with the overlapping length of l, the height of h, the initial gap of d_a and d_b; ε is the permittivity of air; ΔC is the capacitance change; C_{sa} is the capacitance of unit cell; $\boldsymbol{a}$ is the acceleration, and η is defined as d_b/d_a. In this design, η is 5, which indicates that C_{sb} makes a very small contribution for the sensitivity.

However, the actual cross-section of the fabricated accelerometer is depicted in Fig. 2*c*. The electrode plates become non-parallel due to the tilt angle caused by DRIE process. Therefore, the capacitance between electrode changes leads to the actual sensitivity decrease from the designed value.

The capacitance (C'_{sa} and C'_{sb}) of the non-parallel plate capacitors (Fig. 2*c*) can be expressed as [12]

$$C'_{sa} = \frac{\varepsilon l}{2\alpha} \ln\left(\frac{d_2}{d_1}\right), \quad C'_{sb} = \frac{\varepsilon l}{2\alpha} \ln\left(\frac{d_4}{d_3}\right) \tag{2}$$

where α is the tilt angle, d_2 and d_4 are the bigger gap distances, and d_1 and d_3 are the smaller gap distances.

When the proof mass is in the equilibrium position, both C'_{sa+} and C'_{sa-} are equal to C'_{sa}, while both C'_{sb+} and C'_{sb-} are equal to C'_{sb}. If there is an acceleration along the sensing direction, the proof mass generates a corresponding displacement Δd which can be written as $\Delta d = \boldsymbol{a}/\omega_n^2$. The actual capacitive sensitivity (S_{act}) can then be expressed by

$$\begin{aligned} S_{act} &= \frac{\Delta C'}{a} = \frac{N_s}{2a}\left[\left(C'_{sa+} + C'_{sb+}\right) - \left(C'_{sa-} + C'_{sb-}\right)\right] \\ &= \frac{N_s \varepsilon l}{4a\alpha} \ln\left(\frac{d_2 - \Delta d}{d_1 - \Delta d}\frac{d_1 + \Delta d}{d_2 + \Delta d}\frac{d_4 + \Delta d}{d_3 + \Delta d}\frac{d_3 - \Delta d}{d_4 - \Delta d}\right) \end{aligned} \tag{3}$$

The final designed specifications of the accelerometer are shown in Table 1.

3. Fabrication process: The fabrication process of the accelerometer only requires two masks, that is the device layer mask and the handle layer mask. The SOI process flow is demonstrated in Fig. 3. The thickness of the device layer, handle layer, and oxide layer is 60, 400, and 4 μm, respectively.

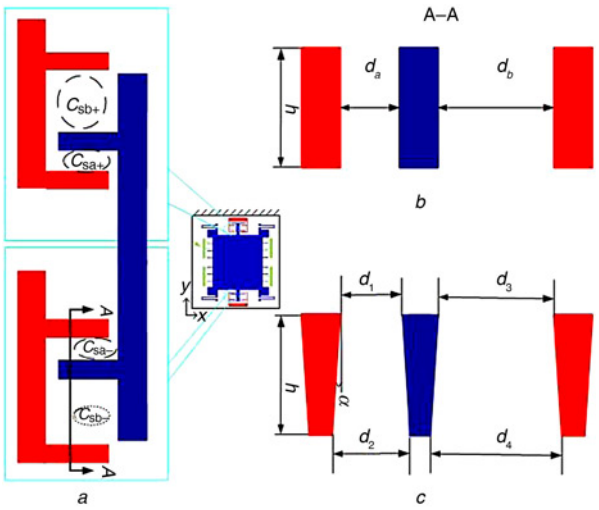


Fig. 2 *Cross-section of the comb fingers*
a Schematic of the differential capacitor
b Ideal cross-section of the comb fingers
c Actual cross-section of the comb fingers with a tilt angle

The most critical step in the process is the DRIE process. First, a 200 nm aluminium (Al) film layer is patterned to form the mask of the back cavity (Fig. 3*a*). Using this mask, the back cavity is formed by the first DRIE (Fig. 3*b*). Then Al film and the oxide layer are etched in Al enchant solution and hydrofluoric acid solutions, respectively (Fig. 3*c*). After back cavity formation on the handle layer, the major structures of the sensor need to be fabricated on the device layer. The second 200 nm Al support film is sputtered to act as the heat transfer layer during the second DRIE (Fig. 3*d*). Then device layer of the SOI wafer is patterned and glue the SOI wafer to the GAW (Fig. 3*e*). Finally, the device layer of the SOI wafer is etched by the second DRIE to define structures (Fig. 3*f*), and the residual photoresist is cleaned by oxygen plasma. The Al support layer is etched off by Al etchant solution to release the movable structure (Fig. 3*g*).

In the above process flow, the key process step is using a GAW to balance the pressure difference (Figs. 3*e* and 4*b*). The paraffin is chosen as an adhesive when gluing the devices to the GAW. The thickness of the adhesive is smaller than depth of the groove of the GAW. Therefore, the air between the device layer and the GAW can flow freely through the groove while pumping vacuum, which makes that the pressure inside the back cavity is equal to that of the chamber. Thus, the device layer will not crack (Figs. 4*b* and 5) as compared with the previous process (Figs. 4*a* and 6). We have fabricated nearly 110 devices, almost all devices after the DRIE will not crack any more. Thus the yield rate is greatly increased.

The top view of the fabricated accelerometer is shown in Fig. 7*a*. The back view of the fabricated accelerometer is shown in Fig. 7*b*. The view of the comb fingers is shown in Fig. 7*c*. The

Table 1 Specifications of the accelerometer

thickness of the device layer	60 μm
area of the proof mass	5060 μm × 4720 μm
overall sensor size	1.56 mm^2
proof mass	3.5 mg
capacitive gap	4.2 μm
spring stiffness	36 N/m
resonant frequency	500 Hz
mechanical noise	150 ng/$\sqrt{Hz}$
capacitive sensitivity	1.55 pf/g

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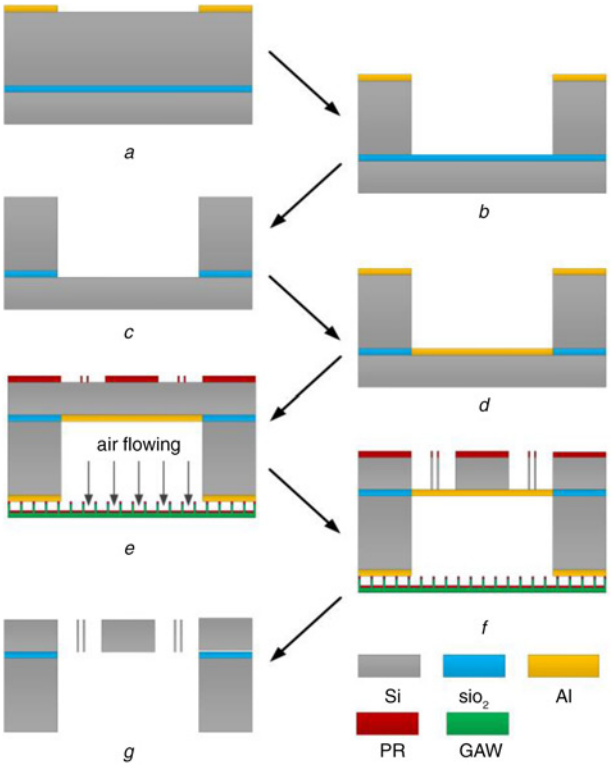


Fig. 3 *Fabrication process of the SOI accelerometer*
a Al pattering
b First DRIE for back cavity
c Al wet etching
d Al sputtering
e Gluing the SOI wafer to the GAW and lithography
f Second DRIE to define structures
g Oxygen plasma cleaning and Al wet etching for releasing the movable structures

close-up view of the gap is shown in Fig. 7*d*. It is clearly seen that the gap of the fabricated comb finger is 4.35 μm, which shows a good agreement with the design value (4.2 μm).

However, owing to the tilt angle caused by DRIE process, the side walls of comb fingers are not strictly consistent with the designed parallel ones. It causes the electrode plates of the capacitor to be non-parallel to each other and decreases the sensitivity further. The actual gap of the comb fingers is shown in Fig. 8. The top gap is 4.19 μm and the bottom gap is 4.76 μm, so it is easy to know that the tilt angle is 0.81°. Using (3), the capacitance sensitivity of the accelerometer is 1.12 pf/g and decreases by 28% compared with the ideal condition. Although the sensitivity formula for the non-parallel cross-section is defined by the logarithmic function (3), it has a good linearity for the acceleration in the range from −1 to 1 g (Fig. 10).

To decrease the tilt angle, the temperature of the chamber in DRIE needs to be lowered [9]. In our previous etching process,

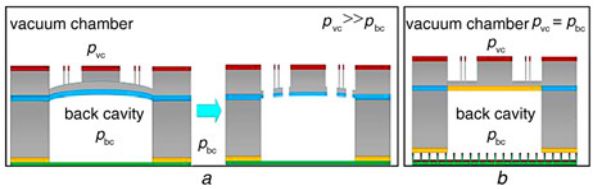


Fig. 4 *Wafer is cracked by the pressure difference between vacuum chamber (p_{vc}) and back cavity (p_{bc})*
a Device cracking due to the pressure difference
b No cracking when using the GAW

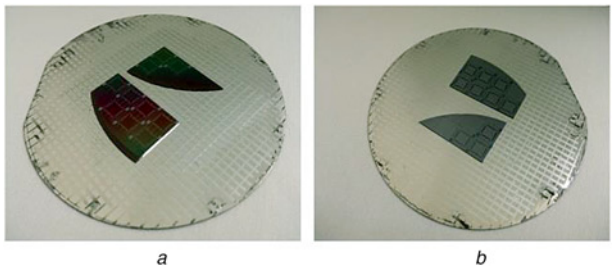


Fig. 5 *Results of the second DRIE process with the GAW*
a Devices glued to GAW before DRIE
b Devices with no cracking after DRIE and oxygen plasma cleaning

the devices were etched for 30 min continuously using DRIE. Heat accumulation of such a long-time DRIE would result in rising of the chamber temperature, which deteriorates the tilt angle. Therefore, we propose to divide the long-time DRIE into several short-time DRIEs and leave some time interval between

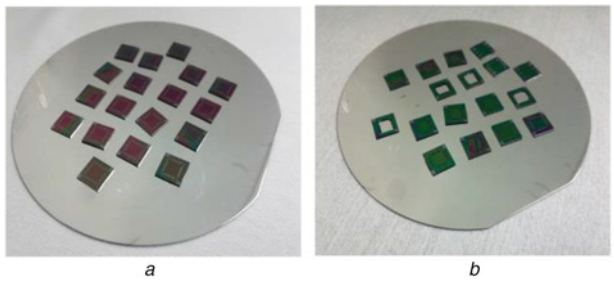


Fig. 6 *Results of the second DRIE without the GAW*
a Devices glued to the wafer before DRIE
b Devices cracking after DRIE

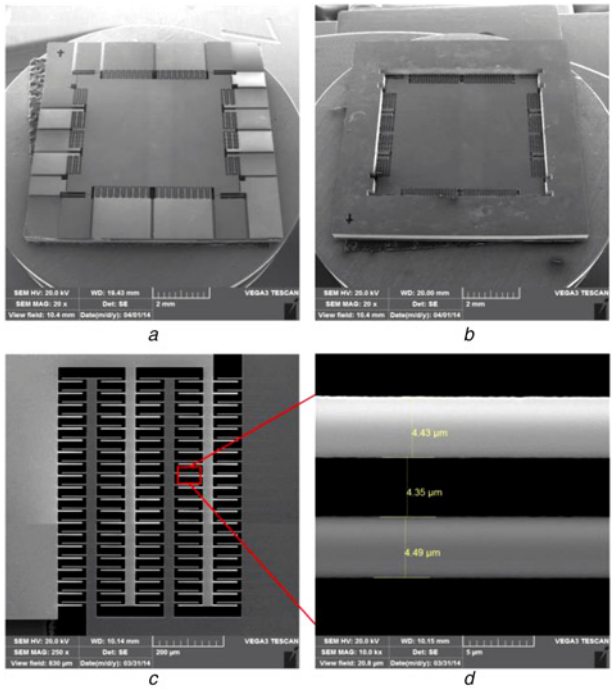


Fig. 7 *SEM view of the fabricated accelerometer*
a Top view of the accelerometer
b Back view of the accelerometer
c SEM image of the comb fingers
d Close-up view of the comb fingers with measured size

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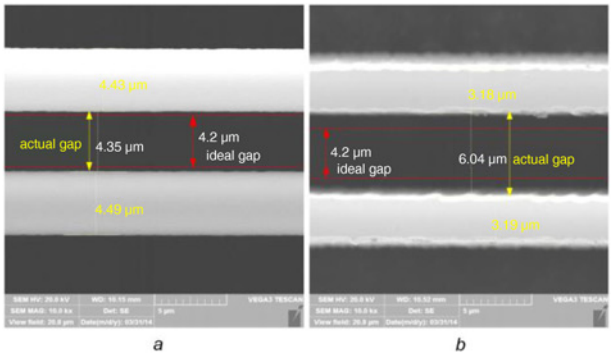


Fig. 8 *SEM views after a 30 min DRIE*
a Top view of the gap between the two comb fingers
b Bottom view of the gap between the two comb fingers

them. For example, the 30 min DRIE is divided into a 20 min DRIE and a 10 min DRIE with a pause of 15 min between the two sub-DRIE steps. We tried three different combinations of etching time during the DRIE to mitigate the heat accumulation. The experimental results are shown in Table 2. The corresponding sensitivity is shown in Fig. 10. It can be seen that the more sub-short DRIEs are, the smaller the tilt angle is. Currently, the smallest tilt angle is 0.27° (Fig. 9), and its sensitivity is improved to 1.44 pf/g, while the loss of sensitivity is decreased to 8% (Figs. 9 and 10).

4. Measurement results and discussion: The digital closed-loop circuit of the accelerometer includes a charge amplifier, gain control, sampling holder, proportion integration differentiation controller, low-pass filter, carrier wave, and a sequential controller (Fig. 11).

The SOI accelerometer was packaged and tested at normal atmospheric pressure and at room temperature (Fig. 12). The sensitivity, bias stability, and noise floor of the accelerometer and the interface circuit are measured. The accelerometer is mounted on

Table 2 Experimental result (DRIE methods versus tilt angle)

DRIE methods				Tilt angle, deg
No.	Number of sub-DRIEs	Time of sub-DRIEs, min	Time interval between two sub-DRIEs, min	
1	1	30	15	0.81
2	2	20 10	15	0.55
3	4	7	15	0.27

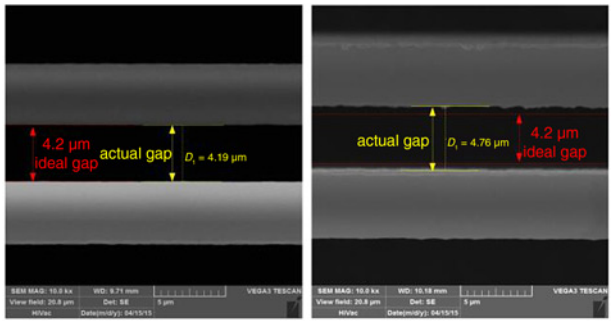


Fig. 9 *SEM views when DRIE process is divided into four stages*
a Top view of the gap between the two comb fingers
b Bottom view of the gap between the two comb fingers

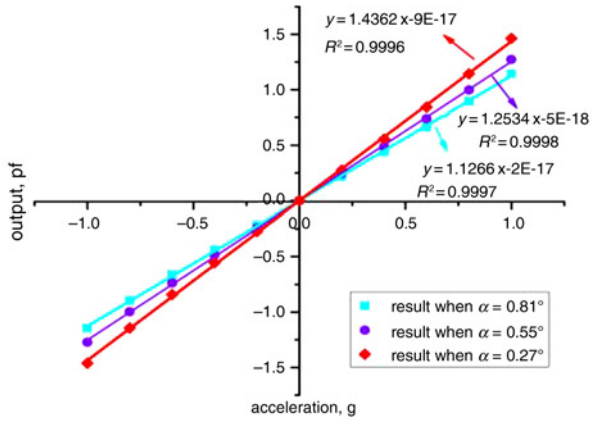


Fig. 10 *Calculated sensitivity of the accelerometer (the cyan line with square symbol corresponds to the tilt angle of 0.81°, the violet line with circle symbol corresponds to the tilt angle of 0.55°, and the red line with diamond corresponds to the tilt angle of 0.27°)*

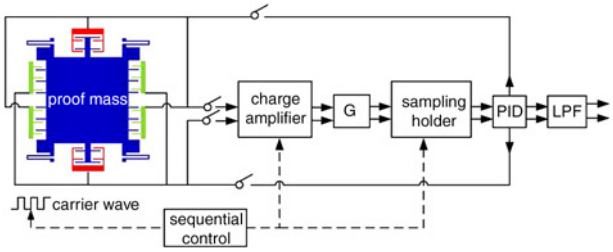


Fig. 11 *Block diagram of the digital closed-loop circuit*

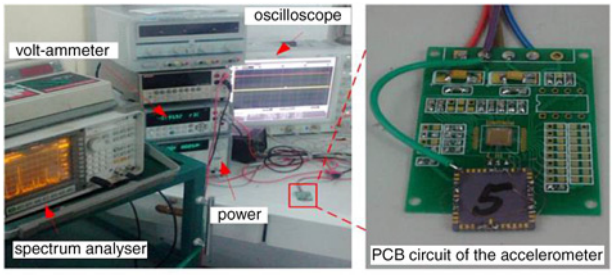


Fig. 12 *Test system setup including a spectrum analyser, a power source, a volt ammeter, an oscilloscope, and a PCB circuit of the accelerometer*

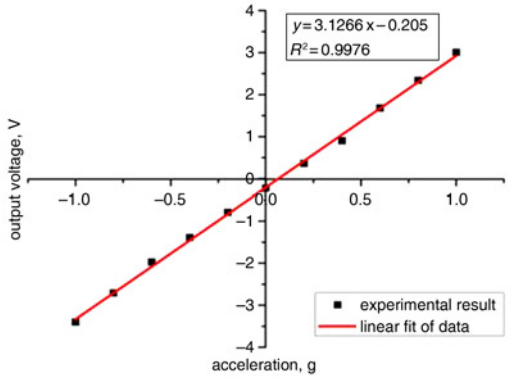


Fig. 13 *Measured sensitivity of the accelerometer*

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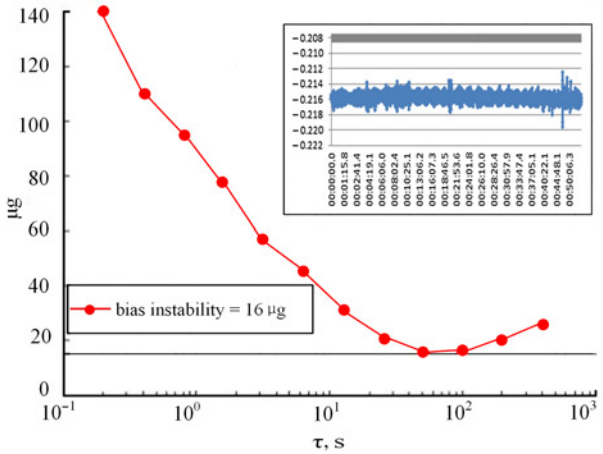


Fig. 14 *Measured bias stability based on Allan variance for 1 h*

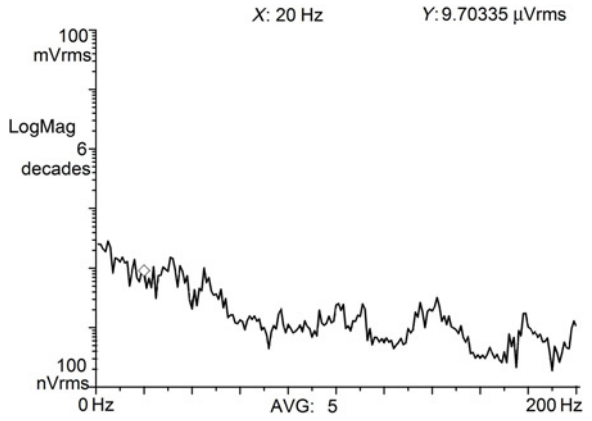


Fig. 15 *Noise floor of the accelerometer*

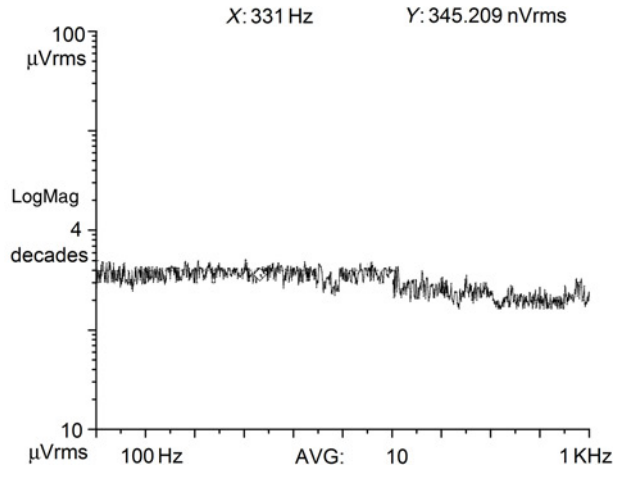


Fig. 16 *Noise floor of the digital closed-loop circuit*

the dividing head to perform gravity field measurement tests. The accelerometer is used to acquire data in the range from −1 to 1 g at an interval of 0.2 g. As shown in Fig. 13, the measured sensitivity is 3.1 V/g. The zero acceleration output of the digital closed-loop circuit is sampled every 200 min for a period of nearly 1 h. The measured data and the calculated Allan variance plot are demonstrated in Fig. 14, which indicates the accelerometer has a bias stability of 16 μg. The power spectral density of noise is 9.70 μV/$\sqrt{\text{Hz}}$ as shown in Fig. 15, which corresponds to a noise floor of 3.10 μg/$\sqrt{\text{Hz}}$. The noise floor of the digital closed-loop circuit alone is shown in Fig. 16. The power spectral density of noise is 345 nV/$\sqrt{\text{Hz}}$, which corresponds to a noise floor of 110 ng/$\sqrt{\text{Hz}}$.

The performance comparison of this work with previous published works is shown in Table 3.

As shown in Table 3, the accelerometer presented in this Letter achieves a high accuracy, which benefits from the large proof mass.

Table 3 Performance comparison of this work with previous published works

	Bias stability, μg	Noise floor, μg/$\sqrt{\text{Hz}}$	Sensitivity, V/g	Proof mass, mg
[4]	8	0.213	105	38
[6]	NA	20	2.5	3.0
[13]	66.1	24.7	NA	0.38
[14]	NA	157	0.0634	NG
[15]	NA	1100	0.38	0.15
this work	16	3.1	3.1	3.5

5. Conclusions: In this Letter, an SOI capacitive accelerometer with high accuracy and increased yield rate is designed, fabricated, and tested. The GAW is proved very effective to solve the crack problem of the device layer during the DRIE, which significantly improved the yield rate. Furthermore, by sectioning the DRIE process into four stages, the tilt angle of the comb fingers is greatly decreased. Based on these improvements, a high-accuracy accelerometer with a low-noise floor of 3.10 μg/$\sqrt{\text{Hz}}$ is realised.

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