Design and investigation of double gate Schottky barrier MOSFET using gate engineering

Sumit Kale, P.N. Kondekar

Department of Electronics and Communication Engineering, PDPM Indian Institute of Information Technology, Design and Manufacturing, Jabalpur 482005, India
E-mail: sumit.kale@iiitdmj.ac.in

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For the first time, a distinctive approach to design and investigate double-gate Schottky Barrier MOSFET (DG SB-MOSFET) using gate engineering is reported. Three isolated gates (one Control gate and two *N*-gates) of different work-functions on both sides of the gate oxides have been used. In the proposed device, without the need of doping, *n*-type region is formed at the source/drain contact-channel interfaces by inducing electron in the ultrathin intrinsic silicon channel using appropriate work-function metal *N*-gates. Using *N*-gates, the Schottky barrier height and tunnelling barrier width have been modulated to enhance the carrier injection similar to conventional dopant segregated (DS) SB-MOSFET. Moreover, the proposed DG SB-MOSFET behaves such as a conventional DS SB-MOSFET. The proposed device is expected to be free from variability caused by random dopant fluctuations. Furthermore, it offers simplified process flow with relaxing the need of doping to form dopant segregation layer and increased immunity to device variability.

1. Introduction: Over the past decade, as continued dimensional scaling approaches to 22-nm technology node, Schottky barrier (SB) MOSFETs have gained renewed interest as an attractive candidate for future high performance CMOS ICs [1–3]. SB-MOSFETs offer the inherent advantages such as immunity to short channel effects, low source/drain (S/D) parasitic resistances and scalability to sub-10 nm gate length dimensions [4, 5]. In SB-MOSFETs, ultra shallow junctions with low resistivity can be easily formed using metal S/D in place of doped S/D. However, in this device, due to existence of intrinsic SB present at the S/D contact-channel interfaces, the low drive current is a major challenge to be overcome. In the past, a lot of efforts have been made to enhance the on-state performance of the conventional SB-MOSFETs, by using critical new channel materials, including Si, Ge, III–V compound semiconductors (InAs, InP, GaN etc.) and low Schottky barrier height (SBH) metal silicides ($ErSi_{2-x}$, $YbSi_{2-x}$, $DySi_{2-x}$, and PtSi etc.) [6–8]. Recently, effective barrier height engineering using dopant segregation during silicidation has been widely adopted by the various research groups to improve the electrical characteristics of the device [9, 10]. In dopant segregation, a thin highly doped layer is formed at the S/D contact-channel interfaces, which enhances the tunnelling probability of carriers owing to strong band bending. However, introducing dopants to modify the effective SBH, results device variability caused by discrete random dopant fluctuations (RDF) [11, 12]. Due to the discrete dopants position, variability in SB profile is observed, which influences the tunnelling current of the device. Moreover, as device dimensions goes below 10–20 nm node with ultrathin silicon channel, this discrete RDF strongly influenced DC as well as high frequency performance and shows more variability than the doped S/D devices [11, 13]. In conventional dopant segregated (DS) SB-MOSFET variability is mainly due to RDF and process induced fluctuations. Hence, to overcome the aforementioned issues, in this Letter, we propose and investigate a distinctive approach to modify effective SBH and the tunnelling barrier width. By using two additional *N*-gates, without introducing dopants in the proposed double-gate Schottky Barrier MOSFET (DG SB-MOSFET), we obtained similar behaviour and identical DC performance to the conventional DS SB-MOSFET. The proposed DG SB-MOSFET is expected to be free from variability caused by RDF and requires low thermal budget with elimination of doping.

2. Device structure and simulation: The cross sectional view of conventional DS SB-MOSFET and the proposed DG SB-MOSFET is shown in Figs. 1*a* and *b*, respectively. The device parameters for the conventional double gate DS SB-MOSFET used in simulations are: intrinsic silicon channel concentration $(n_i) = 1 \times 10^{15}\,\text{cm}^{-3}$, silicon channel thickness $(T_{Si}) = 10$ nm, gate oxide thickness $(T_{ox}) = 1$ nm, control-gate length $(L_g) = 20$ nm, control-gate work function $\Phi_m = 4.7$ eV, control gate underlap length $(L_{un}) = 2$ nm, dopant segregation layer (DSL) length $(L_{dsl}) = 5$ nm and *n*-type doping concentration of DSL $(N_{dsl}) = 1 \times 10^{19}\,\text{cm}^{-3}$. The SBH $\Phi_b = 0.25$ eV is considered for both the devices for fair comparison. The SBH (Φ_b) is calculated as $\Phi_b = \Phi_m - \chi_{Si}$, where Φ_m is S/D metal work function Φ_m and χ_{Si} is the electron affinity of silicon [14]. Here, we have taken work function of 4.42 eV to form Schottky S/D contacts in both the devices. The electron affinity (χ_{Si}) of silicon is considered as 4.17 eV [15–17]. The simulation parameters for the proposed DG SB-MOSFET is same as mentioned above, except for inducing n-region on the intrinsic silicon channel close to S/D contact-channel interface to modify effective SBH and tunnelling barrier width, two additional gates named as *N*-gates are employed. Therefore, for maintaining induced carrier distribution uniform beneath the *N*-gates, silicon film thickness has to be kept within the Debye length, that is

$$L_D = \sqrt{(\epsilon_{Si} V_T)/(qN)} \tag{1}$$

where ϵ_{Si} is the dielectric constant of silicon, V_T is the thermal voltage, and N is the carrier concentration in the Si channel [16]. The spacer oxide thickness (L_{sp}) between the control-gate and two *N*-gates is taken as 2 nm for isolation, similar to L_{un} used in conventional DS SB-MOSFET. In proposed DG SB-MOSFET, the *N*-gates length $(L_{n\text{-gate}})$ is chosen 5 nm same as L_{dsl} to maintain induced effective thermal equilibrium carrier concentration similar in both the devices. The *N*-gates having metal work function of 3.9 eV, corresponds to metal hafnium is

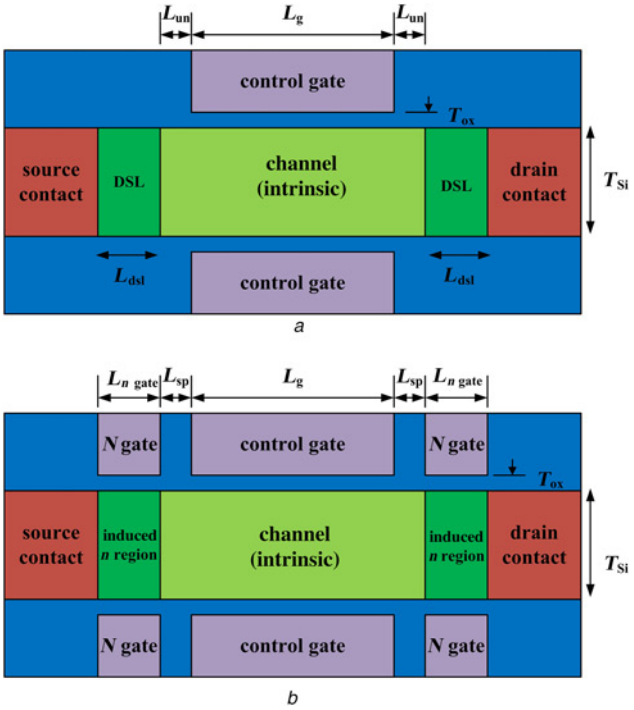

Fig. 1 *Cross sectional view of*
a Conventional DS SB-MOSFET
b Proposed DG SB-MOSFET

considered for simulation. The basic idea applied here for proposed device is to convert the intrinsic channel region in to a (*n*-*i*-*n*) region without doping, similar to conventional DS SB-MOSFET, where *n*-region corresponds to DSL at source side, *i*-region corresponds to intrinsic channel and another n-region corresponds to DSL at drain side. Therefore, we eliminate the requirement of doping to form highly doped layer (*n*-type) at the S/D contact channel interface. Using this approach, we effectively modulate the effective SBH and tunnelling barrier width for electron transport over and through the large and thin SB. To accurate calculations of thermionic and tunnelling current extensive simulations have been performed using Silvaco Atlas 2D device simulator [15]. For tunnelling current estimation, universal Schottky tunnelling model is used, where probability of charge carrier is calculated by assuming a triangular barrier using Wentzel–Kramer–Brillouin (WKB) approximation [18]. We also considered drift-diffusion current transport model in the simulations. The mobility effects are included in simulations using concentration dependent and field dependent mobility models. The SBH lowering effects are considered using image force barrier lowering model. We have calibrated simulation model parameters by reproducing published results reported in [9].

3. Results and discussion: Under thermal equilibrium ($V_{GS} = V_{DS} = 0$), electron and hole concentration along the horizontal cut lines from the centre of the channel are shown in Fig. 2*a*. It is clearly observed that at thermal equilibrium the induced electron concentrations are similar in proposed DG SB-MOSFET and conventional DS SB-MOSFET, which corresponds to (*n*-*i*-*n*) region. The reason is, employing metal (for *N*-gates) having low work function than the silicon channel of high work function, results electrons begins to accumulate beneath the *N*-Gates and form the induced *n*-region [17]. Although, in both the devices, to form Schottky S/D contacts with SBH of 0.25 eV, we have taken higher work function of about 4.42 eV. Hence, work function difference is created between S/D metal and *N*-gates. As a result, induced effective thermal equilibrium electron concentration in

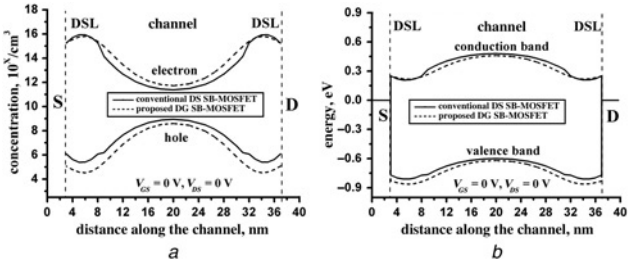

Fig. 2 *For conventional DS SB-MOSFET and proposed DG SB-MOSFET*
a Thermal equilibrium electron and hole concentration
b Thermal equilibrium energy band diagram

proposed DG SB-MOSFET is less than the doping concentration of DSL region. This is due to the fact that employing high work function metal to form S/D contact reduces the electron accumulation near the S/D contact-channel interfaces region, due to depletion is occurred in this region. Similarly, in conventional DS SB-MOSFET thermal equilibrium electron and hole concentration is less than the actual doping of DSL region. Fig. 2*b* shows the thermal equilibrium energy-band diagram of both the devices. It is observed from the figure that the conduction band and valence band of both the devices is following the same trend, which shows the similar behaviour of proposed DG SB-MOSFET with the conventional DS SB-MOSFET. Furthermore, we also observed that employing N-gates modify the conduction band edge at S/D contact-channel interface in proposed device similar to conventional DS SB-MOSFET. Therefore, in this state due to large and thick SB of height 0.25 eV, the carrier injection over and through the barrier is restricted ideally. Although, due to thermal emission of carrier over the barrier leakage current flow in the device.

Fig. 3*a* shows the on-state ($V_{GS} = V_{DS} = 1$), electron and hole concentration distribution along the horizontal cut lines from centre of the channel. It is observed that at $V_{GS} = V_{DS} = 1$, the electron concentration along the channel increases and corresponds as *n*-type channel region. The on-state electron and hole concentration distribution of proposed DG SB-MOSFET resembles the conventional DS SB-MOSFET. The on-state energy band diagram is shown in Fig. 3*b*. From this figure, we note that by applying positive bias on control gate the conduction band edge of both the devices shifts downward due to band bending, which increases tunnelling probability of electrons, results from reduction in effective tunnelling barrier width. In proposed structure, we effectively modified the tunnelling barrier width and SBH for electron injection at S/D contacts-channel interface similar to conventional DS SB-MOSFET. Fig. 4 demonstrates the transfer characteristics of conventional SB-MOSFET, conventional DS SB-MOSFET and the proposed DG SB-MOSFET. The proposed DG SB-MOSFET has similar DC characteristics to conventional DS SB-MOSFET. It is observed that conventional DS SB-MOSFET and proposed

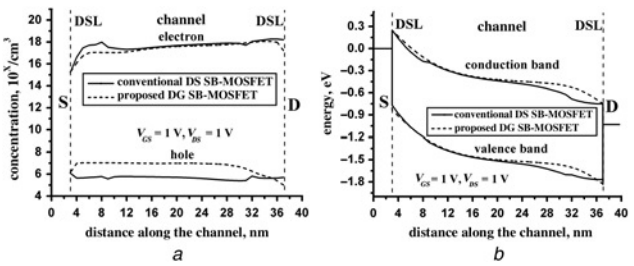

Fig. 3 *For conventional DS SB-MOSFET and proposed DG SB-MOSFET*
a On-state electron and hole concentration
b On-state energy band diagram

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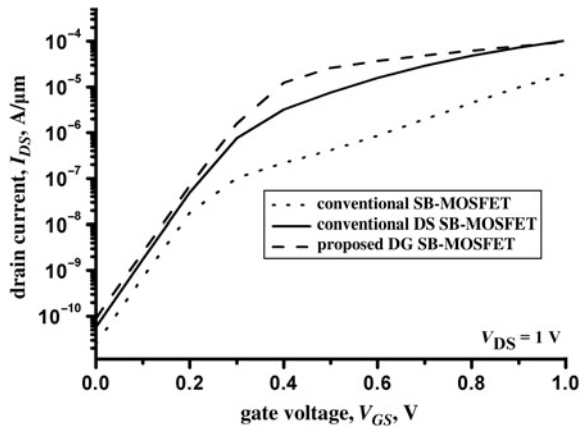

Fig. 4 *Transfer characteristics of conventional SB-MOSFET, conventional DS SB-MOSFET having only control-gate and proposed DG SB-MOSFET having control-gate and two additional gate (N-gates) with work-function of 3.9 eV*

DG SB-MOSFET achieve the approximately identical on-state current of about 1.03×10^{-4} A/μm and 9.73×10^{-5} A/μm respectively, at $V_{GS} = 1.0$ V and $V_{DS} = 1.0$ V. For $V_{DS} = 1.0$ V and $V_{GS} = 0$ V, the off-state current of the proposed DG SB-MOSFET is as low as 8.87×10^{-11} A/μm. Furthermore, the subthreshold swing (SS) of proposed DG SB-MOSFET is found to be 69 mV/decade and is same as for the conventional DS SB-MOSFET. Moreover, both the devices have the similar on to off current ratio (I_{ON}/I_{OFF}) of about $\sim 10^5$. However, the conventional SB-MOSFET has inferior performance as compared with the proposed DG SB-MOSFET in terms of low on-state current of 1.94×10^{-5} A/μm, high SS of 70 mV/decade and low I_{ON}/I_{OFF} less than 10^5.

To analyse the effect of *N*-gate work function on device performance of the proposed DG SB-MOSFET, we have considered five different values of *N*-gate work function as 3.9, 4.1, 4.3, 4.5 and 4.7 eV. The on-state energy band diagram at centre of the channel of the proposed DG SB-MOSFET with different *N*-gate work function is shown in Fig. 5*a*. In the on-state, as *N*-gate work function increases, the tunnelling barrier width for electron injection at the source side SB increases, leading to a reduction in on-state tunnelling probability. For *N*-gate having low work function of 3.9 eV, the tunnelling barrier width is narrower than the tunnelling barrier width of *N*-gate having high work function. Therefore, the on-state tunnelling probability is large for *N*-gate having low work function of 3.9 eV, which results in increased on-state current. The off-state energy band diagram at centre of the channel of the proposed DG SB-MOSFET with different *N*-gate work function is shown in Fig. 5*b*. In the off-state, the increase in *N*-gate work function reduces the tunnelling barrier width for hole injection at the drain side SB, which results increased off-state tunnelling probability [19]. As a result, for increasing *N*-gate work function off-state current of the device increases. However, in proposed device by employing *N*-gate having low work function of 3.9 eV, the off-state current is significantly minimised. Fig. 6 shows the transfer characteristics of the proposed DG SB-MOSFET as *N*-gate work function is varied from 3.9 to 4.7 eV. As expected, it can be observed that with increasing *N*-gate work function the on-state current (at $V_{GS} = 1.0$ V and $V_{DS} = 1.0$ V) of the device reduces. In addition, for increasing *N*-gate work function the SS of the device is also increases. The off-state current (at $V_{GS} = 0$ V and $V_{DS} = 1.0$ V) is higher for *N*-gate having high work function. However, in the proposed device, by considering *N*-gate work function of 3.9 eV, we achieve high on-state current, low off-state current, and low SS as compared with *N*-gate having high work function.

We now investigate the effect of *N*-gate length of the proposed DG SB-MOSFET on device performance, for this purpose, we have chosen *N*-gate length as 5, 7, 9, 11 and 13 nm with 2 nm spacer oxide thickness between control gate and *N*-gates. The transfer characteristics of the proposed DG SB-MOSFET with different values of *N*-gate length are shown in Fig. 7. It can be seen from the figure that variation in *N*-gate length does not make much difference on device performance. However, for low value of *N*-gate length, we obtained higher on-state current than the high value of *N*-gate length. As *N*-gate length increases, the separation between source

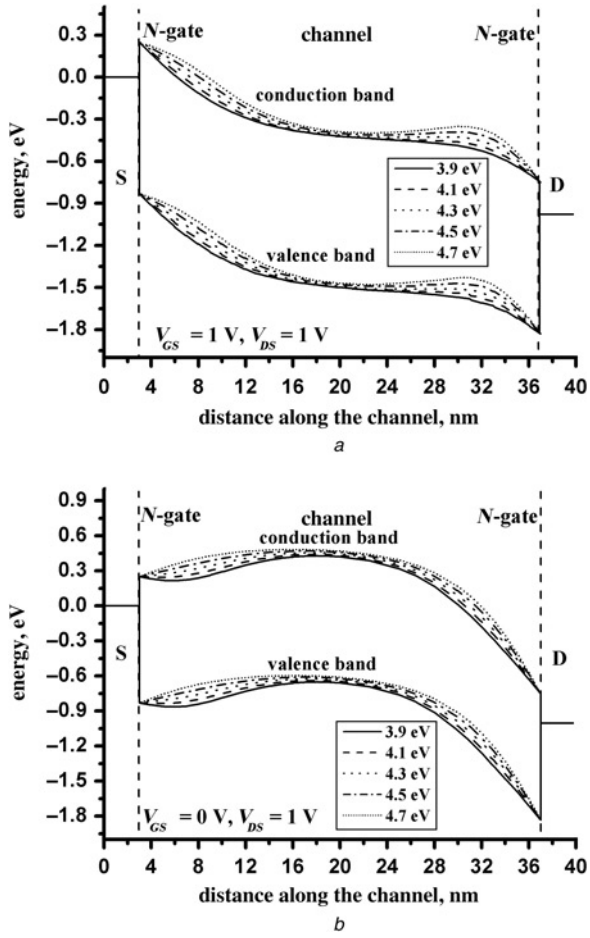

Fig. 5 *Energy band diagram of proposed DG SB-MOSFET with different N-gate work function*
a On-state
b Off-state

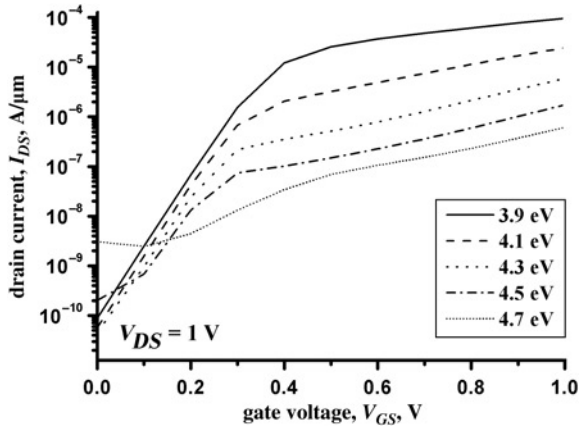

Fig. 6 *Transfer characteristics of the proposed DG SB-MOSFET with different N-gate work function*

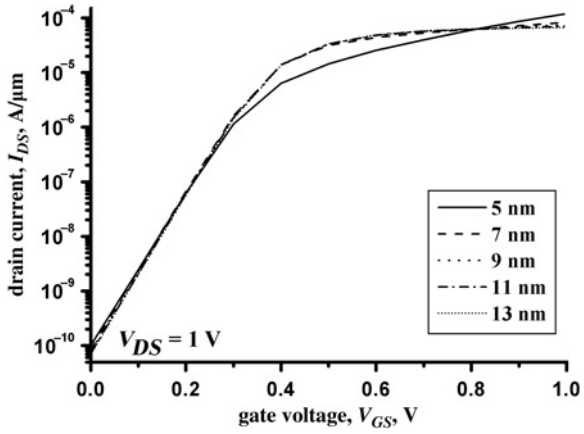

Fig. 7 *Transfer characteristics of the proposed DG SB-MOSFET with different N-gate length*

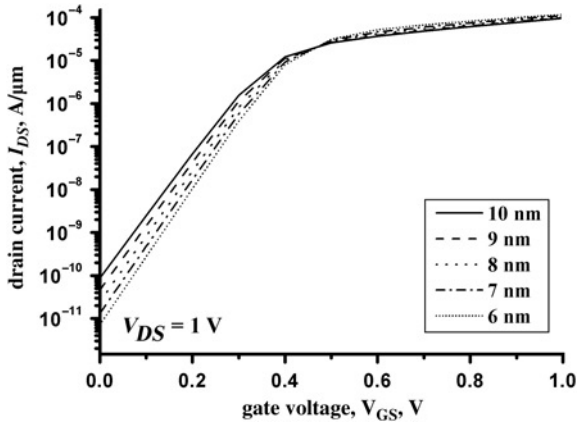

Fig. 9 *Transfer characteristics of the proposed DG SB-MOSFET with different channel thickness*

and drain contacts identical to effective channel length increases, due to this on-state current of the device decreases. The off-state current and SS of the proposed device is approximately same for increasing *N*-gate length.

For investigating the effect of channel thickness on device performance, five different values of channel thickness as 6, 7, 8, 9 and 10 nm is considered. Fig. 8*a* shows the on-state energy band diagram at 2 nm below the oxide-semiconductor interface of the proposed DG SB-MOSFET with different values of channel thickness. In the on-state, as channel thickness decreases the tunnelling barrier width at the source side SB reduces due to increased gate control over the channel [20, 21]. Consequently, the on-state tunnelling probability increases and results in increased on-state current. However, further decreasing the channel thickness below 6 nm increases the effective SB height due to quantum confinement of carriers [20]. As a result, on-state performance of the proposed device degraded, which is not shown here. Fig. 8*b* shows the off-state energy band diagram at 2 nm below the oxide-semiconductor interface of proposed DG SB-MOSFET with different channel thickness. In the off-state, for decreasing channel thickness the conduction band edge shift upwards. This in turn, reduces the thermionic emission of the charge carrier over the source side SB leading to reduction in off-state current. The transfer characteristics of the proposed DG SB-MOSFET with different channel thickness are shown in Fig. 9. It is evident from the figure that on-state current increases with the reducing channel thickness. Similarly, as shown in figure, for thinner channel, off-state current of the device is lower. Moreover, SS of the device is also improved for thinner channel.

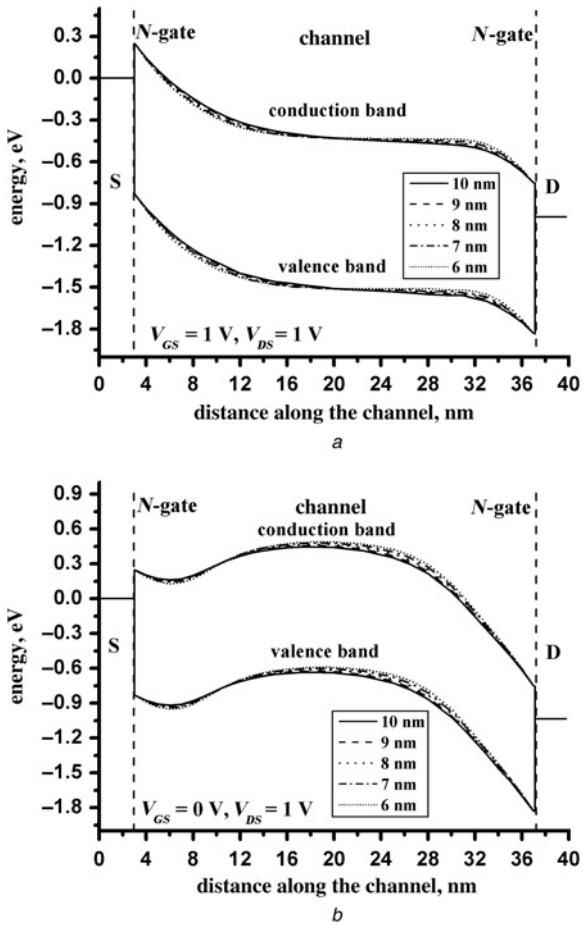

Fig. 8 *Energy band diagram of proposed DG SB-MOSFET with different channel thickness*
a On-state
b Off-state

4. Conclusions: In this Letter, we have successfully investigated a novel approach to design DG SB-MOSFET using gate engineering. In proposed device, we have effectively modulated the SBH and tunnelling barrier width for carrier injection using two additional *N*-gates. The proposed DG SB-MOSFET has similar behaviour and DC performance to the conventional DS SB-MOSFET and improved performance as compared with conventional SB-MOSFET. Our results demonstrate that the requirement of high energy implantation of dopants as in dopant segregation is completely eliminated in the proposed device, which offers the simplified process flow and immunity to device variability. Due to the absence of dopant atoms, the proposed DG SB-MOSFET is free from RDF. The proposed approach to implement DG SB-MOSFET is also applicable for nanowire type SB MOSFETs and provides incentive for further research and experimental verification.

5 References

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