New folding lateral double diffused metal oxide semiconductor breaking silicon limit with ultra-low specific on-resistance

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A new lateral double diffused metal oxide semiconductor (LDMOS) is proposed for the first time with the step oxide layer above the folding silicon substrate. Three technologies, including of the electric field modulation effect, majority carrier accumulation, and folding silicon, are applied simultaneously to the proposed LDMOS for improving the trade-off between the breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$). The majority carrier accumulation layer under the extended gate is formed in the folding silicon substrate during the on-state operation. The high-doping drift region can be depleted completely in the off-state, thanks to an additional electric field modulation, which is analogous to the super junction idea. The uniform lateral electric field has been obtained due to the new electric field peak to improve the trade-off between the BV and $R_{on,sp}$. The proposed LDMOS shows the $R_{on,sp}$ of 0.32 mΩ cm^2 with the BV of 62 V, which has broken the silicon limit relationship with $R_{on,sp}$ of 2.0 mΩ cm^2 under the same BV in the conventional LDMOS. This is the previously reported lowest $R_{on,sp}$ with the BV of about 60 V.

1. Introduction: Lateral double diffused metal oxide semiconductor (LDMOS) has been widely used in intelligent power applications due to the advantage of process compatible with the large-scale integration processes. The desired performance of LDMOS is to have the lowest specific on-resistance ($R_{on,\ sp}$) to minimise the conduction losses for the power integrated circuit. To further improve the trade-off characteristics between the breakdown voltage (BV) and $R_{on,sp}$, several structures have been designed including RESURF (REduced SURface field) [1] and super junction (SJ) technology [2]. In theory, the SJ structure can result in the high BV due to the charges balance in the pillars and low $R_{on,sp}$ is achieved by the highly doping in the N-pillars. However, for SJ-LDMOS, the P-type pillars implemented on a P-substrate cannot be depleted completely before the electric field of silicon reaches its critical breakdown, which is due to the substrate-assisted depletion effect [3]. Several technologies have been proposed and applied in LDMOS to optimise the electric field distribution [4–6].

In this Letter, we report a new folding LDMOS with the step oxide (SOFLDMOS) for the first time. This structure involves three main characteristics. First of all, in the off state, a new electric field peak is introduced in the lateral electric field distribution to optimise the surface electric field by the electric field modulation effect. Second, in the on state, the low-resistance conducting paths are produced by the electron accumulation layers along the folding silicon surfaces. Third, the electron accumulation layers are doubled by the folding silicon to reduce further the $R_{on,sp}$. The saturation current of SOFLDMOS is increased more than 3.4 times compared with that of the conventional LDMOS. For the conventional LDMOS, the concentration of the drift region is uniform and is optimised according to the RESURF technology. With a BV of 62 V, an ultra-low $R_{on,sp}$ of 0.32 mΩ cm^2 is obtained for SOFLDMOS, which is far <2.0 mΩ cm^2 for the conventional LDMOS with the same BV. The SOFLDMOS is proved to successfully break the conventional silicon limit.

2. Device structure and description: The proposed three-dimensional SOFLDMOS is shown in Fig. 1*a*. The key feature is the step oxide layer above the folding silicon substrate. There are three features in SOFLDMOS. First, the high concentration of the drift region can be depleted completely for SOFLDMOS in the off state because the gate electrode is extended to the drain electrode, which is similar to folded accumulation LDMOS (FALDMOS) [7]. Second, a strong majority carrier accumulation layer is formed at the surface of the drift region due to the extended gate electrode and thin field oxide in the on state, and is doubled, thanks to the folding silicon substrate. In effect, this accumulation layer provides the low on-resistance paths for SOFLDMOS. Third, a new electric field peak is introduced near the step oxide to optimise the surface electric field distribution by the electric field modulation effect [8]. As a result, comparing with FALDMOS, a higher BV can be obtained in SOFLDMOS. The folding silicon layer surface is made by using reactive ion etching from the channel to the drain electrode of SOFLDMOS. The cross-sections of the majority carrier accumulation layers along the OA and OB line are correspondingly shown in Figs. 1*b* and *c*. The drift regions I and Π are N-type doping silicon. Due to the electric field modulation effect, the concentration in the region I is higher than that in the region Π. The accumulated majority carrier is formed on both the surface and side-walls of the region I. In Fig. 1*c*, H and W are the height and width of the drift region I, respectively. T_s is the total thickness of the drift regions I and Π. L_d is the length of the drift region. L_{o1} and L_{o2} are the step oxide length. T_{o1} and T_{o2} are the step oxide thickness, respectively. The thickness of the gate oxide is 50 nm in SOFLDMOS. The lengths of the source and channel regions are 2.0 and 3.0 μm in this Letter for the simulation using ISE simulator [9]. The main physics models are applied in ISE simulation [9] including Mobility (DopingDepHighFieldsat Enormal), EffectiveIntrinsicDensity (OldSlotboom), Recombination [SRH(DopingDep) Auger Avalanche (Eparal)]. The criterion of break down is BreakCriteria {Current (Contact="drain"Absval=1e-7)}. The main solving model is Coupled {Poisson Electron Hole}. This electron accumulation layer is the beneficial effect of the metal electrode deposited over the step oxide layer covering the drift region for SOFLDMOS. In the off state, an additional modulation electric field is introduced along Z-direction, which is analogous to the SJ [2].

The SOFLDMOS can be implemented in a 0.18 μm standard complimentary metal oxide semiconductor process. Two critical processes for SOFLDMOS are to form the step oxide layer and

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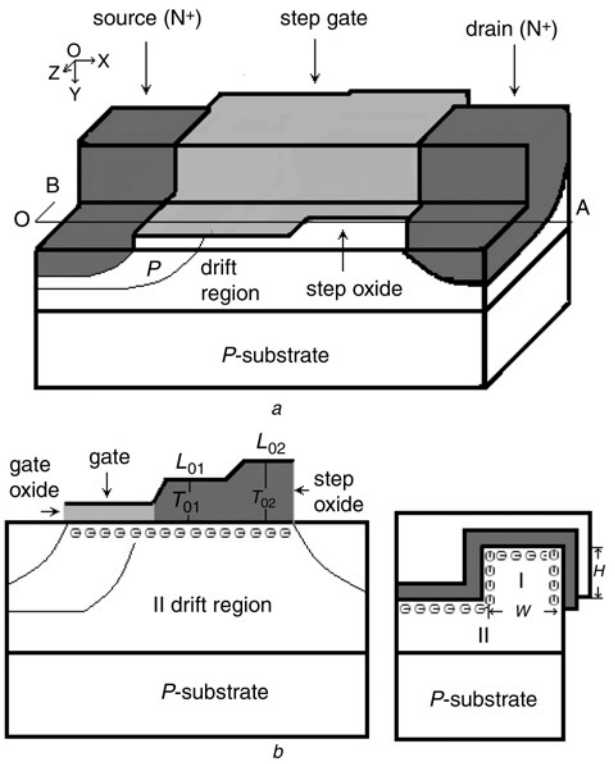


Fig. 1 *Three-dimensional structure of the SOFLDMOS*
a Proposed three-dimensional SOFLDMOS
b Cross-section of line OA
c Cross-section of line OB

trench silicon substrate, which are different from that in the conventional LDMOS. The drift regions I and Π layers are formed by twice phosphorus ions implants, and then driven-in by the rapid thermal process. After the folding silicon substrate is formed by trenching the silicon substrate using an extra mask, the step oxide layer is grown above the folding silicon substrate by twice thermal growth process. The gate oxide is thermally grown before the polysilicon gate is deposited.

3. Results and discussion: The lateral electric field distributions are shown by using ISE simulator in Fig. 2 for the conventional LDMOS, FALDMOS, and SOFLDMOS under the optimised condition. Note that the new electric field peaks P_k has been generated in the middle of the drift region in SOFLDMOS, which

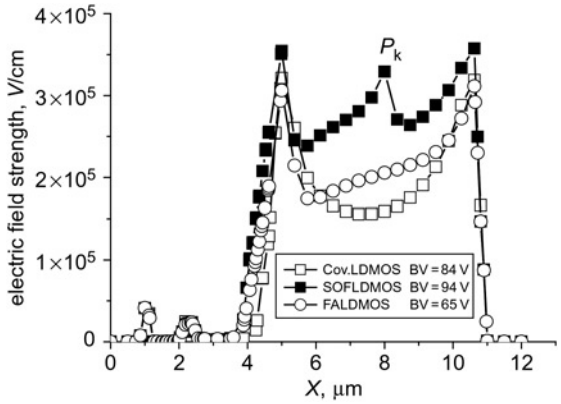


Fig. 2 *Lateral electric field distributions for the conventional LDMOS, FALDMOS, and SOFLDMOS: $L_d = 6$ μm, $W = H = 1$ μm, $L_{o1} = L_{o2} = 3$ μm, $T_{o1} = 0.4$ μm, $T_{o2} = 0.5$ μm, and $T_s = 2.0$ μm*

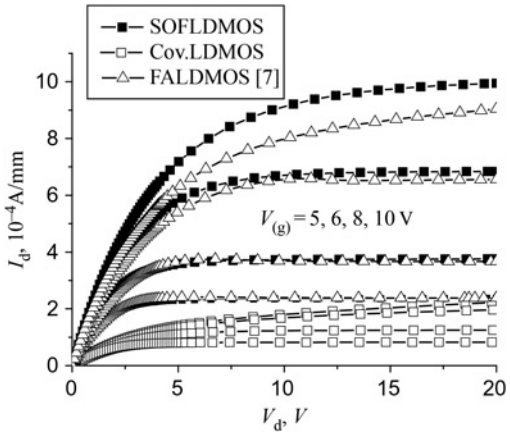


Fig. 3 *On-state characteristics of the conventional LDMOS and SOFLDMOS: $L_d = 4.0$ μm, $L_{o1} = L_{o2} = 2.0$ μm, $T_{o1} = 0.4$ μm, $T_{o2} = 0.5$ μm, $T_s = 2.0$ μm, and $H = W = 1.0$ μm*

is due to the electric field modulation by the step oxide layer. Therefore, a uniform lateral electric field is obtained for SOFLDMOS to improve the BV. In LDMOS, the low $R_{on,sp}$ can be obtained if the surface electric field is uniform at the given BV as explained by Duan *et al.* [8]. In other words, a higher BV (larger $\overline{E_x}$, $\overline{E_x}$ is the average lateral electric field) can be achieved before the device reaches its critical electric field. As a result, the BV in SOFLDMOST (94 V) is higher than that of the

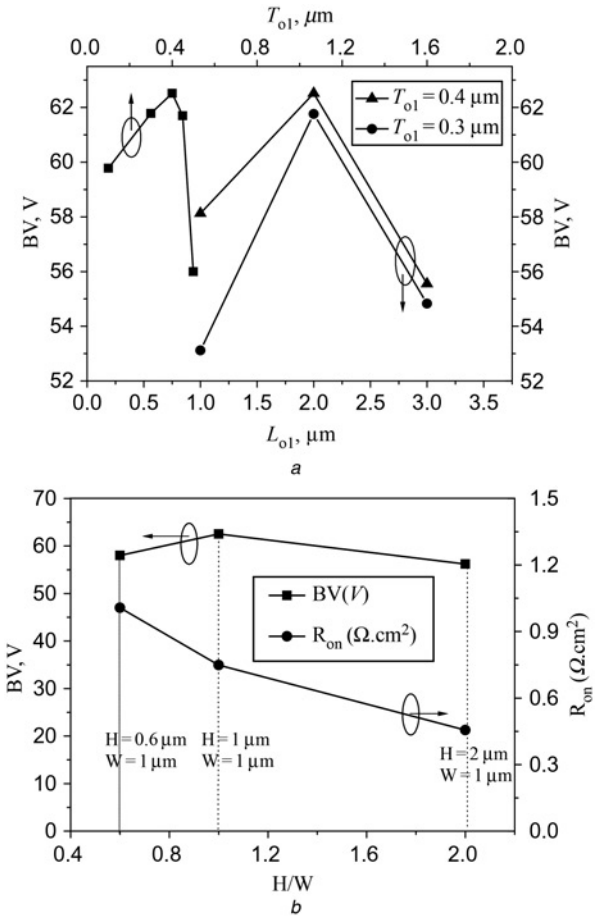


Fig. 4 *BV and $R_{on,sp}$ as the function of L_{o1} and T_{o1}*
a $T_s = 2.0$ μm, $H = W = 1.0$ μm, $L_d = 4.0$ μm, and $T_{o2} = 0.5$ μm; *H/W*
b $T_s = 2.0$ μm, $L_{o1} = L_{o2} = 1/2\ L_d = 2.0$ μm, $T_{o1} = 0.4$ μm, and $T_{o2} = 0.5$ μm

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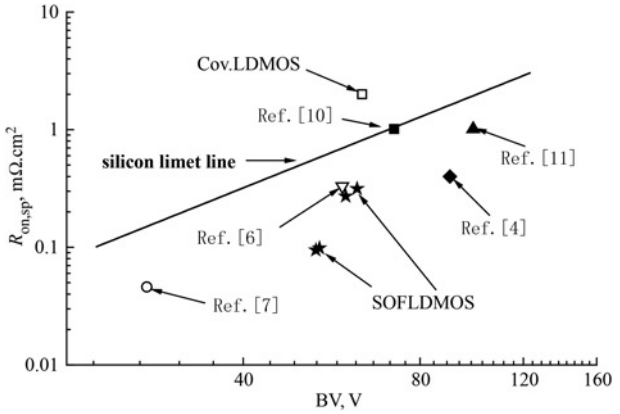


Fig. 5 *$R_{on,sp}$ against BV with the ideal silicon limit line*

conventional LDMOS (84 V) and FALDMOS (65 V) with the same drift region.

Fig. 3 shows the simulated on-state I_{DS}–V_{DS} characteristics of the conventional LDMOS, FALDMOS, and SOFLDMOS. It confirms that, by introducing the folding silicon and doubled majority carrier accumulation layers, SOFLDMOS has lower on-resistance and higher transconductance than that of the conventional LDMOS. It can be seen that the saturation current of SOFLDMOS is more than 3.4 times higher than that of the conventional LDMOS.

Fig. 4*a* shows the BV as the function of L_{o1} and T_{o1}. The new electric field peak P_K shifts gradually as a function of the value of L_{o1}. It is shown that the maximal BV is achieved when the L_{o1} is half of L_d. That is to say, the optimised surface electric field can be obtained when the P_K is located at the middle of the drift region (Fig. 2). The BV is decreased with the T_{o1} thinned, which results from the too high electric field peak P_K. The BV is also decreased with the T_{o1} thickened, which results from too low electric field peak P_K. For SOFLDMOS, the maximal BV is obtained when the T_{o1} is 0.4 μm with the T_{o2} of 0.5 μm (Fig. 4*a*). This mechanism is similar to the step field plate theory. Fig. 4*b* shows the BV and $R_{on,sp}$ as a function of *H/W* for the certain *H* and *W*. The optimised parameters for L_{o1} and T_{o1} are applied to this analysis. It is important to show that the $R_{on,sp}$ was reduced as *H/W* is increased, which results from the increased density of the accumulation layer when the etching depth of the folding silicon is increased. The BV is not affected obviously by *H/W*.

The $R_{on,sp}$ of SOFLDMOST against BV are compared with the reported results in Fig. 5. Proposed SOFLDMOST was simulated with the drift region lengths around 4.0 and 6.0 μm. The *H* and *W* are both 1.0 μm. T_s is 2.0 μm. Fig. 5 shows that a ultra-low $R_{on,sp}$ of 0.32 mΩ cm^2 is obtained with the BV of 62 V, which is much lower than 2.0 mΩ cm^2 for the conventional LDMOS with the same BV. The contact resistance for the source and drain electrodes is <0.01 mΩ cm^2, which is much smaller than the $R_{on,sp}$ of 0.32 mΩ cm^2. Hence, the contact resistance is ignored in this discussion. The experimental results of the references have been demonstrated in Fig. 5. The experimental results had been reported in [10] that the BV is 98.6V with the $R_{on,sp}$ of 1.01mΩ cm^2. For [11], the tested $R_{on,sp}$ of 1.01 mΩ cm^2 with the BV of 72.3V. By comparing with the results of the references, the silicon limit has been broken in SOFLDMOS. The ultra-low $R_{on,sp}$ has been obtained with the BV of about 60 V.

4. Conclusion: A novel SOFLDMOS has been proposed in this Letter for the first time to demonstrate the ultra-low $R_{on,sp}$. Three kinds of the technologies have been applied to SOFLDMOS simultaneously. The new electric field peak is introduced to improve the trade-off between the BV and $R_{on,sp}$ by the electric field modulation effect compared with the proposed FALDMOS by the authors. The results indicate that the silicon limit has been broken in SOFLDMOS. As to our knowledge, the lowest $R_{on,sp}$ of 0.32 mΩ cm^2 under the BV of about 60 V is achieved in this proposed SOFLDMOS. The saturation current of SOFLDMOS is increased more than 3.4 times compared with that of the conventional LDMOS. The significance of the SOFLDMOS concept will be available for not only LDMOST, but also lateral insulated-gate bipolor transistor (LIGBT). However, the turn-off of the SOFLDMOS is very fast as there was no minority-carrier storage in the drift region compared with the LIGBT.

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