Asymmetric lightly doped Schottky barrier CNTFET

Amin Ghasemi Nejad Raeini[1], *Zoheir Kordrostami*[2]

[1]*Gole Gohar mining and Industrial Co, Sirjan, Iran*
[2]*Department of Electrical and Electronic Engineering, Shiraz University of Technology, Shiraz, Iran*
E-mail: Ghasemi_a@golgohar.com

Published in Micro & Nano Letters; Received on 13th November 2015; Revised on 10th January 2016; Accepted on 3rd February 2016

For the first time, an asymmetric lightly doped Schottky barrier carbon nanotube field effect transistor (SB_CNTFETs) is proposed and simulated using quantum simulations. Comparisons are made among four SB_CNTFETs structures for electrical characteristics. One is the conventional SB_CNTFET with an intrinsic channel. The other proposed and studied designations are an asymmetrically doped SB_CNTFET with a doped region near the source only, a symmetrically doped source and drain SB_CNTFETand an asymmetric lightly doped SB_CNTFET which shows the ultimate performance among all. The results show that the new asymmetric lightly doped design decreases significantly the leakage current and thus increases on/off ratio as well as cutoff frequency. It is also demonstrated that this structure possesses two perceivable steps in potential profile of the channel, which lead to another lateral electric field peak inside the channel which leads to the immunity against short-channel effects. The cutoff frequency characteristics of the four structures of SB_CNTFETs have been discussed. Results show that for channel lengths >30 nm cutoff frequency of the asymmetric lightly doped SB_CNTFETis greater than others. The effect of different doped region lengths in a 30 nm SB_CNTFET has been discussed as well. The proposed new design is promising from several points of view discussed in the study.

1. Introduction: The carbon nanotube field effect transistor (CNTFET) is one of the most promising alternatives for the replacement of bulk silicon MOSFETs due to its superior electrical properties [1]. CNTFETs are types of molecular transistors that have already demonstrated high on-currents [1]. In MOSFETs as the thickness scales below 1 nm, off current increases drastically, leading to high power consumption and reduced device reliability [2]. Although the CNTFETs have been shown the potential of replacing MOSFETs but device designs have not yet been optimised. Especially the Schottky barrier CNTFETs (SB_CNTFETs) characteristics can still be improved if an appropriate designation is proposed. Performance optimisations of conventional CNTFETs have been under study for some years [3]. As for halo implantation, previous works have shown that halo doping is one of the device engineering technologies to enhance the immunity against the short-channel effects (SCE) in conventional CNTFETs [3, 4]. Combination of halo implantation and dual-material gate has also been used for CNTFET optimisation [5]. In the literature SB-CNTFETs have been under research much less than the common CNTFETs. In this paper we study the effect of N-type doping in conventional SB_CNTFETs. Doped regions near source/drain contacts have been added and the effects of them on the device performance have been investigated. We have designed an asymmetric SB-CNTFET which simultaneously combines the SB-CNTFETs and common CNTFETs characteristics. The proposed structures benefit from both Schottky and Ohmic contacts while the doped region near the source has been engineered for optimised performance. By using this structure the carrier injection at the source and drain contacts can be separately controlled [2]. The proposed device has a lower off-current, larger transconductance and better frequency response.

To suppress ambipolar behaviour, an asymmetric lightly doped SB_CNTFET (ALDS SB_CNTFET) has been proposed in which near the source contact two lightly and heavily doped regions exist. The source engineered Ohmic contact and the Schottky drain contact define the device characteristics. The results of this paper show that the new asymmetric SB-CNTFET has a better dc and ac performance compared with common CNTFETs or conventional SB-CNTFETs.

The rest of this paper is organised as follows: in Section 2 we give an overview of the simulation approach and the equations to calculate physical parameters using numerical simulations, which are based on the self-consistent solution of the two-dimensional (2D) Green's functions and Poisson equations [5]. In Section 3, we will introduce the new structures and the energy diagram of structures will be discussed. In Section 4, all of the simulation results have been shown and discussed. The effects of our proposed design inALDS SB_CNTFET structure on the off current, on/off current ratio and the cutoff frequency are shown and studied. Finally, we conclude this paper in Section 5.

2. Schottky barrier carbon nanotube field effect transistor: Schematic of the conventional device is represented in Fig. 1*a*. The device is composed of an intrinsic CNT as the channel contacted to the source and drain metal electrodes. The gate controls the Schottky barrier width at the interface of the CNT-metal interface and the tunnelling current is controlled by the gate voltage (Fig. 1).

2.1. NEGF equations: In the CNTFET considered in this work, the quantum confinement effect along the azimuthal direction gives rise to subbands, and the one-dimensional (1D) effective-mass Hamiltonian for the lowest subband of the nanotube can be defined as follows [6]

$$H = \frac{\hbar^2 \partial^2}{2m_z^* \partial^2} + E_{\text{pot}}(z) \tag{1}$$

where m^*_z is the effective mass in the z (transport) direction and $E_{\text{pot}}(z)$ is the 1D potential energy, which is defined according to the Flietner equations

$$\begin{aligned} E_{\text{pot}}(z) &= |E - E_0(z)| - \Delta \quad \text{if} \quad |E - E_0| \geq \Delta \\ E - E_{\text{pot}}(z) &= \frac{|E - E_0(z)|^2 - \Delta^2}{2\Delta} \quad \text{if} \quad |E - E_0| \prec \Delta \end{aligned} \tag{2}$$

In the above equation, $E_0(z)$ is the charge neutrality level and Δ is

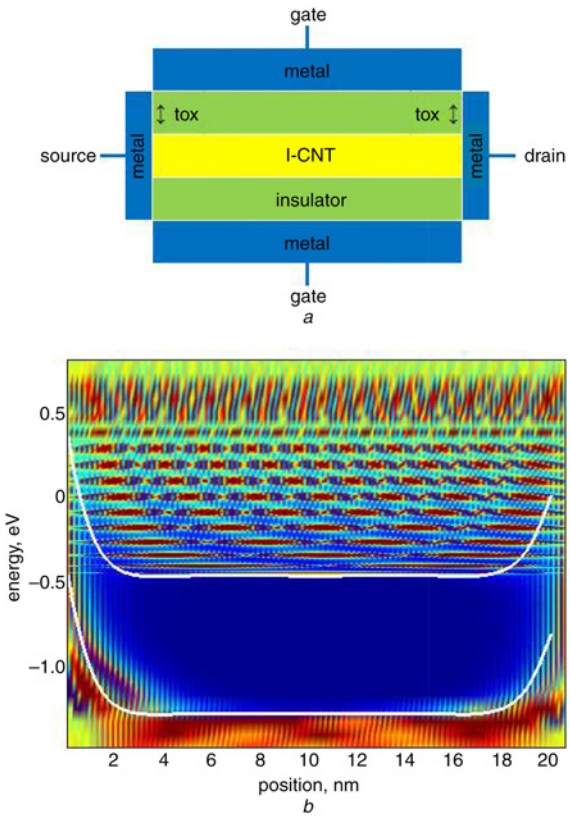

Fig. 1 *Schematic of the conventional device*
a Structure of SB_CNTFET
b Energy-position of SB_CNTFET

the energy distance between the bottom of the lowest subband and E_0.

For semi-infinite source and drain contacts, the self-energies, Σ_S, $_D$, are given by

$$\sum S = \frac{1}{2}(E - 2t - E_S - i\sqrt{4t + E_S - E)(E - E_S)}) \quad (3)$$

$$\sum D = \frac{1}{2}(E - 2t - E_D - i\sqrt{4t + E_D - E)(E - E_D)}) \quad (4)$$

Where E_S and E_D are the subband energies at the source and drain contacts, respectively.

Hence the Hamiltonian and the self-energies are obtained, the Green's function G can be calculated via

$$G(E) = \left[EI - H - \sum s - \sum D\right] \quad (5)$$

2.2. Poisson equation: The 2D cylindrical Poisson equation [6, 7],

$$\frac{\partial^2}{\partial\rho^2} + \frac{1}{\rho}\frac{\partial\phi}{\partial\rho} + \frac{\partial^2\phi}{\partial z^2} = \partial\frac{q_0}{\varepsilon}\frac{1}{2\pi R_t}(P(z) - n(z) - N(A)) \quad (6)$$

was solved to obtain the electrostatic potential $\phi(\rho, z)$, which reduces to the Laplace equation in the device (CNT) and gate insulator (oxide) regions, except for the CNT/oxide interface, because charges exist only at the CNT surface.

The boundary conditions used to solve the Poisson equation for SB_CNTFET are

$$\phi(\rho = R_g, z) = P_{SM} + V_g \quad (7)$$

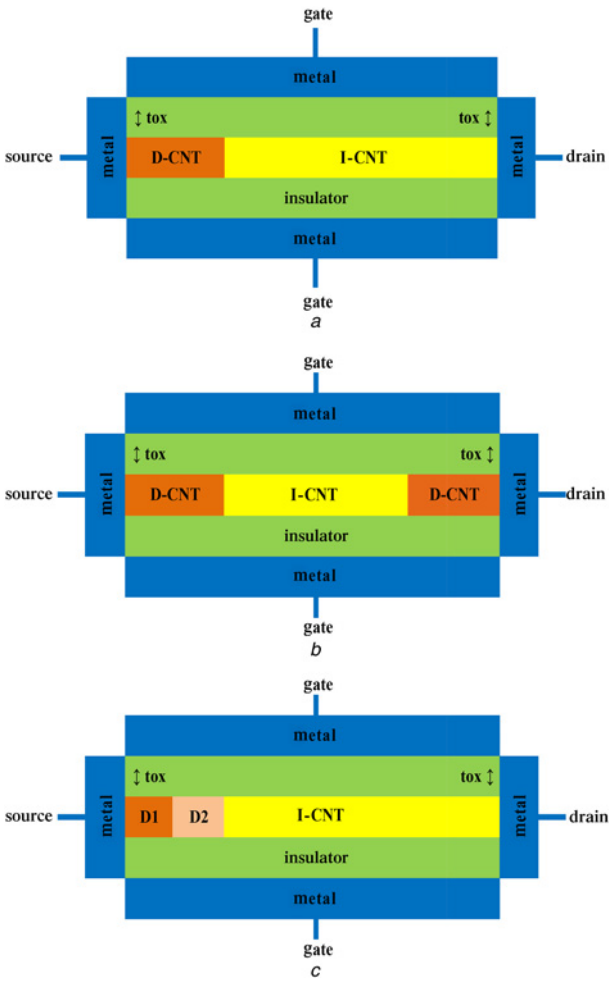

Fig. 2 *Schematic diagram of the three structure of doped SB_CNTFET*
a ADS_SB_CNTFET
b SDSD_SB_CNTFET
c ALDS_SB_CNTFET

$$\left.\frac{\partial\varphi}{\partial\rho}\right|_{\rho=0}(z) = 0 \quad (8)$$

$$\varphi(\rho, z = 0) = P_{SM} \quad (9)$$

$$\phi(\rho, z = L) = P_{SM} + V_d \quad (10)$$

Where P_{sm} is the source built-in potential at the interface of the source and the channel (CNT) which is determined by the work function difference between the metallic contact and the semiconducting nanotube.

2.3. Self-consistent calculation: We repeat the steps of solving the coupled 2D Poisson 1D NEGF equations until a self-consistent potential is obtained. Once self-consistency is achieved, the drain current for coherent transport under a bias voltage v can be calculated by means of the Landauer-Buttiker formula [6, 8]

$$I(V) = \frac{4q_0}{h}\int T(E, V)[f_S(E) - f_D(E)]\,dE \quad (11)$$

where q is the electron charge, $f_{S,D}(E)$ are the Fermi functions at the source and drain sides and $T(E)$ is the source to drain transmission.

The intrinsic cutoff frequency of the CNTFET is computed by [8, 9]

$$Ft = \frac{1}{2\pi}\cdot\frac{gm}{Cg} \quad (12)$$

doi: 10.1049/mnl.2015.0434

where the gate capacitance (C_g) and the transconductance (g_m) are

$$C_g = \frac{\partial Qg}{\partial Vgs}\Big|Vd. \quad (13)$$

$$g_m = \frac{\partial Id}{\partial Vgs}\Big|Vd. \quad (14)$$

3. Proposed designs of SB_CNTFET: Schematic diagram of the three structure of doped SB_CNTFET are shown in Fig. 2, where a (13,0) CNT has been considered as the channel with length of $L = 30$ nm and doped source/drain with length of $L_d = 5$ nm and doping of $N_d = 1.5$ nm^{-1} (Fig. 2).

In Fig. 2*a* an asymmetrically doped source SB_CNTFET (ADS_SB_CNTFET) is shown in which only a 5 nm region near the source is doped. In Fig. 2*b* a symmetrically doped source and drain SB_CNTFET is shown in which both source and drain have the identical doped regions. In Fig. 2*c* an asymmetrically lightly doped source SB_CNTFET (ALDS_SB_CNTFET) is shown in which the doped region near source has been divided in two parts. One part is lightly doped and the other is heavily doped. The dopant concentrations and the length of the two parts are $N_{d1} = 1.5$ nm^{-1}, $N_{d2} = 0.15$ nm^{-1} and $L_{h1} = L_{h2} = L_d/2 = 2.5$ nm.

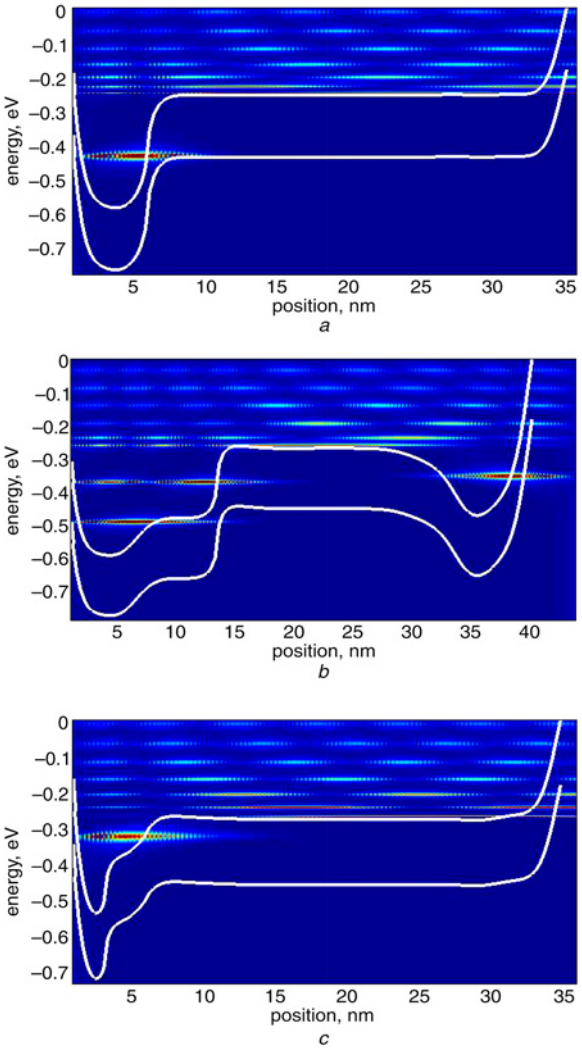

Fig. 3 *Energy-position of*
a ADS_SB_CNTFET
b SDSD_SB_CNTFET
c ALDS_SB_CNTFET

Fig. 3 shows the energy diagram of the three designs. The energies of the conduction and valence band edges define the behaviour of the device. As can be seen in Fig. 3, by using doping the Schottky barriers at the CNT-metal interface becomes thinner and the tunnelling current loses its dependency on the gate voltage. It means that an Ohmic contact is formed. The interesting point in the design of the devices is that the advantages of both Ohmic and Shottky contacts have been used.

4. Result and discussion: The ambipolar behaviour of four structures of SB_CNTFET is clearly observed from Fig. 4. In N-type CNTFET, applying a positive drain voltage decreases the energy barrier at the drain contact and consequently increases hole injection at this contact [1, 3] (in this paper, N-type doping has been used in all structures.). The simulation is carried out at room temperature ($T = 300$ °K).

4.1. Current characteristics of four structures of SB_CNTFETs: We start by simulating the ballistic transfer characteristics of different structures of SB_CNTFETs at the same supply drain voltage ($V_{ds} =$ 0.4 v). As can be seen in Fig. 4 the off-state current of conventional SB_CNTFET is larger than those of other three structures and ALDS structure has the smallest off-state current. The off-state current of ADS_SB_CNTFET is slightly lower than SB_CNTFET and that of SDSD_SB_CNTFET is much lower than that theADS_SB_CNTFET, which means that reduced off-state current of ALDS_SB structure is mostly attributed to the special design of its doped regions. Compared with other structures, ALDS structure has a slightly lower on-state current than that of SDSD_SB_CNTFET, but the on/off ratio (I_{on}/I_{off}) of ALDS_SB structure is significantly large compared with other structures.

4.2. Characteristics of scaling down: To further investigate the scaling potential of proposed new structure, the comparisons have been made among the four SB_CNTFET structures at different channel lengths. The variations of off-state current, on-state current and on/off ratio versus channel length are shown in Fig. 5. The off current and on current are defined as the channel current when $V_g = 0$ v, $V_{ds} = 0.4$ v and $V_g = V_{ds} = 0.4$ v, respectively.

In Fig. 5*a*, it is observed that for new structure, longer channel will lead to lower off-state currents. This is due to the fact that as channel length increases, the gate control on the electrostatic of channel region enhances and consequently the leakage current diminishes dramatically [10]. Fig. 5*b* shows the on-state current, it is noted that the on-state current (I_{on}) of four structures remains approximately constant, which indicates that the ballistic on-state current is nearly independent of the channel length with the gate

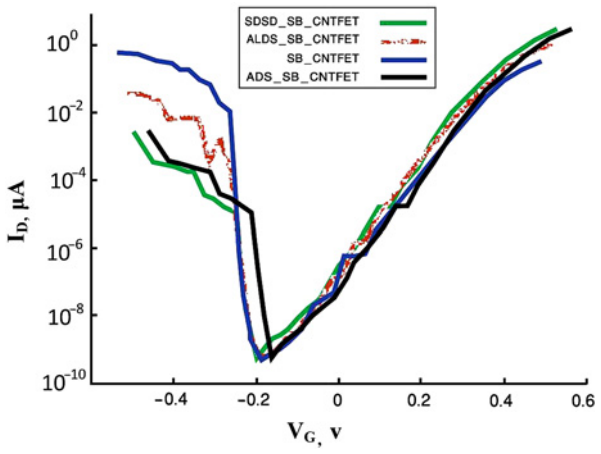

Fig. 4 *Output characteristics of the SB-CNTFET structure at different gate voltages, Vds = 0.4 v*

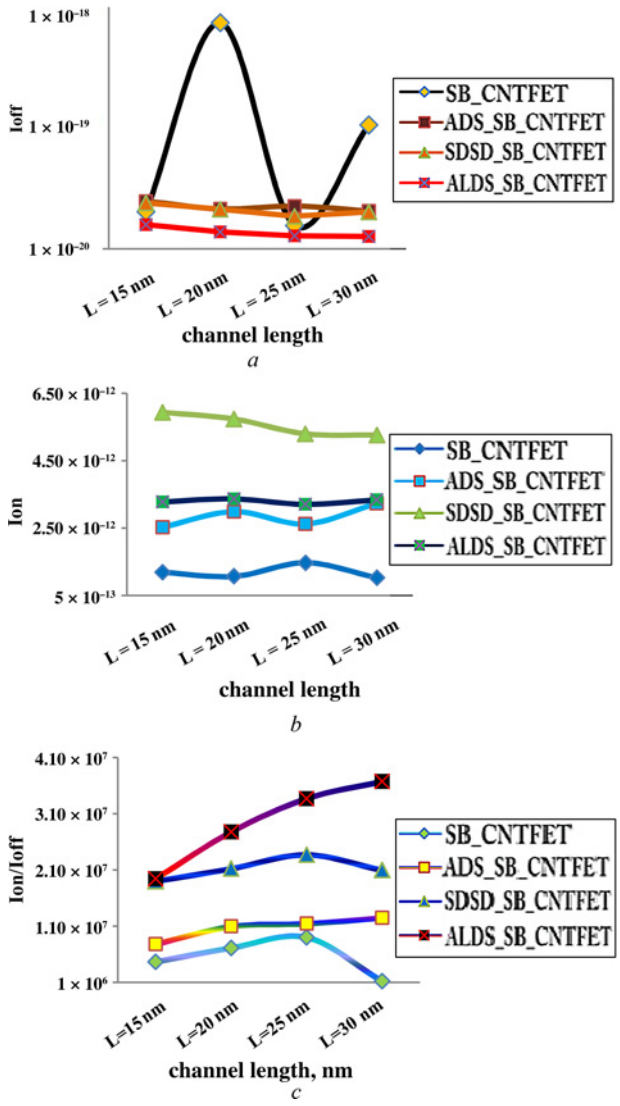

Fig. 5 *Variation of*
a Ioff
b Ion
c Ion/Ioff of four structures of SB_CNTFETs with channel length at $V_{gs} = V_{ds} = 0.4$ v

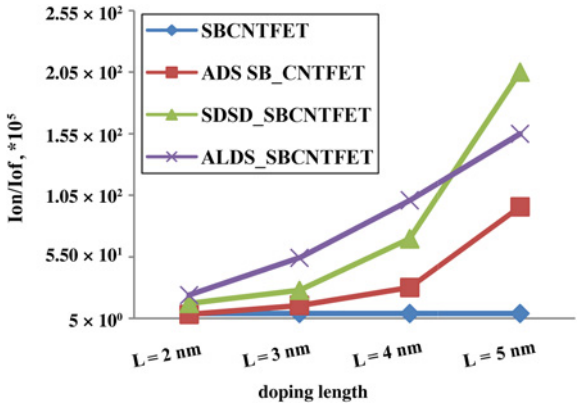

Fig. 6 *I_{on}/I_{off} of four structures of SB_CNTFETs with doping Length at gate length = 30 nm*

length range from 15 to 30 nm. Hence the on/off current ratio improves with an increase of the length (Fig. 5*c*). In Fig. 5*c*, the ALDS structure shares larger I_{on}/I_{off} ratio, indicating that it is

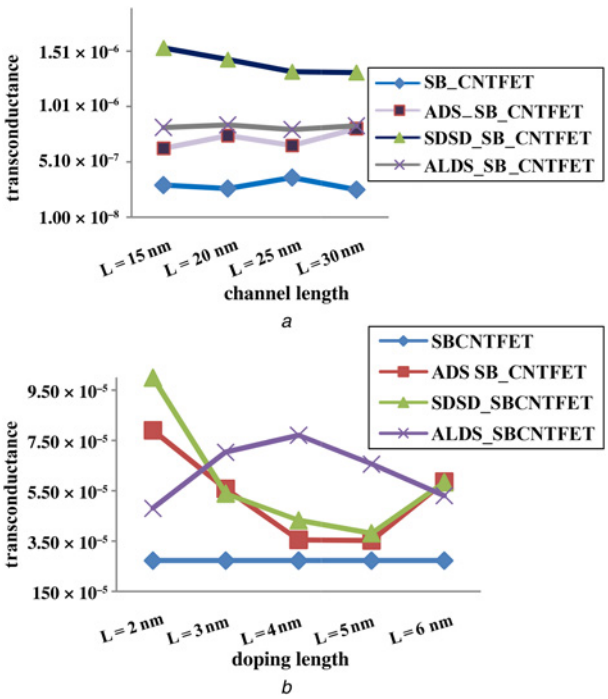

Fig. 7 *Variation of g_m with*
a Channel length at $V_g = V_d = 0.4$ v
b Doping length at gate length = 30 nm

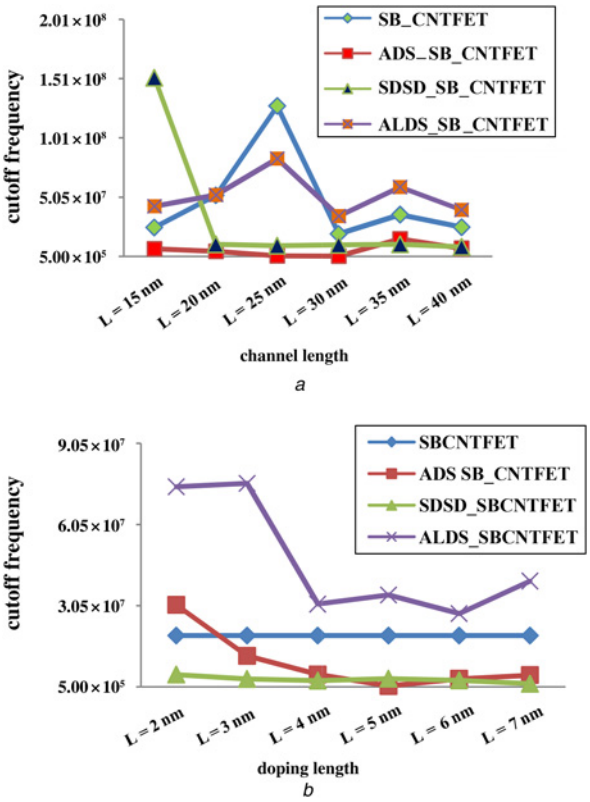

Fig. 8 *Variation of cutoff frequency with*
a Channel length and $V_g = V_d = 0.4$ v
b Doping length at channel length = 30 nm, $V_d = 0.4$ v

possible to achieve a good ballistic on/off ratio current close to 2×10^7 even at a channel length of 15 nm and (13,0) chiral vector.

The on/off ratio versus doping length is plotted in Fig. 6. It helps for selecting the good doping length. It is depicted in Fig. 6 that

doi: 10.1049/mnl.2015.0434

SB_CNTFET with doped regions can reduce off-state current which an increase in the on/off ratio.

The variation of transconductance (g_m) versus the channel length and the doping length is shown in Fig. 7. As shown in Fig. 7*a*, longer channel length leads to lower transconductance for SDSD_SB_CNTFET and a constant level for ALDS structure. This is primarily due to an increase in channel length that results in a larger effective channel length, which reduces SCE and DIBL [6]. The variation of transconductance (g_m) with doping length at channel length = 30 nm are shown in Fig. 7*b*. It is also observed that generally the transconductance of ALDS Structure is significantly larger than ADS_SB_CNTFET and SB_CNTFET structures.

The cutoff frequency (F_t) with respect to the doping length and channel length is shown in Fig. 8. In Fig. 8*a*, we found that the intrinsic cut-off frequency keeps decreasing approximately as the channel length increases from 25 to 30 nm range and the intrinsic cutoff frequency of ALDS structure is larger than those in other devices, which means it has higher average electron velocity than other devices. The simulated intrinsic cutoff frequency of ALDS_SB_CNTFET, SB_CNTFET, SDSD_SB_CNTFET and ADS_SB_CNTFET at Lch = 30 nm is about 34.5 MHz, 19.4 MHz, 15 MHz and 10 MHz, respectively. The variations of cutoff frequency with doping length at channel length = 30 nm are shown in Fig. 7*b*.

As shown in Fig. 8*b*, the cutoff frequency of the new proposed device is larger than all other transistors. This means that our proposed ALDS_SB_CNTFET exhibits very good ac and dc characteristics and has improved the performance of the SB_CNTFETs.

5. Conclusions: In this paper, the behaviour of CNTFET transistor with Schottky contact is theoretically studied with a quantum kinetic model. This is the first time that a structure such as ALDS with an improved ac and dc performance is proposed. Results show that compared with the other structures, ALDS_SB_CNTFET significantly decreases leakage current and thus increases on/off ratio, indicating that the proposed structure has better gate controllability than conventional SB_CNTFET.

The influence of channel length on current characteristics has been studied. The simulations revealed that longer channel can decrease off-state currents for ALDS Structure, while the ballistic on-state current of four structures remains approximately constant. The cutoff frequency of the new transistor was optimised by selecting the appropriate doping level and length. The ALDS_SB_CNTFET benefits from two doped regions near the source which improves the device parameters compared with other devices. The proposed CNTFET is a new structure satisfying a well-behaved nano transistor requirements defined by device designers.

6 References

[1] Amin Ghasemi N.R., Kordrostami Z., Javaheri M.: 'High on/off current ratio in SB-CNTFET based on tuning the gate insulator parameters for different ambient temperatures'. IEEE NEMS, 2015

[2] Pourfath M., Ungersboeck E., Gehring A., *ET AL.*: 'Optimization of Schottky barrier carbon nanotube field effect transistors'. Microelectronic Engineering, 2004, pp. 428–433

[3] Kordrostami Z., Hossein Sheikhi M., Zarifkar A.: 'Cutoff frequency and switching delay of underlap carbon nanotube FETs' (Taylor & Francis Group, 2013), pp. 681–694

[4] Kordrostami Z., Sheikhi M.H., Zarifkar A.: 'Influence of channel and underlap engineering on the high-frequency and switching performance of CNTFETs', *IEEE Trans. Nanotechnol.*, **11**, (3), 2012, pp. 526–533

[5] Wang W., Li N., Xia C., *ET AL.*: 'Quantum simulation study of single halo dual-material gate CNTFETs'. Solid-State Electronics, 2014, pp. 147–151

[6] Cao Y., Sinha S., Balijepalli A.: 'Compact modeling of carbon nanotube transistor and interconnects'. INTECH OPEN, 2010, pp. 217–236

[7] Arefinia Z.: 'Investigation of the performance and band-to-band tunneling effect of a new double-halo-doping carbon nanotube field-effect transistor', *Physica E*, **41**, (10), 2009, pp. 1767–1771

[8] Wang W., Zhang T., Zhang L., *ET AL.*: 'High-frequency and switching performance investigations of novel lightly doped drain and source hetero-material-gate CNTFET'. Materials Science in Semiconductor Processing, 2014, pp. 132–139

[9] Hejazifar M.J., Ziabari S.A.S.: 'Investigation of the cutoff frequency of double linear halo lightly doped drain and source CNTFET', *Int. Nano Lett.*, 2014, **4**, (3), pp. 1–5

[10] Ahn C., Shin M.: 'Quantum simulation of coaxially gated CNTFETs by using an effective mass approach', *J. Korean Phys. Soc.*, 2007, **50**, (6), pp. 1887–1893