# Bistable memory and logic-gate devices fabricated by intercrossed stacking of graphene–ferroelectric hybrid ribbons

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A ferroelectric-gated graphene field-effect transistor was fabricated by consecutively stacking two distinct graphene–ferroelectric hybrid ribbons at right angles. Two graphene layers play different roles. One graphene layer acts as a gate electrode and the other graphene layer acts as a channel between two electrodes, source and drain. Electric gating at the gate graphene modulates the resistance of the channel graphene. By means of ferroelectric polarisation, bistable resistance states of the channel graphene could be recorded, and the retention time of bistability was estimated to be 460 days by extrapolating of two resistance values in time–resistance relationships. Furthermore, the underlying concept to fabricate bistable memory device was extended to the methodology to realise a logic-gate device by stacking three distinct graphene–ferroelectric hybrid ribbons.

**1. Introduction:** Graphene, an atomically two-dimensional (2D) carbon sheet, is an up-and-coming material for emerging optoelectronic devices due to its superior material properties [1]. One of its most singular features is that electrical properties of graphene can be modulated by controlling the Fermi level by means of doping [2]. While doping concentration performed by the blending of chemicals is volatile, doping induced by permanent polarisation in an adjacent ferroelectric polymer will be an optimal scheme in terms of non-volatility [3]. Specifically, ferroelectric polymers based on poly(vinylidene fluoride – trifluoroethylene) [P(VDF-TrFE)] are environmentally insensitive, mechanically flexible and transparent in visible light [3, 4]. Occasionally, they can be used as a supporting layer for the transfer of graphene. Therefore, ferroelectric polymers do not need to be removed after a graphene transfer. This is a superior scheme compared with a graphene transfer based on poly(methyl methacrylate). For a synergetic effect of two materials, if a graphene–ferroelectric hybrid ribbon (GFeR) is defined as a basic module, a diverse range of optical and electronic systems can easily be manufactured by assembling and stacking the basic modules at designed positions on a substrate. In this Letter, we demonstrate bistable graphene field-effect transistors fabricated by the stacking of two basic modules, each of which consists of a GFeR. Furthermore, a logic-gate device will be also demonstrated by adapting the basic concept to realise the bistable graphene field-effect transistor.

**2. Device structure and fabrication:** Single-layer graphene synthesised by chemical vapour deposition on a copper foil was purchased from GRAPHENE SQUARE, Inc. Ferroelectric P(VDF-TrFE)(75:25, Elf Atochem) was dissolved in cyclohexanone, spin-coated onto graphene on a Cu foil, and annealed at 130°C for 1 h, after which the thickness was 1.2 µm. Two identically sized GFeR (300 µm × 1 mm) were prepared, and the Cu foil was etched with a copper etchant, ammonium persulphate $(NH_4)_2S_2O_8$. For preparation of substrate, a thermally grown $SiO_2$/Si wafer was cleaned for 30 min with the mixture of sulphuric acid and hydrogen peroxide, and rinsed away with deionised water several times. On a cleaned $SiO_2$/Si wafer, three electrodes as a source, drain and gate were formed by evaporating Cr/Au (10 nm/50 nm) and patterning the metal via a lift-off process. One GFeR was transferred onto the prepared wafer, covering the source and drain electrodes, after which it was dried at 100°C for 1 h. The second GFeR was stacked onto the pre-positioned GFeR at right angles, covering the gate electrodes, and dried at 100°C for 1 h as well. The device structure and each electrode were assigned as depicted in Fig. 1*a*. Fig. 1*b* shows the cross-sectional view of the K–K′ dotted line in Fig. 1*a*, in which the ferroelectric film in the first GFeR [1st P(VDF-TrFE) in Fig. 1*b*] acts as a gate dielectric and the graphene in the first GFeR acts as a channel in a field-effect transistor. The channel graphene was represented as $G_{CH}$. The ferroelectric film in the second GFeR [2nd P(VDF-TrFE) in Fig. 1*b*] encapsulates the

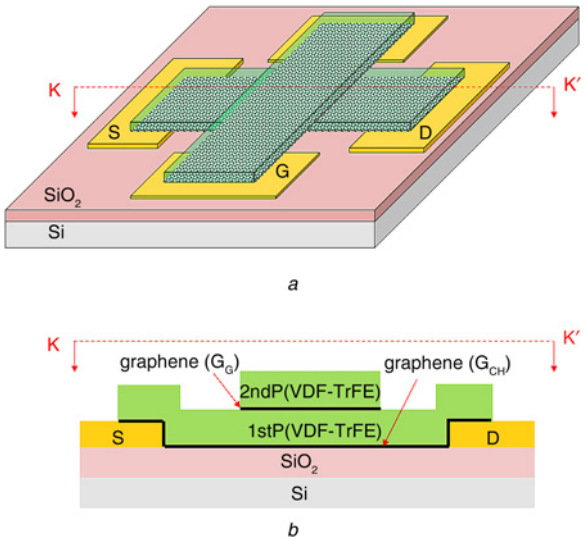


**Fig. 1** *Graphene field-effect transistor fabricated by stacking two ferroelectric–graphene hybrid ribbons at right angles*
*a* Schematic diagram of the 3D graphene field-effect transistor
*b* Cross-sectional view of K–K′


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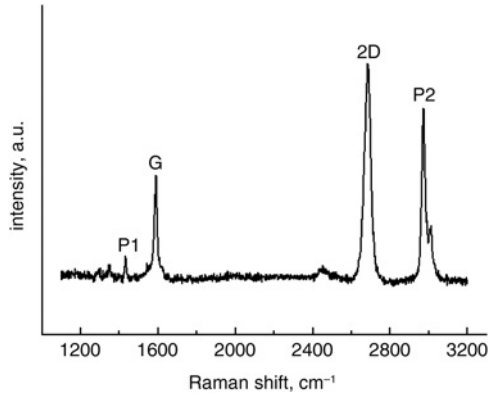


**Fig. 2** *Raman shift of graphene–ferroelectric hybrid film*

gate graphene ($G_G$). All current–voltage relationships were measured with a HP4156 semiconductor parameter analyser in an electromagnetic field shielded box.

**3. Raman spectroscopy measurement:** To secure the single-layer graphene in the basic module of GFeR, Raman shift was measured with a laser source of 514 nm at Raman spectroscopy (ARAMIS, Horiba Jobin Yvon). Fig. 2 represents the result of Raman shift. The intensity ratio of G peak (1584 $cm^{-1}$) and 2D peak (2684 $cm^{-1}$) is about 2.08, therefore the single-layer graphene in the GFeR was confirmed. There are two more peaks P1 (1430 $cm^{-1}$) and P2 (3000 $cm^{-1}$) in Raman shift result, which describe the molecular vibration modes in the ferroelectric polymer, P (VDF-TrFE) [5, 6].

**4. Non-volatile memory device:** To secure the ferroelectricity of the first P(VDF-TrFE) layer, the gate current ($I_G$) was measured by applying triangular gate voltage ($V_G$) between −100 and +100 V. Fig. 3 shows the hysteretic behaviour and two peaks corresponding to the coercive voltages. For the P(VDF-TrFE) film with a thickness of 1.2 µm, the corresponding coercive field was calculated to be 65.8 MV/cm (=79 V/1.2 µm), the value of which is consistent with those in earlier studies [7]. Therefore, ferroelectric polarisation switching is maintained in the device fabricated by stacking. By applying a pulsed $V_G$ ($V_{G,pulse}$) lasting for 1 s from −100 to +100 V, each drain current ($I_D$) was measured and the channel resistance ($R_{CH}$) was extracted, as shown in Fig. 4. Unlike gate current $I_G$ behaviour, the $R_{CH}$ hysteresis is asymmetric, which is explained by the position of the charge neutral point ($V_{CNP}$) of the channel graphene ($G_{CH}$) used in our sample. According to earlier studies [8], the transistors consisting of graphene–ferroelectric hybrid film showed hysteretic $R_{CH}$ characteristics, in which the degree of

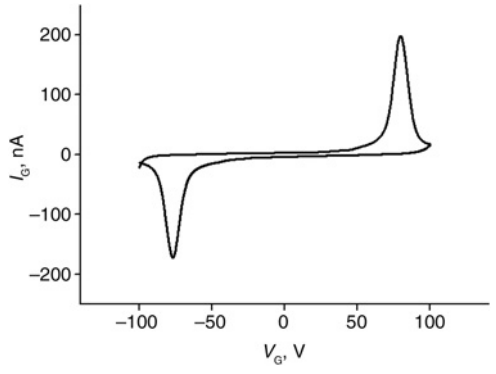


**Fig. 3** *Gate current hysteresis for the gate voltage*

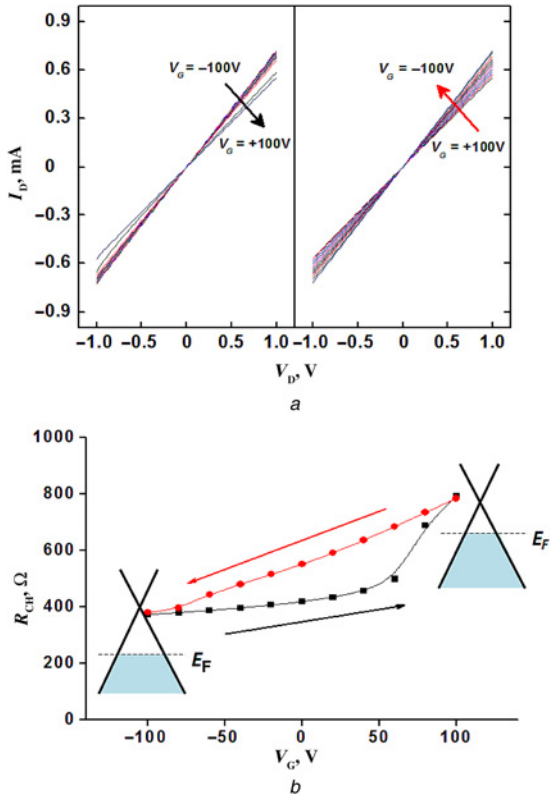


**Fig. 4** *Current–voltage characteristics*
*a* Current–voltage curves as each gate bias modulation
*b* Resistance hysteresis of the channel graphene for the gate voltage ($V_G$)
Steps of $V_G = 20$ V, with the $R_{CH}$ values extracted from the slope in the $I_{DS}$–$V_{DS}$ relationships. The arrow denotes the voltage sweep direction. Insets represent the relative positions of the Fermi level ($E_F$) in Dirac cones

symmetry in $R_{CH}$ depends on $V_{CNP}$, from which our sample corresponds to highly p-doped graphene. After the application of a $V_{G,pulse}$ of +100 V, the Fermi level of graphene will locate closer to the Dirac point than in the case of application of $V_{G,pulse}$ of −100 V; thus, the applications of positive gate voltage deplete the carriers in graphene, resulting in a relatively highly resistant state.

To secure bistability of graphene–ferroelectric transistor, its retention performance was measured as shown in Fig. 5. After the application of a $V_{G,pulse}$ of +100 V, the gate electrode was floated and the $R_{CH}$ values were extracted by measuring $I_D$. Initially, a high-resistance state of 1200 Ω was measured. After a few seconds had elapsed, the resistance $R_{CH}$ decreased to <800 Ω. After an abrupt transition, $R_{CH}$ was gradually reduced. On the other hand, with an application of a $V_{G,pulse}$ of −100 V, $R_{CH}$ ($t$ = 0) was noted in a low-resistance state of 400 Ω, gradually increasing after an initial abrupt transition within a few seconds, similar to the findings in a high-resistance state. In general, the retention performance of a ferroelectric-gated field-effect transistor is determined by charges injected from the semiconductor channel to the interface layer between the ferroelectric and the semiconductor [9, 10]. The injected charges are trapped inside the interface layer, which results in the screening of the polarisation field. Therefore, mobile carriers in the channel area can be liberated from the ferroelectric polarisation in time. As shown in Fig. 5*a*, log($R_{CH}$) after 1000 s changes linearly in time for both a high-resistance state and a low-resistance state. In this linear regime, the injection current $J$ is described as follows:

$$J = \alpha E_i \tag{1}$$



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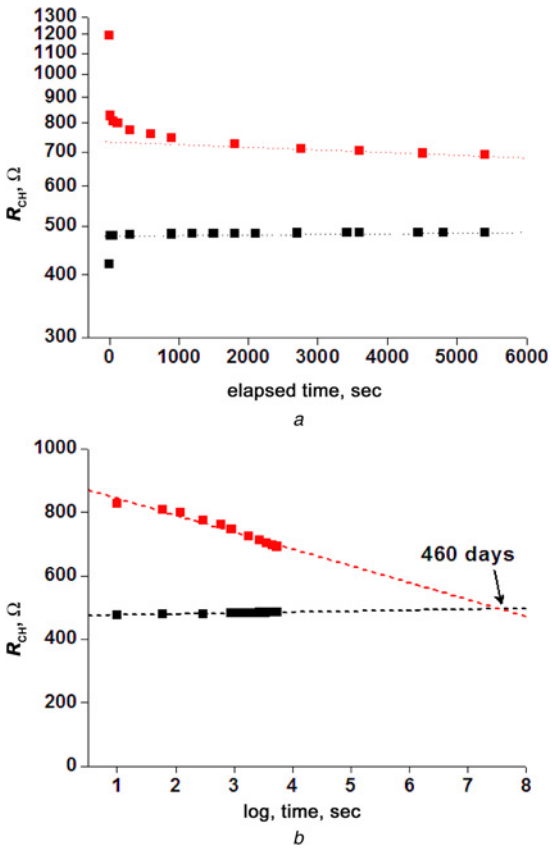


**Fig. 5** *Retention times of the channel resistances as measured by pulsed gate voltages for +100 V (red) and −100 V (black)*
*a* Log-scaled resistance of the linear time scale
*b* Linear-scaled resistance of the log time scale

Here $E_i$ is the electric field induced in the interface layer and $\alpha$ is a proportional constant. The electric field $E_i$ is an exponential decay function of time

$$E_i \propto \exp\left(\frac{-\alpha t}{\varepsilon_i \varepsilon_0}\right) \tag{2}$$

In this equation, $\varepsilon_i$ is the dielectric constant of the interfacial layer and $\varepsilon_0$ is the permittivity of a vacuum. As conjectured from (1) and (2) and the relationship between $\log(R_{CH})$ and the elapsed time in Fig. 5*a*, it is clear that the retention time of the ferroelectric-gated field-effect transistor fabricated by consecutively stacking is governed by the mechanisms of charge injection and screening at the interface of the graphene and the ferroelectric layer.

To estimate the maximum retention time of bistability, Fig. 5*a* was re-plotted with a linear-scaled $R_{CH}$ and the log-scaled time relationship in Fig. 5*b*. By extrapolating two fitted lines, two lines crossover at 460 days after recording, indicating that this device is compatible with devices fabricated by conventional processes.

Compared with previous publications [3, 10], our sample shows a short period to settle on stable resistance state, which enables our device on operating more reliably. Previous results used a nearly neutral graphene, thus the charge neutral point is located near zero voltage. In other words, the carrier type of graphene can be flipped from electron to hole or vice versa by ferroelectric polarisation switching. For the case of electron, the doping concentration of graphene can be time dependent because of injection of counterpart dopant from environment [11]. The graphene used in our device, however, was highly doped enough to maintain its majority carrier type from ferroelectric polarisation as shown in Fig. 4*b*. If

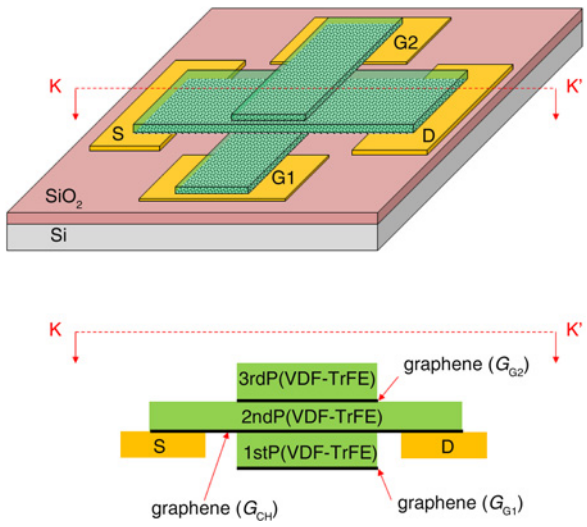


**Fig. 6** *Graphene field-effect transistor fabricated by stacking three ferroelectric–graphene hybrid ribbons at right angles*
*a* Schematic diagram of logic-gate device
*b* Cross-sectional view of K–K′

the initial doping concentration is less than polarisation, the hysteresis loop would have shown two infection points, one is in forward sweep, and the other is in reverse sweep.

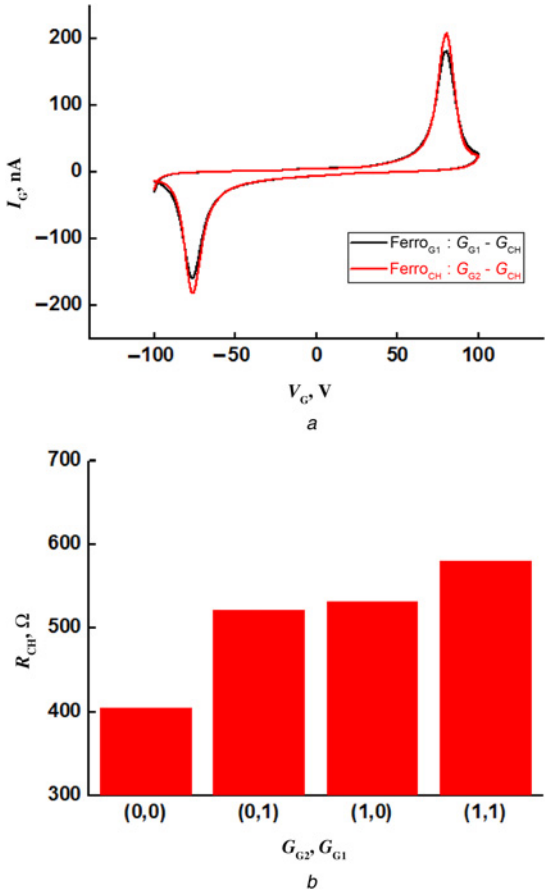


**Fig. 7** *Logic-gate operation*
*a* Gate current hysteresis for the gate voltage
*b* Logic-gate operations of channel resistance for two gate inputs


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**5. Logic-gate device:** By stacking three different GFeR at right angles, a logic-gate device could be fabricated as shown in Fig. 6. Fig. 6*b* represent the cross-sectional view of the K–K′ dotted line in Fig. 5*a*, in which the ferroelectric film in the first GFeR [1st P(VDF-TrFE)] and the second GFeR [2nd P (VDF-TrFE)] act as gate dielectric and the graphene in the second GFeR acts as a common channel in two vertically stacked field-effect transistors. The graphene layers in the first GFeR and the third GFeR act as gate electrodes, $G_{G1}$ and $G_{G2}$. The ferroelectric film in the third GFeR [3rd P(VDF-TrFE)] encapsulates the gate graphene, $G_{G2}$ as depicted in Fig. 6*a*.

To secure the ferroelectricity of the first and the second P (VDF-TrFE) films, the each gate current ($I_G$) was measured by applying triangular gate voltage ($V_G$) between −100 and +100 V. Fig. 7*a* shows two hysteretic loops for two capacitors, $G_{G1}$–1st P (VDF–TrFE)–$G_{CH}$ and $G_{G2}$–2nd P(VDF–TrFE)–$G_{CH}$. Two hysteresis loops are almost identical. By assigning $V_G$ of +100 and −100 V to logic state 1 and 0, channel resistance represents the output of logic gate. When ($G_{G2}$, $G_{G1}$) is applied to (1, 1), p-type graphene is mostly depleted, resulting in a highest resistance state. Reversely, ($G_{G2}$, $G_{G1}$) = (0, 0) accumulates holes, so the channel resistance is mostly reduced. (0, 1) and (1, 0) represent the intermediate resistance values. If reference resistance level is defined as a certain value between resistance values of (0, 0) and (0, 1), the logic gate operates as OR gate. Also, if reference resistance level is defined as a certain value between resistance values of (0, 1) and (1, 1), the logic gate operates as AND gate. Fig. 7*b* shows the channel resistance ($R_{CH}$) depending on the application of two input gate voltages, $G_{G1}$ and $G_{G2}$.

**6. Conclusion:** A ferroelectric-gated graphene field-effect transistor was fabricated by stacking two distinct GFeRs. Electric gating induced ferroelectric polarisation switching, which affected the resistance of the channel graphene. By extrapolating the channel resistances given the relationship of the log-scaled resistance and time, bistable resistance states were maintained separately for 460 days. Further optimisation of the interface between the graphene and the ferroelectric layer will offer much longer data retention times. Also, the basic concept to fabricate the bistable memory device was applied to the logic-gate device, which could be easily fabricated by repetitive stacking of GFeRs. Additionally, low-voltage operating memory and logic-gate devices will also be possible if the ferroelectric film is scaled down and the transfer process is elaborated automatically. It is expected that the method introduced here can be used for the fabrication of high-performance organic memory devices on diverse flexible substrates.

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