Optical storage behaviour in InAs quantum dots embedded in GaAs quantum well structure

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Published in Micro & Nano Letters; Received on 25th May 2016; Accepted on 16th August 2016

The optical storage behaviour of InAs quantum dots (QDs) device has been investigated by testing capacitance–voltage (*C–V*) and current–voltage (*I–V*) character. Since QDs are embedded in the GaAs quantum well, it can be charged by the spatial separation of electrons and holes. When the device is biased in a storage mode, the optical excitation with the photon energy larger than the energy gap gives rise to a step jump in the responsive current, which is previously stored in the device during the illumination. The holes in the QDs which represent the stored information are storage and deletion by bias. The storage time is on the order of milliseconds as measured by pulsed photovoltage/photocurrent response ratio of the device. The device structure can be used as a photonic memory cell because of long storage time and fast retrieval of photons. Moreover, the memory operation can be carried out by applying a lower voltage.

1. Introduction: Exploitation of semiconductor-microstructure based photonic memory cells has recently been motivated by their potential applications in all-optical computers and optical signal processing systems [1–9]. Photonic memory cell may act as an optical dynamic random access memory in all-optical computers, while it may also serve as either a storage unit or a delay unit in optical signal processing systems [3]. Memory operation for III–V quantum dot (QD) structures has been demonstrated either based on optically [4–6] or electrically controlled charge storage [7–9].

Moreover, the read and write process in QD devices require lower operation voltages since tunnelling is employed for carrier injection and depletion [10]. Already these devices were found to possess higher read and write speeds, more storage capacity, greater endurance, and more reliable in comparison to other non-volatile memory devices [11, 12].

The QDs have shown stronger confinement of holes that could be applied in memories. Recently, it has been reported on exciton storage in self-assembled InAs dots in GaAs well in all-electronic structure [2, 13]. The approach of the memory concept is based on created excitons by dissociation and separate storage of the optical electrons and holes [2, 13]. This Letter reports the storage phenomenon measured by the *I–V* curve at different light intensities. It has proved by experiments that the storage time is related to the duration of the illumination.

2. Experimental: The sample was grown by molecular beam epitaxy (MBE) on an n^+-type (1 0 0) GaAs substrate. After the growth of a Si-doped 10^{18} cm^{-3} 1 µm GaAs buffer layer and an undoped 30 nm GaAs spacer, the undoped double barrier structure was deposited in the sequence of the first 25 nm AlAs barrier, a 3 nm GaAs interlayer, a 6 nm $In_{0.15}Ga_{0.85}As$ QW, a 45 nm GaAs well, a 1.8 ML self-assembled InAs QD layer with a 5 nm GaAs overlayer and the second 25 nm AlAs barrier. On the top, an undoped 30 nm GaAs spacer and a Si-doped 10^{18} cm^{-3} 30 nm GaAs capping layer are overgrown [14, 15].

By using standard photolithography the wafer is processed into rectangular mesas and ohmic contacts are separately made to the top and back contact layers by evaporating Au/Ge/Ni alloying with square aperture left for the optical access [14, 15]. The back contact is formed on the n^+-GaAs substrate by evaporating and alloying. The energy band diagram of the device is shown in Fig. 1.

3. Results and discussion: The *I–V* characteristic of the device is measured by a Newport-power-meter-model 1936C and a Keithley 4200-SCS, with different 633 nm laser intensities as shown in Fig. 2. As the laser intensity increases from 20 to 200 nW, the photocurrent increase in positive bias direction. The response current shows a step-like enhancement when the forward biased beyond +1.4 V. When the photon energy is the smaller than 1.42 eV bandgap of GaAs, the step-like enhancement no longer appears under both forward and reverse biases. Due to the spatial separation of electrons and holes, as well as the additional in-plane localisation provided by the QDs, excess electrons and holes can be stored enough long time [14–16]. The storage time of the device is shown on the order of milliseconds by pulsed photocurrent response. Simultaneous display the device can store holes for about ms at room temperature.

The *I–V* curve may be divided into three parts as shown in Fig. 2. The first part, electrons and holes increased gradually, which shows the current increased slowly at the illumination of the 633 nm wavelength. The electrons are captured by the thin InGaAs QW. The similar process will also occur to holes, what will be trapped in the QDs. This process can be interpreted as Writing '1'. The second part, since the light intensity is constant, so that the electrons and holes have a certain proportion, then QDs are not saturated at the time, and holes trapped in the QDs. Due to energy restrictions, QDs cannot transit from one energy level to another level. So the holes can be stored for a long time in InAs QDs until the device is applied a higher voltage. This process can be interpreted as Storage. The third part, the QD energy level occur transition at a higher bias voltage. The stored holes tunnel which in a high electric field, and the response current rapidly increased. This process can be interpreted as Erase '0' as depicted in Fig. 3.

Due to the number of QD storing holes, the storage time is longer in the large light intensity. The bias voltage of charge storage is about 1.6 V, erase voltage probably greater than 2 V. The sample is under about 1.6 V fixed bias, the laser beam (633 nm) through the chopper to illuminate to the sample, and then test the photocurrent/photovoltage transient response with pulsed light. The optical frequency has changed from 100 to 250 Hz. The laser light intensity was 1 mW. The weak signal is read out through the oscilloscope internal resistance (about 1 MΩ) of the amplifier. The storage time measured is shown in Fig. 4. From the diagram, the storage time is 4.8 ms at 100 Hz longer than 250 Hz due tothe duration of the illumination. The

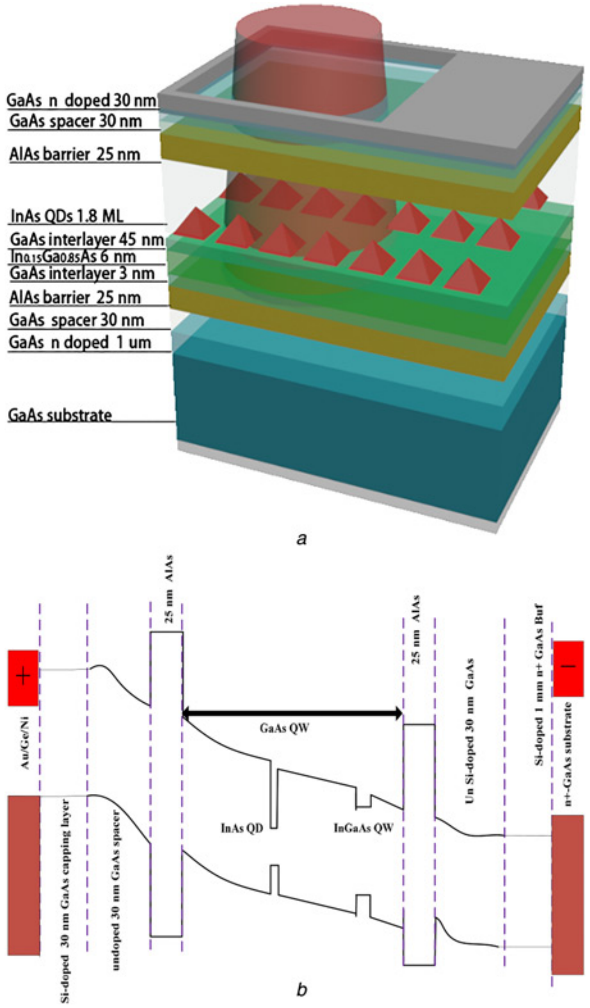

Fig. 1 *Energy band diagram of the device*
a Three-dimensional diagram of the device
b Conduction-band and valence-band diagram of the device

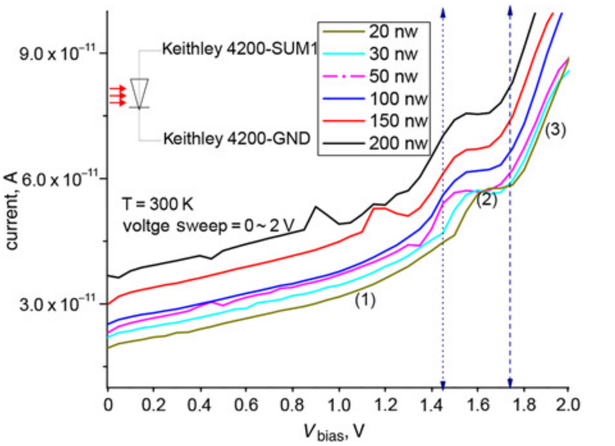

Fig. 2 *I–V curve from 20 to 200 nW under the illumination of the 633 nm wavelength*

experiments show that maximum storage time is 0.6 s in low optical frequency.

To verify storage mechanism of a certain light intensity, we choose light intensity changed from 200 to 600 nW to observe the storage phenomenon of the *C–V* curve. From Fig. 5, some basic experimental phenomena can be seen. The storage capacity

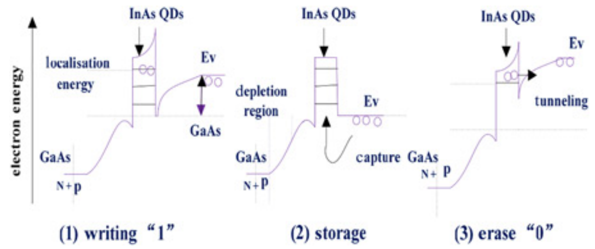

Fig. 3 *Storage mechanism of the InAs QDs*

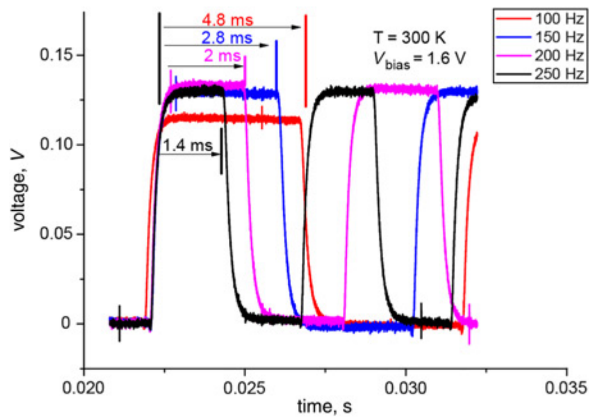

Fig. 4 *Storage time of the device against photovoltage/photocurrent response at different optical frequencies*

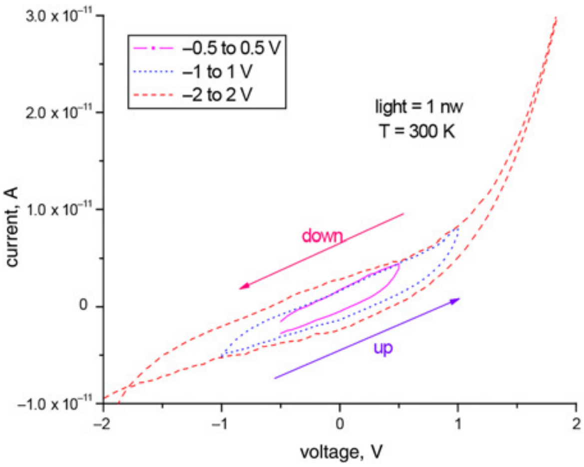

Fig. 5 *I–V sweeps of the p–i–n diode containing InAs QDs*

increases with the light intensity increase. By the formula $I = Cd(u)/d(t)$, the I, C and $d(u)/d(t)$ is light current, the capacitance and the voltage variation rate, respectively. When the light intensity increases and the voltage change rate fixed at a certain point, the value of the capacitance is larger. From the *I–V* curve we can see, the storage capacity increases in the lower voltage area. The storage capacity of the QDs reached the maximum at about 2 V from the *C–V* curve, the tunnelling effect occurred. As the tunnelling of the holes inside QDs gradually being released, the amount of charges stored decreased, so that the capacitance value decreased. The storage holes of the QDs are basically full about 1.6 V. When the bias is greater than about 2.7 V, the QD has basically emptied. So, in the middle of the bias should be the QD storage and release process.

doi: 10.1049/mnl.2016.0339

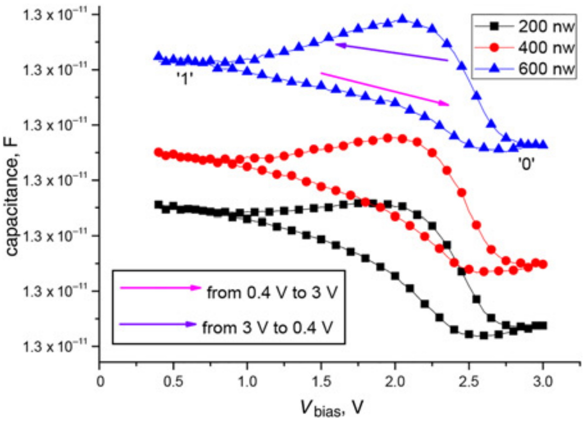

Fig. 6 *C–V sweeps of the p–i–n diode containing InAs QDs and InGaAs well from 200 to 600 nW at 300 K*

The *I–V* curve is shown still in Fig. 5 that can prove the existence of QDs causing the hysteresis phenomenon due to the QD storage charge. From positive scan to negative scan (from −0.5 to 0.5, −1 to 1, −2 to 2, respectively), the electrons and holes are composited, the rest produced the so-called ‘fish eye’ graphics, namely the storage charge of the QDs. Based on the geometry and integral method, the charge of the QDs can be calculated. We find that the size of the so-called ‘fish eye’ is relation to the bias voltage, which the voltage can limit the QDs energy level transition.

It is emphasised that a hysteresis can be shown in comparison of the up-sweeping and down-sweeping *C–V* curves under the different light intensity as shown in Fig. 5. The above fact implies that a noticeable amount of holes has been transferred back and forth by up-sweeping and down-sweeping of biases. Fig. 5 shows the switching between the two states by the capacitance hysteresis curve of the sample. If the V_{bias} is swept from 0.4 V to the storage situation at 1.6 V, the InAs QDs are full and a smaller capacitance may be observed. The charge carriers tunnel out of the QDs (erasing of the information) at 3 V bias [16]. If the V_{bias} is swept from 3 V to the storage situation at 1.6 V, the InAs QDs are charged with holes and a larger capacitance is observed. So we can define that the storage position has the difference between both capacitance values for 0 and 1 states.

In particular, we find that the number of holes that can be stored in the QDs depends on the duration of the illumination. The storage time is on the order of milliseconds as measured by pulsed photocurrent response of the device. By extending the time for illumination, the storage time is longer about 0.6 s. The limit of the erasing time is measured when the QDs are not sufficiently charged, which femtosecond laser is used as excitation light source. The exciting light of the 800 nW wavelength is used to the InAs QDs device, which is the optimal response wavelength of the devices. The 100 ps erasing pulse is applied to the device at $V_{\text{bias}} = 3$ V. When reduced optical pulsed time (100 ps, cycle 30 µs), the erasing time are 5 ns as shown in Fig. 6. The hysteresis opening at 1.8 V is measured after applying write/erase pulses with reduced pulse widths down to10 ns [17] (Fig. 7).

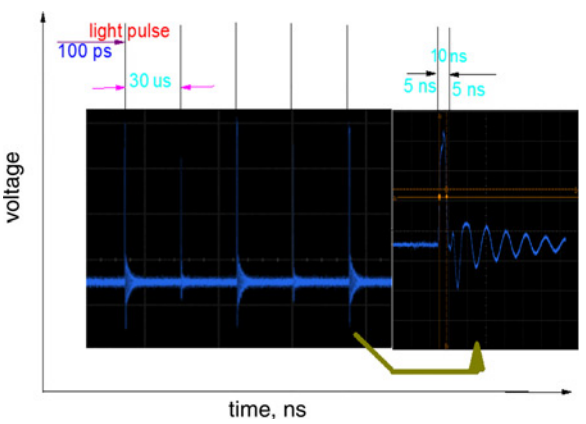

Fig. 7 *Photovoltage response to the sample at 100 ps light pulse*

To verify the QD memory, the writing ‘1’ and erasing ‘0’ can be understood as a QD charging and discharging processes, it required a certain voltage to control. When the pulse width was too short for any charging/discharging of the QDs [17], the writing and erasing pulsed response would vanish in the oscilloscope.

4. Conclusion: In summary, we have demonstrated the mechanism of optical storage and deletion of charge in InAs QDs embedded in GaAs quantum well. We verify the storage properties of the QDs by the step shape of the *I–V* curve. Moreover, the storage time depends on the illumination time and the light intensity. The storage time is measured by pulsed photovoltage/photocurrent response of the device at different optical frequencies. The storage time is 0.6 s at room temperature. The holes in the QDs which represent the stored information are here storage ($V_{\text{bias}} = 1.6$ V) and deletion ($V_{\text{bias}} = 3$ V) by measuring the capacitance of the p–i–n diode. This process can also be understood as charging and discharging of QDs. We find 5 ns erasing time $V_{\text{bias}} = 3$ V. These results show the self-organised QDs in GaAs quantum well can be used as a very fast detector for the writing and erasing in a memory structure.

5. Acknowledgments: This work was supported by National Scientific Research Plan of China (grant no. 2011CB932903) and State Scientific and Technological Commission of Shanghai (grant no. 118014546).

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doi: 10.1049/mnl.2016.0339