Dicing-free SOI process based on wet release technology

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A simple, low-cost and reliable dicing-free silicon-on-insulator (SOI) process is presented for solving three major challenges in manufacturing the microelectromechanical systems devices, i.e. stiction, notching and dicing damage. In this process, the cavity is used and patterned on the handle layer to solve the stiction problem, and the exposed oxide is removed in hydrofluoric acid (HF) solution before deep reactive ion etching (DRIE) on the structure layer to eliminate the notching effect's impact. The dies are attached temporally to a designed frame by the silicon dioxide. After removing the oxide using HF solution, the dies are separated from the wafer cleanly without dicing damage. The layout design rules on the front side and backside patterns are established. Furthermore, a grooved carrier wafer with specific design rules was introduced to enhance the yield rate of the process. Finally, a tuning fork gyroscope was fabricated to demonstrate the proposed fabrication process and a yield rate of over 81% was achieved. The process solves the stiction, notching and dicing damage problems only involving the apparatus associated with lithography and DRIE, offering an economic and complete SOI process solution.

1. Introduction: The silicon-on-insulator (SOI) technology has been widely utilised for academic research and commercial manufacture in microelectromechanical systems (MEMS) fields because it can provide high aspect ratio structures, precise control of the dimensions and low-cost fabrication [1, 2]. The SOI process typically starts with patterning the device features on the structure layer by deep reactive ion etching (DRIE), followed by removing the intermediate oxide layer to release the moveable structure and finally the wafer was diced into dies [3].

However, the SOI process usually faces three major challenges in manufacturing the MEMS devices, i.e. stiction, notching and dicing damage. First, the capillary forces would pull the devices structure down to the handle layer and adhered together permanently, that is, the so-called stiction [4]. Second, notching effect happens when the reaction ions accumulate on the oxide layer, leading to over-etching and bad roughness at the bottom of the device structures [5]. Third, the traditional dicing methods using blades will create debris and the water flow will damage the delicate device features [6]. The three challenges can be solved by using some processes with the aid of special machines. For example, the stiction problem can be addressed by supercritical drying [7] or vapour hydrofluoric acid (HF) technology [8]; the notching can be suppressed by bias pulsing procedure [9]; and the dicing damage can be avoided by using laser dicing system [10] or bonding a cap wafer to the SOI wafer [11].

To solve the three challenges simply and economically without additional machines, much effort have been made. For example, researchers proposed to release the device structures using the notching effect [12] to avoid the stiction by roughening the bottom surface of the structure layer. In our previous work, we improved this process by a selective roughening on the bottom surface of the structure layer [13]. Thus, the thickness-sensitive structures such as the suspension beams are not damaged by the notching effect. However, the selective roughening SOI process is unsatisfactory because of the imperfect profile of proof mass and combs and widely distributed etching holes. To form a backside cavity on the handle layer is another favourable solution to solve the stiction problem [14]. Consequently, any physical contact between the released proof mass and the underneath handle layer is ruled out. We improved this process with a dicing-free capability by using the lag effect of the DRIE to form narrow breaking trenches [15]. In that work, the notching problem is completely solved by the removal of the oxide layer underneath the device structures before patterning the device features. Though in the process the stiction and notching problems are solved satisfactorily, and the dies are also separated free of dicing apparatus, the vibration and debris during the manually breaking step become a potential problem to the delicate device features.

Overstolz *et al.* present a clean dicing-free process based on vapour HF technology [16]. In this process, the defined surrounding trenches on the handle layer and structural layer are shifted by a certain displacement to create overlapping area. Etching the silicon dioxide on the overlapping area using HF vapour phase etching (HF VPE) system, the devices are unloaded from the wafer. This dicing-free process is extended by Sari *et al.* [17] further by increasing the allowable proof mass from 2×2 mm^2 to 4×7 mm^2. Though this process solves the troublesome stiction and dicing damage issues, the notching problems still remain because the handle layer is still kept under the structure layer during the DRIE. Furthermore, the dicing-free process depends on the complicated, expensive and dangerous HF VPE system in releasing the bulky handle layer block.

In this Letter, we propose a simple, low-cost and reliable dicing-free SOI process based on wet release technology, offering a total solution to the three major challenges. In this process, the cavity is used and patterned on the handle layer to solve the stiction problem, and the exposed oxide is removed in HF solution before DRIE on the structure layer to eliminate the notching effect's impact. The surrounding trenches on the handle layer and structural layer are designed and shifted by a certain displacement forming an overlapping area between the two layers. Removing the oxide on the overlapping area, the dies are separated from the wafer cleanly. Different from the process in [16, 17], this process etches off the bulky handle layer under the movable structures in advance to eliminate the notching effect's impact and simultaneously avoid using the HF VPE system in the following releasing step. To prevent the SOI wafer from cracking in the double-sided or etching through process, a grooved carrier wafer (GCW) was introduced in our previous work [18] to bond it to the SOI wafer. Thus, the pressure inside and outside the cavity can be balanced. However, the design rules of GCW are not specified. In this work, we also propose the corresponding design rules for the groove design to improve the process yield further. This process only involves the apparatus that associated with lithography and DRIE and requires no additional expensive apparatus such as HF

VPE system, dicing machines etc. making it particularly suitable for academic research and prototypes fabrication in a low-cost way.

2. Design rules of the dicing-free SOI process

2.1. Dicing-free SOI process flow: An SOI wafer that consists of a structural layer of 60 μm, a handle layer of 400 μm and an intermediate oxide layer of 4 μm is employed in this work to demonstrate the proposed process flow (Fig. 1). The process starts with forming a mask on the handle layer using the thick photoresist AZ4620 (Fig. 1*a*). Then the cavity and the backside trenches are etched in handle layer by DRIE, followed by removing the photoresist in acetone and etching off the exposed oxide in HF solution (Fig. 1*b*). Third, the photoresist EPI680 is patterned on the structure layer and then the handle layer is bonded to the GCW using photoresist (Fig. 1*c*). Fourth, the device features and the front side trenches are formed in the structure layer by DRIE (Fig. 1*d*). Soaking the bonded wafers in acetone for about half an hour, the SOI wafer is separated from GCW. At this time, the devices attach to the SOI wafer only through the oxide on the overlapping area (Fig. 1*e*). Finally, the devices are detached from the wafer by removing the oxide on the overlapping area using HF solution (Fig. 1*f*).

2.2. Layout design rules: To explain the design rules of the proposed process, an in-plane *Z*-axis tuning fork MEMS gyroscope is taken as an example for fabrication demonstration. Two masks are needed in this process to pattern the handle layer and structure layer. Thus, the layout of the gyroscope consists of two layers as presented in Fig. 2, defining the front side and backside features. The layout design rules for the SOI process are listed as follows:

I. *Design rules for W_{bt}:* On the backside handle layer, there are two major structure patterns. The width of the cavity is determined by the size of the proof mass, which is usually in a size of several hundred to thousand microns. The backside trenches are used to separate the gyroscope with the SOI wafer on the handle layer. It should be kept in a narrow width to save the layout area. Then the lag effect tends to become severe in forming the comparatively narrow backside trenches. In this process, the lag effect can be neglected by enlarging the width of the backside trenches (W_{bt}) to 100 μm by experimental verification.

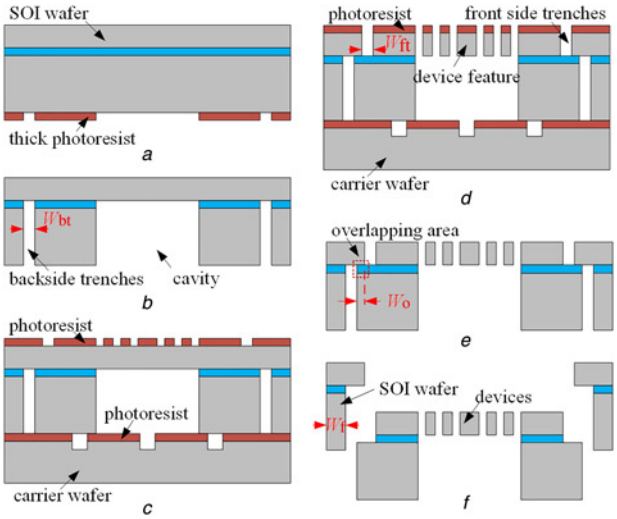

Fig. 1 *Fabrication flow of the dicing-free SOI process*
a Forming photoresist mask
b Patterning the backside features
c Forming photoresist mask and bonding wafers
d Patterning the front side features
e Detaching the wafers and removing the photoresist
f Releasing the devices

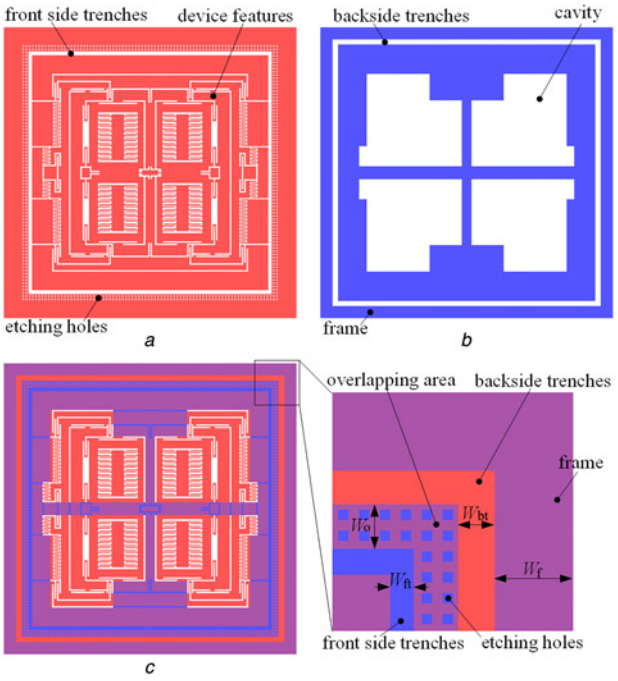

Fig. 2 *Schematic layout of the gyroscope*
a Layout of the front side features
b Layout of the backside features.
c Front and backside layout shown together with the overlapping area zoomed in

II. *Design rules for W_{ft}:* On the front side structural layer, there are two major structure patterns. The typical gap of the device is usually between 2 and 20 μm since the device is mainly consisted of the comb finger capacitors, beams and proof mass. Therefore, the front side trenches used to isolate the gyroscope with the SOI wafer on the structure layer can be set as 2–20 μm to eliminate the lag effect. In this gyroscope design, the parameter is set as 20 μm.

III. *Design rules for W_o:* The overlapping width (W_o) is a very important parameter, which is generated by shifting a certain displacement between the front side and backside trenches to attach the gyroscope to the SOI wafer during the DRIE process. To ensure the enough attaching strength, the W_o should be larger than 50 μm. However, the larger W_o, the larger layout area will be wasted, and it will become more difficult to etch off the silicon dioxide on the overlapping area. In this gyroscope design, the width is set as 100 μm.

IV. *Design rules for square etching holes:* The square etching holes with side length (L_{eh}) of 20 μm are widely distributed on the overlapping area of the structure layer for easy release and detachment. By making a trade-off between the release time and the attaching strength, the distance between every two etching holes (D_{eh}) is set to 20 μm in this gyroscope design.

V. *Design rules for W_f:* A frame needs to be designed to temporarily support the gyroscope before etching off oxide on the overlapping area. The width should be large enough to avoid the frame break during forming the cavity. In this design, the width is set as 1 mm.

2.3. Design rules of the GCW: In the double-sided or etching through process, a silicon or glass wafer is usually bonded to the fabricated SOI wafer to prevent the helium that is used for cooling the SOI wafer from escaping. The bonded wafer is the so-called carrier wafer. However, using the conventional planar carrier wafer, the structure layer tends to crack due to the different pressures between the cavity and the DRIE process

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chamber. To solve this problem, a double-sided polished silicon wafer with the thickness of 500 µm is patterned with orthogonal grooves for balancing the pressure of the two sides of the SOI wafer. The GCW, as schematically shown in Fig. 3, should meet the following design rules to achieve a high yield rate:

VI. *Design rules for D_g and W_g:* The GCW should be strong enough to support the SOI wafer. The strength of the GCW is affected by the depth of the grooves (D_g). Shallower grooves will benefit the strength of the GCW; however, the insufficient depth will result in the blockage of the grooves by the photoresist used to bond the carrier wafer and the SOI wafer. The width of the groove (W_g) should be as small as possible to ensure the enough large adhesion area between the carrier and the SOI wafer. However, the minimum value should be larger than the depth to avoid the blockage. In this design, D_g is set as 20 µm and W_g is set as 100 µm.

VII. *Design rules for P_g:* When the cavity is larger than 1 × 1 mm, the structure cracking happens often due to the pressure difference between the cavity and the DRIE chamber. Thus, at least a groove must be distributed under the cavity to connect the cavity with the chamber. In this design, the cavity is 2.4 × 2.2 mm, thus the distance between every two grooves (P_g) should be <2.2 mm. P_g is set as 2 mm when the W_g is set as 100 µm.

For clarity, the parameters of design rules used in the gyroscope design are summarised and listed in Table 1.

3. Fabrication verification: The process developed in this Letter is verified by fabricating the tuning fork gyroscope step by step. First, the cavity and the backside trenches are formed by backside DRIE and the removal of the exposed oxide, as shown in Fig. 4*a*. The cavity is the premise of avoiding the notching and stiction. Next, the effect of using the GCW can be demonstrated as shown in Fig. 4*b*. No device crack is observed after the front side DRIE. At this moment, the devices adhere to the SOI wafer only via the oxide on the overlapping area (Fig. 1*e*). Removing the oxide on the overlapping area in HF solution, the tuning fork gyroscope (Fig. 5*b*) is unloaded from the SOI wafer (Fig. 5*a*).

In our design, the total number of designed and fabricated gyroscopes on a 4-inch SOI wafer is 88. At last, 72 out of 88 gyroscopes are successfully released and no structure damage is observed under an optical microscope, which indicates a yield of over 81%. Among the 16 failure gyroscopes, 8 gyroscopes are failed by particles in the photoresist, 4 gyroscopes are damaged in fetching the devices from the HF solution and 4 gyroscopes are broken intentionally during the DRIE step to obtain the etching depth parameter.

The front side and backside scanning electron microscopy (SEM) images of the gyroscope are shown in Figs. 6*a* and *b*, respectively. Fig. 6*c* presents the side wall of the gyroscope in which the backside trenches sidewall, front side trenches sidewall and overlapping area are shown in details. Fig. 6*d* demonstrates the bottom surface

Table 1 Design rules parameters used in the gyroscope design

Design rule number	Description	Symbol	Value, µm
I	width of the backside trenches	W_{bt}	100
II	width of the front side trenches	W_{ft}	20
III	width of the overlapping area	W_o	100
IV	length of the etching holes	L_{eh}	20
–	distance of the etching holes	D_{eh}	20
V	width of the frame	W_f	1000
VI	depth of the grooves	D_g	20
–	width of the grooves	W_g	100
VII	distance of the grooves	P_g	2000

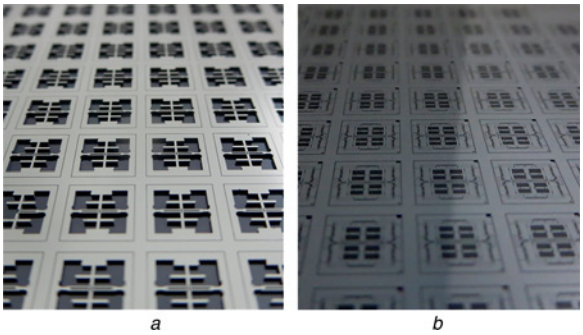

Fig. 4 *Patterning the two side features of the SOI wafer*
a Patterning the backside of the SOI wafer
b Patterning the front side of the SOI wafer

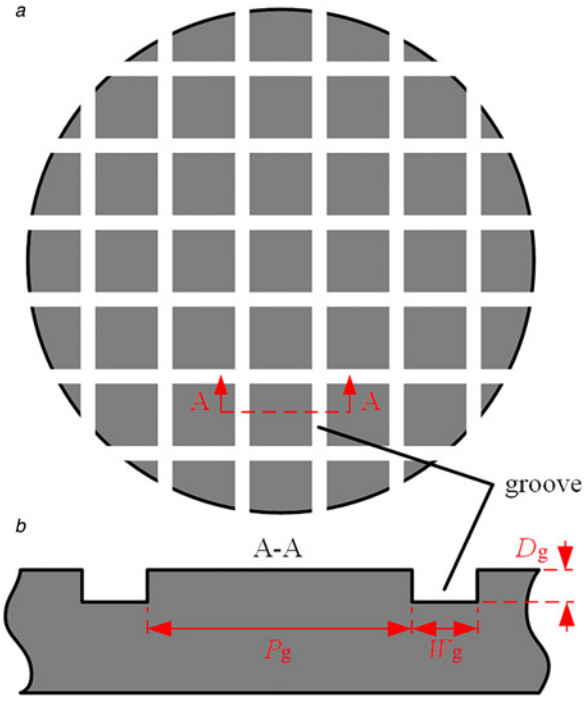

Fig. 3 *Schematic of the GCW*
a Front view of the GCW
b Partial zoomed-in cross-section

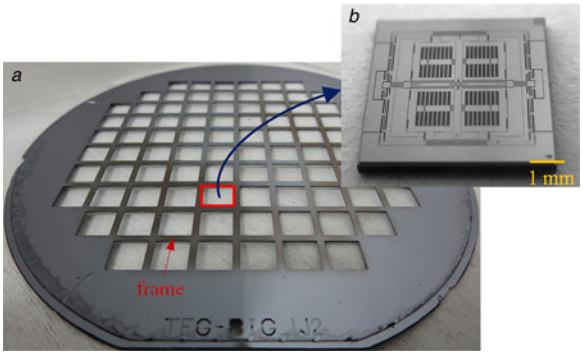

Fig. 5 *Unloading the gyroscope from the SOI wafer*
a SOI wafer with frame remains
b Fabricated gyroscope

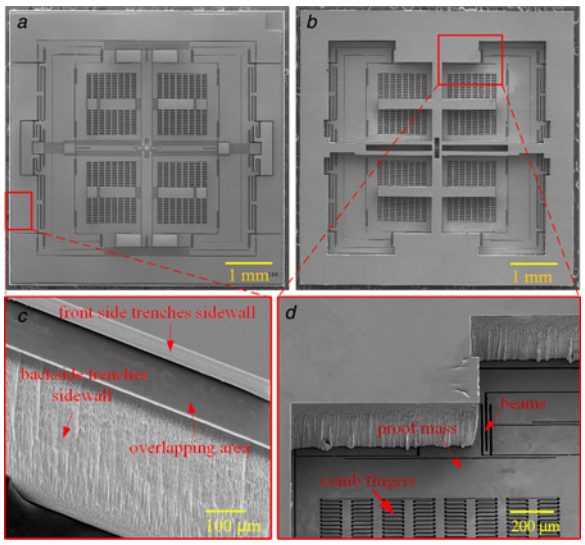

Fig. 6 *SEM of the fabricated gyroscope*
a Front side of the gyroscope
b Backside of the gyroscope
c Side wall of the gyroscope
d Bottom surface of the gyroscope features

of the beams, comb fingers and proof mass showing that no notching occurs at the bottom of the structures. So, it can be seen that the three challenges, i.e. stiction, notching and dicing damage of the SOI process are successfully solved.

4. Conclusions: A simple, low-cost and reliable dicing-free SOI MEMS process with detailed design rules is established and verified in this Letter. The experimental results prove the process can solve the troublesome stiction, notching and dicing damage problems effectively without involving additional expensive apparatus. This process is developed to fabricate MEMS devices for academic research and prototypes fabrication at laboratory level. Thus the process maybe has troubles in automated production for involving the unconventional process such as attaching the carrier wafer.

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6 References

[1] Renard S.: 'Industrial MEMS on SOI', *J. Micromech. Microeng.*, 2000, **10**, (2), pp. 245–249
[2] Zotov S.A., Simon B.R., Trusov A.A., *ET AL.*: 'High quality factor resonant MEMS accelerometer with continuous thermal compensation', *IEEE Sens. J.*, 2015, **15**, (9), pp. 5045–5052
[3] Wang Z.F., Cao W., Shan X.C., *ET AL.*: 'Development of 1 × 4 MEMS-based optical switch', *Sens. Actuators A, Phys.*, 2004, **114**, (1), pp. 80–87
[4] Tas N., Sonnenberg T., Jansen H., *ET AL.*: 'Stiction in surface micromachining', *J. Micromech. Microeng.*, 1999, **6**, (4), pp. 385–397
[5] Kim C.-H., Kim Y.-K.: 'Prevention method of a notching caused by surface charging in silicon reactive ion etching', *J. Micromech. Microeng.*, 2005, **15**, (2), pp. 358–361
[6] Lin J.-W., Cheng M.-H.: 'Investigation of chipping and wear of silicon wafer dicing', *J. Manuf. Process.*, 2014, **16**, (3), pp. 373–378
[7] Resnick P.J., Clews P.J.: 'Whole wafer critical point drying of MEMS devices'. Proc. SPIE, 2001, pp. 189–196
[8] Jang W.I., Choi C.A., Lee M.L., *ET AL.*: 'Fabrication of MEMS devices by using anhydrous HF gas-phase etching with alcoholic vapor', *J. Micromech. Microeng.*, 2002, **12**, pp. 297–306
[9] Laermer F., Urban A.: 'Challenges, developments and applications of silicon deep reactive ion etching', *Microelectron. Eng.*, 2003, **67-68**, pp. 349–355
[10] Venkatakrishnan K., Tan B.: 'Thin silicon wafer dicing with a dual-focused laser beam', *J. Micromech. Microeng.*, 2007, **17**, (12), pp. 2505–2515
[11] Awatani Y., Matsumoto Y., Kato K.: 'Damage free dicing method for MEMS devices'. IEEE/LEOS Int. Conf. Optical MEMs, 2002, pp. 3–4
[12] Haobing L., Chollet F.: 'Layout controlled one-step dry etch and release of MEMS using deep RIE on SOI wafer', *J. Microelectromech. Syst.*, 2006, **15**, (3), pp. 541–547
[13] Chang H., Xie J., Fu Q., *ET AL.*: 'Micromachined inertial measurement unit fabricated by a SOI process with selective roughening under structures', *Micro Nano Lett.*, 2011, **6**, (7), p. 486
[14] Alper S.E., Azgin K., Akin T.: 'A high-performance silicon-on-insulator MEMS gyroscope operating at atmospheric pressure', *Sens. Actuators A, Phys.*, 2007, **135**, pp. 34–42
[15] Xie J., Hao Y., Shen Q., *ET AL.*: 'A dicing-free SOI process for MEMS devices based on the lag effect', *J. Micromech. Microeng.*, 2013, **23**, (12), p. 125033
[16] Overstolz T., Clerc P., Noell W., *ET AL.*: 'A clean wafer-scale chip-release process without dicing based on vapor phase etching'. '17th IEEE Int. Conf. on Micro Electro Mechanical Systems. Maastricht MEMS 2004 Technical Digest', 2004, pp. 717–720
[17] Sari I., Zeimpekis I., Kraft M.: 'A dicing free SOI process for MEMS devices', *Microelectron. Eng.*, 2012, **95**, pp. 121–129
[18] Li E., Li P., Shen Q., *ET AL.*: 'High-accuracy silicon-on-insulator accelerometer with an increased yield rate', *Micro Nano Lett.*, 2015, **10**, (10), pp. 477–482

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