Ultra-low leakage SRAM design with sub-32 nm tunnel FETs for low standby power applications

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Tunnel-field-effect transistors (TFETs) operate by quantum band-to-band tunnelling and display a steeper subthreshold slope than MOSFETs which substantially diminishes the standby current. This work explores the TFET-based SRAM utilisation for Low STandby Power applications. An 8 T TFET SRAM cell operating at $V_{DD} = 1$ V, which, in contrast to other 6 T TFET SRAMs, is write-disturb- and half-selection-free is proposed. Simulations based on 30 nm p- and n-TFETs models relying on I_D, C_{GS}, C_{GD} vs. V_{GS}, and V_{DS} look-up tables extracted from TCAD, indicate that the proposed cell has a Read SNM and a Write SNM of 120 and 200 mV, respectively, which are well above state of the art values repotted in the literature. When utilised in an 128 × 128-bit memory array the proposed cell enables read and write operation at 3.84 GHz and 806 MHz, respectively, and a cell leakage of less than 2fA/bit, which makes it an excellent choice for Internet of Things applications.

1. Introduction: Static power dissipation represents a serious problem that affects nano-scale CMOS circuits. Today, circuit designers face many challenges in their pursuit to limit the negative effects of very short-channel devices, especially the leakage currents. The static power dissipation is of critical concern for many of the growing markets such as sensor networks, Internet of Things, where energy management systems and circuits need to maximise battery life or use energy harvesting technologies. These systems typically operate at very low activity levels and thus experience extended standby periods. In modern system on chips (SoCs) with long standby periods, SRAM leakage is the dominant factor in total energy consumption. Thus, its reduction by means of device, cell and/or architecture level optimisations is the key element towards energy efficient designs. In SRAMs, long channel devices with thick gate oxide are used to suppress leakage but to maintain the cell speed in 100's MHz or GHz, such a solution requires increased device width, which results in extremely prohibitive area cost. For instance, Fukuda *et al.* proposed the use of a 65 nm 6 T SRAM cell built with long-channel and thick-oxide. Over 1000× leakage reduction at room temperature as compared with standard 6 T SRAM design was reported, reaching a value as low as 27fA/b, by reverse biasing the source during standby. A cell area of 2.159 μm^2, almost 10× higher when compared with standard cells, shows the limitations of such strategy, as no advanced CMOS technology is able to offer, today, reduced cell area, and fA/bit leakage.

Possible solutions for solving the leakage problem consists in extending the CMOS platform with other energy efficient devices, such as NEMFET [1], RRAMs [2, 3], and Embedded Flash [4]. However, these devices are limited by their write endurance, low operating frequency, and higher then CMOS operating voltage, making the matching difficult.

Tunnel field effect transistors (TFETs) could be the key element towards ultra-low leakage memory design as they operate by band-to-band tunnelling, which, being different than MOSFET's working principle, is not limiting the theoretical subthreshold slope (S) to 60 mV/dec. as in CMOS' case [5–7]. While optimised TFETs can provide leakage currents (I_{OFF}) in the order of fA/μm [6] one major concern has been the low on current provided by such devices. Recent progress demonstrated fabricated TFETs with drain current of 760 μA/μm [6] while subthreshold slopes as low as 30 mV/dec have been already measured [8]. Such results confirm the TFET good potential for successful utilisation in low power/stand-by power applications and encouraged research on TFET circuits. Yet, the published reports have described mostly TFET-based SRAM cells [9–13], which mimic their CMOS counterparts and have difficulties in obtaining sufficient stability during read and write operations [9–11]. Moreover, the use of the TFETs as access transistors in memory cells is restrained by their uncontrolled conduction under reverse biasing conditions, which consists of the forward activation of *p-i-n* junction with current flowing from source to drain without gate control at negative V_{DS} (referred in literature as unidirectional behaviour [10]). During the write operation, the TFET's unidirectionality seriously increases the power consumption for all cells in write-disturb conditions (cells that are not written, but on the same column as the accessed ones). This leads to high parasitic currents between bitcells and bitlines. The parasitic current appears around 0.6 V for silicon TFETs in reverse bias regime (negative V_{DS}) due to the turn-on of the *p-i-n* diode [14], a reason for which the researchers are forced to target very low V_{DD}s. Moreover, aggressively scaled supply voltage values result in an even larger difficulty in achieving sufficient stability margins and operation speed in active mode. New architectural solutions were developed to improve the single cell stability but cells proposed in such reports [11, 13, 15] still suffer from *half-selection*, *write-disturb* (WD), and soft errors when organised in memory cell arrays.

This work targets the investigation of TFET based SRAMs for Low STandby Power (LSTP) application with ultra-low leakage

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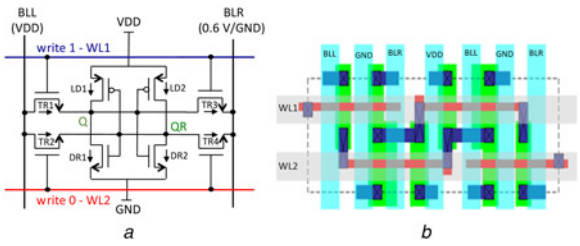

Fig. 1 *Proposed SRAM architecture*
a Schematic representation of 8 T TFET SRAM cell
b 8 T cell layout with 2 bitline connections. Top connections made with Metal 2 for BLL, BLR, VDD, GND (vertical), and Metal 3 for WL1 and WL2 (horizontal)

for long battery life and/or energy harvesting. The TFET devices used for analysis are published in [16] and are compatible with FDSOI-CMOS for fabrication. We propose an 8 T TFET SRAM bit-cell which overcomes half-selection and write-disturb architecture level issues. The new design exhibits ultra-low leakage (<2fA/bit @ 1 V V_{DD}), high operation speed (100's MHz to GHz range), and similar area as state of the art 8T-CMOS SRAM cells. In contrast to Saripalli's design [9], which is limited in dynamic performance, our cell is fully compatible with dynamic voltage and frequency scaling. The leakage induced by the unidirectional TFET behaviour is also avoided and the new cell maintains reasonable stability in all operating modes without relying on any assist technique.

The Letter is organised as follows. In Section 2, the proposed 8 T SRAM cell organisation and layout are described. Section 3 presents the cell operation and its performance (speed and stability). Finally, Section 4 provides a comparative analysis of the energy efficiency of the proposed cell and the one of standard CMOS SRAMs. Conclusions and comments on future work are presented in Section 5.

2. 8T TFET SRAM cell: The proposed SRAM architecture is depicted in Fig. 1*a*. The novel cell is designed with dual word lines (WL1 and WL2) and a pair of bitlines (BLL and BLR). Read makes use of BLL and WL1 only, while both bitlines and either of the wordline depending on the to be written data value are used for write. In retention, BLL is set to VDD and the right bitline (BLR) is kept at 0.6 V.

The chosen device widths are 200 nm for loads and drivers (LD1÷2 and DR1÷2), and 100 nm for access (TR1÷4). The sizing, unconventional when compared with a typical 6 T CMOS SRAM cell, is adjusted to properly balance read and write stabilities and optimise the bitline capacitance.

The physical implementation of the proposed cell is similar to 8 T Dual-Port (DP) cell from [17]. Since in a DP cell each access transistor is connected to a separate bitline, the layout has four physical bitline connections. In order to obtain compatibility with our cell (Fig. 1*b*) without performing area consuming layout modifications on the single-cell level, the two vertical BLL and BLR lines are tied

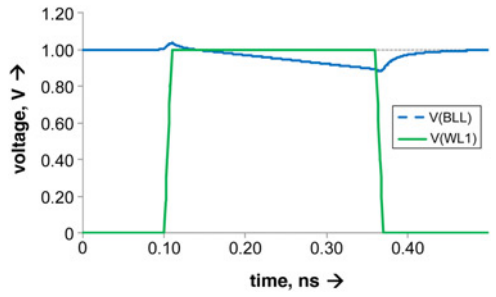

Fig. 2 *Wordline and bitline signals during read operation*

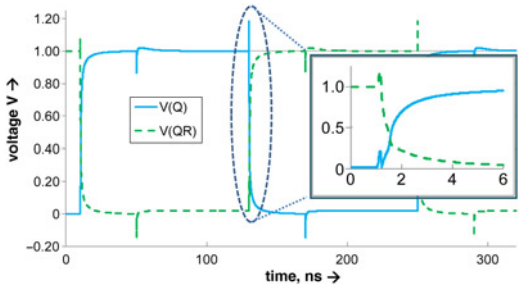

Fig. 3 *Waveform display for storing nodes Q and QR during write operation; inset highlighting of write operation speed*

together at the I/O side. Using an industrial cell layout as a reference and device sizes as previously defined in this section we obtained a cell area of 0.338 μm^2, which means a 29% area overhead when compared with a 6 T cell without the two additional access transistors and the same transistor sizing.

3. Operation and performance: The read operation is similar to that of a typical 6 T SRAM, with the difference that it is left-sided and always uses WL1. The sensing depends on the BLL being discharged through the cell when '0' is stored on Q node (Fig. 1*a*), or remaining at V_{DD} when Q value is '1'. This operation for the former case is presented in Fig. 2. The minimum (critical) wordline pulse length required to pull down the BLL voltage by 100 mV (typical requirement) is 260 ps at $V_{DD} = 1$ V. Several methods have been proposed for single-ended read in literature [18–20] for CMOS memories. Such methods may be used directly, or with minor modifications, to implement TFET-based sensing circuits that operate in conjunction with the proposed 8T-cell.

To perform a write operation BLR is pulled down to GND and depending on the value to be written in the cell, either WL1 or WL2 is set to V_{DD}. Fig. 3 depicts two consecutive '1' to '0' write cycles. Due to the existence of two wordlines for each cell, either a '0' or a '1' can be written into the cells on the same wordline at a time. As a result, in order to write a full word, two consecutive write phases have to be performed, writing separately '0s' and '1s' in the respective cells. A minimum WL pulse width of 1.24 ns is required for a successful cell write at 1 V supply. Since, TFET leakage is fairly independent of the supply voltage value, performance can be improved by a factor of 2.5× by increasing it to 1.2 V without impacting the bitcell leakage.

In the proposed cell, V_{DS} never goes below −0.6 V for any device in the SRAM cell array, resulting in parasitic current suppression. Assume Q = '1' and QR = '0'; under this conditions, TR3 operates in reverse mode with its $V_{DS} = -0.6$ V. In this condition, the TFET current remains in the fA range, therefore not causing significant parasitic current (as explained in introduction). The other transfer transistor connected to the BLR (TR4) has its drain at the node storing '1' and hence operates at a positive V_{DS} whereas the current for $V_{GS} = 0$ is always very low. This approach allows for maintaining negligible leakage for WD cells for all operating conditions, hence avoiding the WD problem. For the other case when node QR stores an '1', the total leakage is the same with TR3 operating in forward bias and TR4 in reverse bias.

The results presented in this section demonstrate that TFET circuits can be competitive with LP CMOS also in terms of speed, as long as nominal or larger than nominal (for our case greater than 1 V) supply voltages are used. In the presented 8 T TFET cell, the leakage is carefully controlled by avoiding excessive device reverse biasing. The design supports higher operating frequency with the increase of supply voltage.

The obtained noise-margin values are approximately 120 mV for read static noise margin (RSNM) and 200 mV write static noise

Table 1 Summary of active energy evaluation for read, write, and average per active cycle (assuming one read for one write)

Cell type	E_{READ} (fJ)	E_{WRITE} (fJ)	E_{AVG} (fJ)	P_{Leak} (W)
128 rows × 128 columns				
8 T TFET	46.4	205	126	3.28×10^{-11}
6 T 0.120 μm^2	99.0	202	151	2.39×10^{-7}
6 T 0.197 μm^2	213	425	319	1.30×10^{-7}
256 rows × 64 columns				
8 T TFET	32.6	275	154	1.64×10^{-11}
6 T 0.120 μm^2	95.9	391	243	1.19×10^{-7}
6 T 0.197 μm^2	207	824	515	6.49×10^{-8}
64 rows × 256 columns				
8 T TFET	73.9	212	143	8.19×10^{-12}
6 T 0.120 μm^2	106	118	112	5.97×10^{-8}
6 T 0.197 μm^2	229	248	238	3.24×10^{-8}

margin (WSNM). These values represent a 5× and 8× improvement when compared with the standard 6 T TFET SRAM cell in balanced case counterparts. These values can be further increased through the application of appropriate assist techniques [21, 22] such as, for instance, negative bitline voltage during write [21].

4. Energy efficiency: To evaluate the energy efficiency during the active mode, three cells were considered for the comparison: (i) the 8 T TFET cell presented in the previous section, (ii) the high speed (HS) 0.197 μm^2 6 T cell [23], and (iii) the high density (HD) 0.120 μm^2 6 T cell [23]. Cells (ii) and (iii) were simulated using 32 nm LP PTM models and their sizing their sizing was extrapolated based on [24] and adjusted to match the bitcell area.

The evaluation was limited to the memory array level only. The effects taken into account consisted in: (i) the bitline discharge during read, assumed at 100 mV for all cells, (ii) the wordline activation during write and read, (iii) the bitline discharge during write, and (iv) the energy consumed in the cell during write. The supply voltage for PTM cells was lowered to 0.76 V in order to obtain similar read delay as for the TFET cell, operating at $V_{DD} = 1$ V. The read and write energy estimation for various array sizes was performed by first evaluating the bitline and wordline capacitances per cell for the given voltage swing and analytically deriving the total values.

During standard 6 T cell (either HD or HS CMOS cell) read operation, energy is dissipated by the read bitline discharge occurring for all the cells on the accessed wordline and by the wordline activation. A reasonable statistical assumption is that only half of the read cells store '0', and, as the read is single ended in the 8 T TFET cell, half will discharge the bitline. Therefore, the read energy for 6 T CMOS and 8 T TFET cells can be expressed as in (1) and (2), respectively:

$$E_{READ\_6T\_PTM} = ncol \times E_{READ\_COL} + E_{READ\_WL}, \quad (1)$$

$$E_{READ\_8T\_TFET} = ncol \times \frac{E_{READ_{COL}}}{2} + E_{READ\_WL}, \quad (2)$$

where *n*col is the number of columns in the array, and each energy contribution is evaluated separately for cells (i)–(iii), based on their bitline and wordline capacitance values and the column size.

The evaluation is done with the following assumptions: (i) 32-bit word size, (ii) for write, half of the cells change their content, and (iii) for read, half of the cells on the accessed wordline store '0' and discharge the bitline. By applying these assumptions, the 6 T CMOS and 8 T TFET cells read/write energy can be expressed as in (3) and (4), respectively:

$$E_{WRITE\_6T\_PTM} = 32 \times E_{WRITE_{COL}} + 16 \times E_{WRITE_{CELL}} + E_{WRITE_{WL}} + (m\text{col} - 32) \times E_{READ_{COL}}(@T_{WR}), \quad (3)$$

$$E_{WRITE\_8T\_TFET} = 32 \times E_{WRITE_{COL}} + 16 \times E_{WRITE_{CELL}} + E_{WRITE_{WL}} + (m\text{col} - 32) \times \frac{E_{READ_{COL}}(@T_{WR})}{2}, \quad (4)$$

where $E_{READ_{COL}}(@T_{WR})$ is the energy related to the read bitline discharge of Half-Selected cells on the accessed wordline. The estimation is made by taking into account the reduced wordline pulse width (T_{WR}) during write as compared with read, resulting in less than 100 mV bitline voltage drop. The results obtained for different array configurations are summarised in Table 1.

The highest contribution to the TFET memory energy consumption comes from the wordline capacitance, which is approximately 2× larger when compared with the one of a similar size CMOS counterpart due to its double gate structure. However, TFET E_{READ} is always lower than the CMOS E_{READ} mainly due to the single ended read with bitline discharge only in-case of reading '0'.

E_{WRITE} exhibits dependence on the number of columns, since it requires activating sequentially both wordlines and hence increasing the wordline activation energy contribution to the total active energy. When comparing the 128 × 128 and the 64 × 256 cases one observes a 2x E_{WRITE} increase, which results in the 6 T 0.120 μm^2 cell having the lowest active energy per cycle. However, for wordline lengths not exceeding 128 cells TFET remains the most energy efficient providing a 16.5 and 47.6% lower average energy per cycle when compared with 6 T 0.120 μm^2 cell for 128 × 128 and 256 × 64 cases, respectively. In the 64 × 256 case, TFET SRAM consumes more than the 6 T 0.120 μm^2 cell because of higher E_{WRITE} for TFET SRAM with longer wordlines. However, the assumption of one read per one write activity (which is almost never the case in real applications) hinders the TFET in 64 × 256 configuration due to its high E_{WRITE} value. Even so, the TFET array could be more energy efficient if the number of reads is higher than the number of writes. For example, L1 cache typically serves 4 read requests for 1 write, in which case even for a 64 × 256 array configuration, the TFET cell has the lowest average energy per cycle.

Table 2 summarises and compares the key TFET cell properties as compared with high speed (HS), HD 6 T CMOS cells, and the ultra-low leakage cell in [25]. The speed in active modes is assessed taking into consideration the device parasitics. The 8T-TFET SRAM cell leakage is 4-orders-of-magniture smaller than the one of 6T-CMOS PTM SRAM cells operating at the same speed. The extracted leakage current is approximately 19 pA and 2 fA for the

Table 2 Summary of results based on 128 × 128 array for energy comparison

Cell type	Tech, nm	V_{DD}, V	E_{AVG}	I_{LEAK_CELL}, A	Access T(Rd/Wr)	Cell area, μm^2
8 T TFET (proposed)	32	1	1.26×10^{-13} J	2.00×10^{-15}	260 ps/1.24 n	0.338
6 T (HD) CMOS	28	0.76	1.51×10^{-13} J	1.92×10^{-11}	260 ps/148 ps	0.120
6 T (HS) CMOS	28	0.76	3.19×10^{-13} J	1.043×10^{-11}	260 ps/187 ps	0.197
6 T [25] CMOS	65	1.2	25 μW/MHz*	27×10^{-15}	*7 ns/7 ns*	2.159

Measurement value for full memory

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6T-CMOS PTM (at 0.76 V supply) and 8T-TFET SRAM (at 1 V supply) cells, respectively.

The TFET SRAM cell area is 2.8× and 1.7× larger than the one of the 6 T HD and HS CMOS SRAM cells, respectively, and 6.38× smaller than the one of the ultra-low leakage 6 T CMOS SRAM cell [25]. Contrary to the CMOS SRAMs, which typically use voltage scaling to minimise standby leakage [26, 27], the TFET SRAM cell extremely low leakage value at nominal V_{DD} eliminates the voltage scaling need, which leads to an additional circuitry reduction and the simplification of both the design stage and the memory operation itself. The proposed TFET cell would allow designers to build applications by trading, once again, memory size vs. power: CMOS kilo-bit (Kb) memory can be replaced with mega-byte (MB) TFET memory while consuming less static and dynamic power than CMOS counterparts. For example, 1 Kb of 6T-HD SRAM can be replaced with 1 Mb of proposed 8T-TFET SRAM while still having 19.6% less leakage.

5. Conclusions: In this Letter a TFET-based SRAM cell was proposed. The cell's static power is 4–6 orders-of-magnitude reduced when compared with CMOS standard cells and exhibits very weak dependence on the V_{DD} value. RSNM and WSNM are 120 and 200 mV, thus significantly higher than the other TFET cells proposed in the literature. The proposed 8 T SRAM cell maintains full functionality in all operation modes at 1 V supply voltage with no architectural limitation linked to the half-selection problem. The cell design allows for the use of long wordlines with bit interleaving. The proposed cell avoids problems coming from memory-array-related issues, such as the influence of the write-disturb and half-selected cells on the active power consumption, performance, and stability. The estimated operation speed of an 128 × 128 TFET cells SRAM array is approximately 260 ps (3.84 GHz) for read and 1.24 ns (806 MHz) for write, which despite of being lower than the one of bulk 6 T cell SRAMs are high enough for the targeted applications. Moreover, raising the supply voltage to 1.2 V enabled read and write operation speedups of approximately 2.5× without any substantial leakage increase. Its high energy efficiency during active operation coupled with an extremely low cell leakage validates the proposed cell as an attractive candidate for LSTP circuit design where cell area is of a secondary importance.

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