

Two-dimensional potential, electric field and drain current model of source pocket hetero gate dielectric triple work function tunnel field-effect transistor

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Low ON current and conduction for the negative gate-to-source voltage are the major drawbacks of the steep subthreshold slope tunnel field-effect transistor (TFET). Low work function on the source side of gate contact, high- κ gate dielectric and highly doped layer (delta doping) helps to enhance the ON current of the device. Whereas, low work function of gate electrode on the drain side and low- κ gate dielectric is used to eliminate the problem of conduction for the negative gate-to-source voltage. In the same concern, an analytical model for potential distribution of tri metal hetero gate dielectric delta doped TFET is developed by solving the two-dimensional (2D) Poisson's equation. Moreover, the extraction of electric field is performed by the developed potential model. However, model of drain current for the device is based on the Kane's band-to-band tunnelling generation rate. Finally, the verification of the developed model is performed with the 2D technology computer aided design ATLAS simulation results.

1. Introduction: The downscaling of the bulk metal-oxide semiconductor field-effect transistor (MOSFET) produces better performance, low cost, and compactness of electronics equipment. However, the shrinkage of device dimensions raised some serious issues such as short channel effects, high OFF current and subthreshold slope is limited to 60 mV/decade in the case of bulk MOSFET [1–5]. To eliminate these problems, novel quantum tunnelling phenomena based gated P-I-N diode commonly known as tunnel field-effect transistor (TFET) is studied widely for the replacement of MOSFET. TFET shows better device performance in terms of very low leakage current, subthreshold slope below 60 mV/decade [6–8] and comparatively higher immunity to short channel effects due to tunnelling mechanism of charge carrier for the current flow. Besides this, the conduction for the negative gate-to-source voltage for n-TFET (vice versa for p-TFET) [9] and low current driveability are the drawbacks which prevent the use of device in circuits and system level applications. In this regards, different modifications in the device structure are presented in the recent research. The use of source pocket shows the improvement in the device performance by creating band banding [10]. Further, the concept of hetero gate dielectric is used to improve the device controlling and also reduces the conduction for the negative gate bias [11]. Moreover, the work function engineering helps to enhance the ON-state current by the reducing the depletion width on the source side [12, 13]. Whereas, the use of lower work function on the drain side of gate material increases the depletion width at drain/channel section which results into decrement in the leakage current [14, 15]. Still, none of the researcher considered these three changes (tri metal, hetero gate dielectric and delta doping) at a time to get the integrated advantages. Hence, the triple work function, hetero gate dielectric and delta doped TFET are considered for improving the device performance with development of the analytical model. For this, the new developed potential model is obtained by analytical solution of the two-dimensional (2D) Poisson's equation. Further, the electric field is calculated from the developed potential model to analysis the device electrostatic behaviour and computation of the tunnelling generation rate. Apart from this, the most important parameter drain current based on the band-to-band tunnelling generation rate is obtained by Kane's theory of tunnelling.

Finally, the developed model has been verified against 2D ATLAS device simulator results.

2. Device structure and design parameters: Fig. 1 shows schematic of source pocket hetero gate dielectric triple metal TFET (SP-HGD-TM-TFET). For the analytical model development, the entire channel region is divided into five sections (R1, R2, R3, R4 and R5). Separation of channel is done by considering the effect of gate material work function, gate dielectric, lightly doped channel and heavily doped pocket. Detail about the selection criteria of regions is given in Table 1.

For the same, the design parameters are selected are as follows: Oxide thickness (t_{ox}) = 2 nm, body silicon thickness (t_{si}) = 10 nm, channel length ($L = L_5$) = 50 nm, pocket length ($L - L_4$) = 2 nm, source length (L_S) = 100 nm, drain length (L_D) = 100 nm, drain doping (N_D) = $1 \times 10^{20} \text{ cm}^{-3}$, source doping (N_S) = $1 \times 10^{20} \text{ cm}^{-3}$, channel doping (N_A) = $1 \times 10^{17} \text{ cm}^{-3}$, pocket doping (N_P) = $5 \times 10^{18} \text{ cm}^{-3}$, dielectric constant for the low- κ dielectric (ϵ_1) = 3.9, dielectric constant for the high- κ dielectric (ϵ_2) = 21, work function of the gate section near to source (M1) = 3.9 eV,

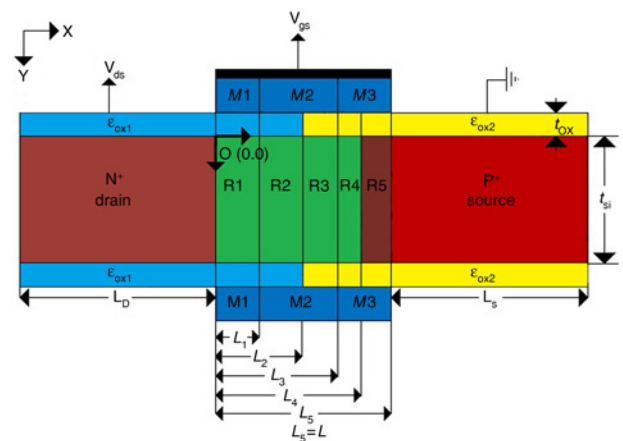


Fig. 1 Device schematic of SP-HGD-TM-TFET

Table 1 Classification of device regions based on gate metal, gate dielectric and channel doping

Region no.	Gate metal	Gate dielectric	Channel concentration
region 1 (R1)	M1	SiO ₂	$1 \times 10^{17} \text{ cm}^{-3}$
region 2 (R2)	M2	SiO ₂	$1 \times 10^{17} \text{ cm}^{-3}$
region 3 (R3)	M2	HfO ₂	$1 \times 10^{17} \text{ cm}^{-3}$
region 4 (R4)	M3	HfO ₂	$1 \times 10^{17} \text{ cm}^{-3}$
region 5 (R5)	M3	HfO ₂	$5 \times 10^{18} \text{ cm}^{-3}$

work function of middle segment of gate ($M2$) = 4.6 eV, and work function of gate segment near to drain side ($M3$) = 3.9 eV.

The following models are used in the simulations: Schokley–Read–Hall model, Auger recombination model, Fermi–Dirac statistical model, field dependent mobility model, concentration dependent mobility model and band-to-band tunnelling Kane’s model are used for the device technology computer aided design (TCAD) simulations.

3. Development of analytical model

3.1. Analytical model for potential distribution: For obtaining potential distribution in channel, the Poisson’s equation is solved in five regions individually considering appropriate boundary conditions. In this concern, regions R1, R2, R3, R4 and R5 have surface potentials as ϕ_1 , ϕ_2 , ϕ_3 , ϕ_4 and ϕ_5 , respectively. Therefore, the Poisson’s equation for different regions can be written as

$$\frac{\partial^2 \phi_i(x, y)}{\partial x^2} + \frac{\partial^2 \phi_i(x, y)}{\partial y^2} = \frac{-qN_A}{\epsilon_{si}}, \quad (i = 1, 2, 3, 4) \quad (1)$$

and

$$\frac{\partial^2 \phi_5(x, y)}{\partial x^2} + \frac{\partial^2 \phi_5(x, y)}{\partial y^2} = \frac{-qN_P}{\epsilon_{si}}, \quad (i = 5) \quad (2)$$

The solution of the above mentioned Poisson’s equation is obtained by considering the assumption that potential distribution in different regions in the channel is parabolic in nature. For this, the considered parabolic potential profile in channel is represented as follows

$$\phi_1(x, y) = a_1(x) + b_1(x)y + c_1(x)y^2 \quad (0 \leq x \leq L_1, 0 \leq y \leq t_{si}) \quad (3)$$

and

$$\phi_{i+1}(x, y) = a_{i+1}(x) + b_{i+1}(x)y + c_{i+1}(x)y^2 \quad (L_i \leq x \leq L_{i+1}, 0 \leq y \leq t_{si}), \quad (i = 1, 2, 3, 4) \quad (4)$$

here $L_5 = L$ is the channel length of device.

Expressions (3) and (4) satisfy the boundary conditions of electric field at front gate oxide and silicon interface as well as back gate oxide and silicon interface for each region can be expressed as

$$\left. \frac{d\phi_i(x, y)}{dy} \right|_{y=0} = \frac{\epsilon_{oxi}(a_i(x) - V_{gsi})}{\epsilon_{si} t_{ox}}, \quad (i = 1, 2, 3, 4, 5) \quad (5)$$

and

$$\left. \frac{d\phi_i(x, y)}{dy} \right|_{y=t_{ox}} = \frac{\epsilon_{oxi}(V_{gsi} - a_i(x))}{\epsilon_{si} t_{ox}}, \quad (i = 1, 2, 3, 4, 5) \quad (6)$$

here $\epsilon_{ox1} = \epsilon_{ox2} = \epsilon_{ox3} = \epsilon_{ox4} = \epsilon_{ox5}$.

The effective gate voltage can be expressed as

$$V_{gsi} = V_{gs} - V_{fbi} \quad (7)$$

where the flat band voltage (V_{fbi}) is the work function difference of the gate and semiconductor can be written as

$$V_{fbi} = \phi_{mi} - \phi_{pi} \quad (8)$$

here ϕ_{mi} is the work function of gate in the i th region and ϕ_{pi} is the work function of channel silicon in the i th region can be written as [10]

$$\phi_{pi} = \chi + \frac{E_g}{2q} + \phi_F \quad (9)$$

In expression (9), ϕ_F can be defined as [10]

$$\phi_F = \frac{KT}{q} \log \left(\frac{N_A}{n_i^2} \right) \quad (10)$$

where χ , E_g , q and ϕ_F represent the electron affinity, bandgap of channel material, charge of carriers and Fermi potential, respectively. Hence, from expressions (3) and (4) and boundary condition defined in expressions (5) and (6), the obtained value of b_i and c_i (for $i = 1, 2, 3, 4, 5$) are

$$b_i(x) = \frac{\epsilon_{oxi}(a_i(x) - V_{gsi})}{\epsilon_{si} t_{ox}} \quad (11)$$

and

$$c_i(x) = \frac{\epsilon_{oxi}(V_{gsi} - a_i(x))}{\epsilon_{si} t_{ox} t_{si}} \quad (12)$$

Further, from expressions (3) to (4) and (11) to (12), we can write channel potential as

$$\phi_i(x, y) = a_i(x) + \frac{\epsilon_{oxi}(a_i(x) - V_{gsi})}{\epsilon_{si} t_{ox}} y - \frac{\epsilon_{oxi}(a_i(x) - V_{gsi})}{\epsilon_{si} t_{ox} t_{si}} y^2, \quad (i = 1, 2, 3, 4, 5) \quad (13)$$

1D representation of the Poisson’s (1) and (2) using expression (13) can be defined as

$$\frac{\partial^2 a_i(x)}{\partial x^2} - \frac{2\epsilon_{oxi} a_1(x)}{\epsilon_a t_{ox} t_{si}} = \frac{-qN_A}{\epsilon_{si}} - \frac{2\epsilon_{oxi} V_{gsi}}{\epsilon_{si} t_{ox} t_{si}}, \quad (i = 1, 2, 3, 4) \quad (14)$$

and

$$\frac{\partial^2 a_5(x)}{\partial x^2} - \frac{2\epsilon_{ox5} a_5(x)}{\epsilon_{si} t_{ox} t_{si}} = \frac{-qN_P}{\epsilon_{si}} - \frac{2\epsilon_{ox5} V_{gs5}}{\epsilon_{si} t_{ox} t_{si}} \quad (15)$$

The solution of expressions (14) and (15) is shown below

$$a_i(x) = A_i e^{\sqrt{\alpha_i} x} + B_i e^{-\sqrt{\alpha_i} x} - \beta_i / \alpha_i, \quad (i = 1, 2, 3, 4, 5) \quad (16)$$

here α_i ($i = 1$ to 5) are defined as

$$\alpha_1 = \alpha_2 = \frac{2\epsilon_{ox1}}{\epsilon_{si} t_{ox} t_{si}} \quad (17)$$

and

$$\alpha_3 = \alpha_4 = \alpha_5 = \frac{2\epsilon_{ox2}}{\epsilon_{si} t_{ox} t_{si}} \quad (18)$$

whereas, the obtained values of β_i ($i = 1$ to 5) are

$$\beta_i = \frac{-qN_A}{\epsilon_{si}} - \frac{V_{gsi}\epsilon_{oxi}}{\epsilon_{si}t_{oxi}}, \quad (i = 1, 2, 3, 4) \quad (19)$$

and

$$\beta_5 = \frac{-qN_P}{\epsilon_{si}} - \frac{V_{gs5}\epsilon_{ox3}}{\epsilon_{si}t_{ox3}} \quad (20)$$

To determine the values of the coefficients A_i and B_i in expression (16), the following boundary conditions are employed:

- (i) Potential at the drain channel interface and channel source interface is equal to sum of drain to source voltage, drain built in potential and source built in potential, respectively

$$\psi_1(0, 0) = V_{bid} + V_d \quad (21)$$

and

$$\psi_5(L, 0) = V_{bis} \quad (22)$$

where V_{bid} and V_{bis} are defined as $V_T \ln(N_D N_C / n_i^2)$ and $V_T \ln(N_S N_P / n_i^2)$, (N_D , N_S , N_C and N_P are doping concentration of drain, source, channel and source pocket), respectively. Here, V_d is drain voltage, whereas, source voltage is considered zero. V_T represents the thermal voltage and numerically it is 26 mV at room temperature.

- (ii) Continuity of potential and electric field at the interface of each region are

$$\psi_i(L_i, 0) = \psi_{i+1}(L_i, 0), \quad (i = 1, 2, 3, 4) \quad (23)$$

and

$$\left. \frac{d\psi_i(x, y)}{dx} \right|_{x=L_i} = \left. \frac{d\psi_{i+1}(x, y)}{dx} \right|_{x=L_i}, \quad (i = 1, 2, 3, 4) \quad (24)$$

From expressions (16) and (21)–(24), the relationship among A_i and B_i (for $i = 1, 2, 3, 4, 5$) can be written as

$$A_1 = V_{bid} + V_{ds} + \frac{\beta_1}{\alpha_1} - B_1 \quad (25)$$

$$B_1 = (A_5 + p_2)o_1 + (B_5 + q_2)r_1 + \left(\frac{\beta_3 - \beta_2}{\frac{\alpha_3}{2\sqrt{\alpha_2}}} \right) e^{\sqrt{\alpha_2}L_2} \quad (26)$$

$$A_2 = A_1 - \left(\frac{\beta_2 - \beta_1}{\frac{\alpha_2}{2}} \right) e^{-\sqrt{\alpha_1}L_1} \quad (27)$$

$$B_2 = B_1 - \left(\frac{\beta_2 - \beta_1}{\frac{\alpha_2}{2}} \right) e^{\sqrt{\alpha_1}L_1} \quad (28)$$

$$A_3 = A_5 + p_2 \quad (29)$$

$$B_3 = B_5 + q_2 \quad (30)$$

$$A_4 = A_5 + \left(\frac{\beta_5 - \beta_4}{\frac{\alpha_5}{2}} \right) e^{-\sqrt{\alpha_5}L_4} \quad (31)$$

and

$$B_4 = B_5 + \left(\frac{\beta_5 - \beta_4}{\frac{\alpha_5}{2}} \right) e^{\sqrt{\alpha_5}L_4} \quad (32)$$

However, the obtained values of constants A_5 and B_5 in terms of the bias voltage and device geometry are

$$A_5 = \frac{V_{bid} + V_{ds} + (\beta_1/\alpha_1) - ((\beta_2/\alpha_2) - (\beta_1/\alpha_1)) - (\beta_1/\alpha_1) \cosh(\sqrt{\alpha_1}L_1) - p_2(p_1 + o_1)}{p_1 + o_1} - \frac{(q_2 + B_5)(q_1 + r_1) - (((\beta_3/\alpha_3) - (\beta_2/\alpha_2))/\sqrt{\alpha_2})) \cosh(\sqrt{\alpha_2}L_2)}{p_1 + o_1} \quad (33)$$

and

$$B_5 = \frac{V_{bid} + V_{ds} + (\beta_1/\alpha_1) + ((\beta_2/\alpha_2) - (\beta_1/\alpha_1)) \cosh(\sqrt{\alpha_1}L_1) - p_2(p_1 + o_1)}{(q_1 - r_1) - (p_1 + o_1)e^{-2\sqrt{\alpha_5}L_5}} - \frac{q_2(q_1 + r_1) - (((\beta_3/\alpha_3) - (\beta_2/\alpha_2))/\sqrt{\alpha_2})) \cosh(\sqrt{\alpha_2}L_2) - \cosh(\sqrt{\alpha_2}L_2) - (p_1 + o_1)(V_{bis} + (\beta_5/\alpha_5))e^{-\sqrt{\alpha_5}L_5}}{(q_1 - r_1) - (p_1 + o_1)e^{-2\sqrt{\alpha_5}L_5}} \quad (34)$$

where

$$p_1 = \frac{e^{\sqrt{\alpha_3}L_2}(\sqrt{\alpha_2} + \sqrt{\alpha_3})}{2\sqrt{\alpha_2}e^{\sqrt{\alpha_2}L_2}}, \quad q_1 = \frac{e^{-\sqrt{\alpha_3}L_2}(\sqrt{\alpha_2} - \sqrt{\alpha_3})}{2\sqrt{\alpha_2}e^{\sqrt{\alpha_2}L_2}} \quad (35)$$

$$o_1 = \frac{e^{\sqrt{\alpha_3}L_2}(\sqrt{\alpha_2} - \sqrt{\alpha_3})}{2\sqrt{\alpha_2}e^{-\sqrt{\alpha_2}L_2}}, \quad r_1 = \frac{e^{-\sqrt{\alpha_3}L_2}(\sqrt{\alpha_2} + \sqrt{\alpha_3})}{2\sqrt{\alpha_2}e^{-\sqrt{\alpha_2}L_2}} \quad (36)$$

and

$$p_2 = \left(\frac{\beta_5 - \beta_4}{\frac{\alpha_5}{2}} \right) e^{-\sqrt{\alpha_5}L_4} + \left(\frac{\beta_4 - \beta_3}{\frac{\alpha_4}{2}} \right) e^{-\sqrt{\alpha_4}L_3} \quad (37)$$

$$q_2 = \left(\frac{\beta_5 - \beta_4}{\frac{\alpha_5}{2}} \right) e^{\sqrt{\alpha_5}L_4} + \left(\frac{\beta_4 - \beta_3}{\frac{\alpha_4}{2}} \right) e^{\sqrt{\alpha_4}L_3} \quad (38)$$

whereas the value of other constants A_i and B_i (for $i = 1, 2, 3, 4$) in terms of the bias voltage and device geometry can be obtained from the developed expression of A_5 and B_5 with the relationship mentioned in expressions (25)–(32).

3.2. Analytical model for electric field: Band-to-band tunnelling generation depends on the electric field, for the same concern, the electric field is extracted by developed potential model.

- (i) Lateral electric field

$$E_{xi}(x) = \left. \frac{\partial \phi_i(x, y)}{\partial x} \right|_{y=0}, \quad (i = 1 \text{ to } 5) \quad (39)$$

and

$$E_{xi} = \sqrt{\alpha_i} e^{\sqrt{\alpha_i} x} - \sqrt{\alpha_i} e^{-\sqrt{\alpha_i} x}, \quad (i = 1 \text{ to } 5) \quad (40)$$

(ii) Vertical electric field

$$E_{yi}(x) = \frac{\partial \phi_i(x, y)}{\partial y}, \quad (i = 1 \text{ to } 5) \quad (41)$$

and

$$E_{yi} = \frac{\epsilon_{ox}(a_i(x) - V_{gsi})}{\epsilon_{si} t_{ox}} - \frac{\epsilon_{ox}(a_i(x) - V_{gsi})}{\epsilon_{si} t_{ox} t_{si}} 2y, \quad (i = 1 \text{ to } 5) \quad (42)$$

The resultant electric field is given as mentioned below

$$|E| = \sqrt{E_x^2 + E_y^2} \quad (43)$$

3.3. Analytical model for drain current: The flow of current in the TFET is due to the band-to-band tunnelling of charge carriers. Hence, the drain current is extracted by employing the Kane's band-to-band tunnelling model [16, 17]. The overall drain current is calculated by the integrating the band-to-band tunnelling generation rate over the tunnelling region. The tunnelling region is defined as a rectangular-shaped region. It varies from 0 to t_{si} in the y -direction, whereas it varies in lateral position from the potential is equal to source potential to its drops by E_g/q to value of the source potential [18–21].

$$I_{ds} = q \int_{l_1}^{l_2} \int_0^{t_{ox}} G_{bttb} dx dy \quad (44)$$

$$G_{bttb} = A E_{avg}^{D-1} E_x e^{[-B1/E_{avg}]} \quad (45)$$

and

$$E_{avg} = \frac{E_g}{q l_{path}}, \quad l_{path} = l_1 - l_2 \quad (46)$$

here

$$l_1 = x(\phi_{source}) \quad (47)$$

and

$$l_2 = x\left(\phi_{source} - \frac{E_g}{q}\right) \quad (48)$$

Since, the tunnelling path exist in region 5, hence, the E_x in the drain current is selected by region 5. Here, $A = 8.1 \times 10^{18} (\text{eV})^{1/2} / \text{cm} \cdot \text{s} \cdot \text{V}^2$, $B = 5.057 \times 10^7 \text{ V/cm} \cdot (\text{eV})^{3/2}$ and $D = 2.5$ for the indirect band-to-band tunnelling.

4. Validation of the model: The verification of the proposed model against TCAD ATLAS Silvaco simulation results is presented in this section. Fig. 2 shows the surface potential for the channel region for the three different gate-to-source voltages and a good agreement of analytical and simulation results can be noticed from the same figure. The increment in the gate-to-source voltage increases the channel potential. Whereas Fig. 3 presents the electric field in the channel for $V_{gs} = 0.8 \text{ V}$, $V_{gs} = 0.9 \text{ V}$ and $V_{gs} = 1.0 \text{ V}$. The electric field on the drain side is reduced due to the effective reduction in potential barrier which widens the

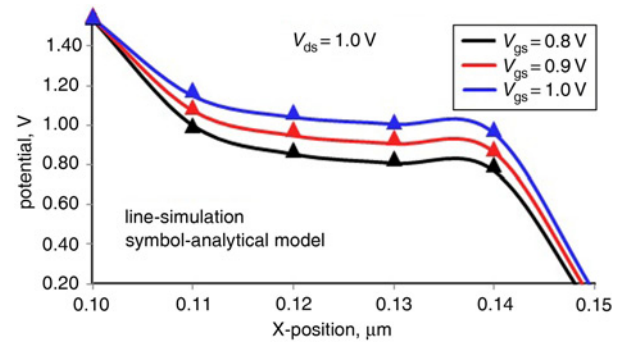


Fig. 2 Variation of the electric potential along the lateral direction in the channel for different gate-to-source voltage below 2 nm from silicon and front gate oxide interface

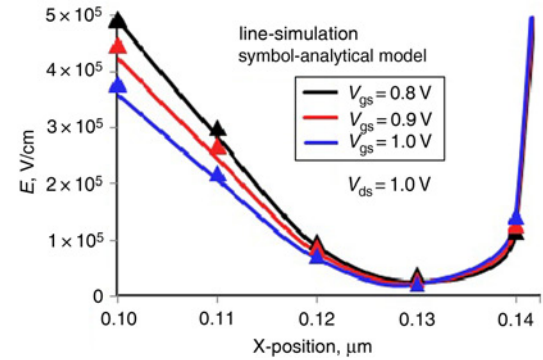


Fig. 3 Variation of the electric field along the lateral direction in the channel for different gate-to-source voltage below 2 nm from silicon and front gate oxide interface

depletion layer on the channel drain interface. Apart from the potential and electric field, the drain current variation with the drain-to-source voltage is presented in Fig. 4. It shows that the high value of gate-to-source voltage provides higher drain current.

Moreover, the impact of the length of the delta doped region on the electric potential is depicted in Fig. 5, which shows increment in the electric potential with increasing delta doping length. An increment in the delta doped length leads to more accumulation of the electrons on the source/channel interface which reduces the depletion layer width on the channel side. Hence, the impact of the increment in the delta doped region is noticed as an increment in the drain current as shown in Fig. 6.

Impact of dielectric variation on the device performance is demonstrated in Fig. 7. For the clear view, it is separated into the two figures. The first figure in Fig. 7 shows the electrical potential difference between low- κ gate dielectric (SiO_2) and hetero gate dielectric (SiO_2 on the drain side and HfO_2 in the source side). An increment in

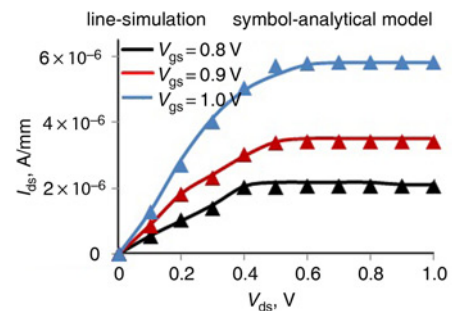


Fig. 4 Drain current variation with drain-to-source voltage for different gate-to-source voltage

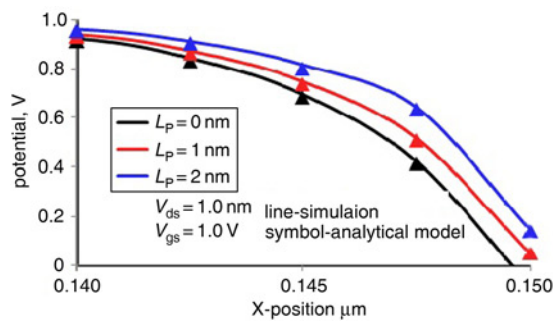


Fig. 5 Variation of the electric potential along the lateral direction in the channel for different delta doping length below 2 nm from silicon and front gate oxide interface

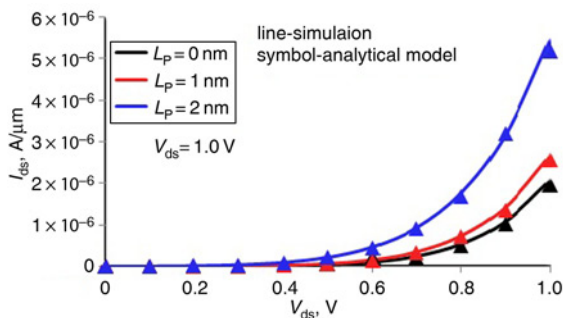


Fig. 6 Drain current variation with the gate-to-source voltage for different delta doping length

the channel potential on the source side is noticed in case of hetero gate dielectric as compared with low- κ , whereas, potential on the drain side remains same for low- κ and hetero gate dielectric on the drain side. Hence, lower depletion width on the source channel interface exists. Further, the comparison between high- κ gate dielectric and hetero gate dielectric is presented in the second part of figure in Fig. 7. Reduction in the potential on the drain side occurs due to low- κ gate dielectric on the drain side, so, the higher barrier exists on the drain side in case of hetero gate dielectric. Whereas,

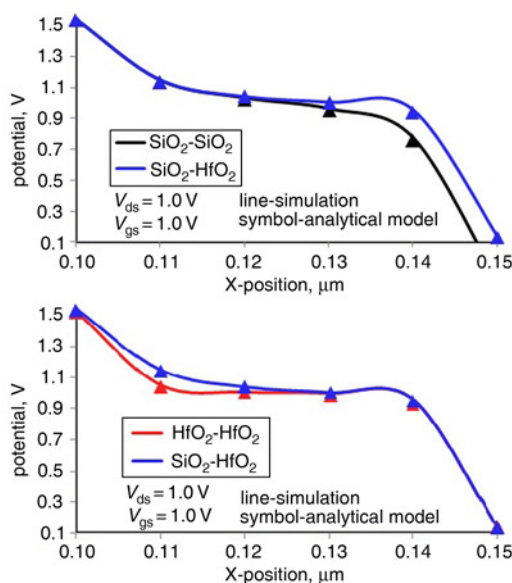


Fig. 7 Variation of the electric potential along the lateral direction in the channel for different combination of the gate dielectric below 2 nm from silicon and front gate oxide interface

the potential on the source side is same for the both due to use of same dielectric on the source side. Hence, it can be concluded from this paragraph that tunnelling barrier on the source side is similar to the hetero gate dielectric and high- κ gate dielectric, whereas the similar barrier exists on the drain side in case of the hetero gate dielectric and low- κ gate dielectric. Hence, use of hetero gate dielectric provides the benefits of the low- κ and high- κ materials such as high ON current as in high- κ gate dielectric and low OFF current as in the low- κ gate dielectric.

5. Conclusion: This Letter deals with the analytical model for the electric potential, electric field and drain current of the TFET with delta doping, gate dielectric and work function engineering. The model authentication is also presented with the 2D simulation results and a good resemblance of analytical model and simulation results is found. It demonstrates the effect of the delta doping length on the electric potential and drain current. It is stated that the drain current improves with the increase of the delta doping length from 0 to 2 nm. Apart from this, the impact of gate dielectric on the surface potential is shown by a comparative study of low- κ , high- κ and hetero gate dielectric. This model is very much helpful for the circuit design and design parameter optimisation to get better device performance.

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