Performance estimation of polarity controlled electrostatically doped tunnel field-effect transistor

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In this work, the performance estimation of polarity controlled electrostatically doped tunnel field-effect transistor (TFET) is reported. The proposed device exhibits heavily doped n-*type* Si-channel with two distinctive gates, namely control gate (CG) and polarity gate (PG). First, the CG and PG work functions of 4.72 eV are considered to convert the layer beneath CG and PG of intrinsic type. Next, the PG voltage of −1.2 V is used at source side to induce a $p+$ region, so that, it follows the similar trend as like a n^+ –i–p^+ gated structure of conventional TFET. Silvaco ATLAS simulation of the proposed device shows I_{ON}/I_{OFF} ratio of $\sim 7.8 \times 10^{10}$ and OFF current is less than 1 fA, with high-k dielectric of gate material at V_{DS} = 0.5, V. Finally, a minimum point subthreshold slope of 12 mV/decade at 300 K is achieved, which indicates that the proposed TFET has the potential to achieve better than ITRS low-standby-power switch performance.

1. Introduction: Apart from short-channel effects (SCEs), drain induced barrier lowering, subthreshold leakage current and subthreshold swing (SS) limit to 60 mV/decade, the fabrication of bulk metal–oxide–semiconductor field-effect transistor (MOSFET) in nanoscale regime is a challenging task due to the formation of larger doping concentration gradient, higher thermal budget, expansive thermal annealing technique and random dopant fluctuations (RDFs) [1]. For this purpose, an alternative device named as junctionless (JL) field-effect transistor (FET) [2] is suggested as a viable option, which does not have any metallurgical junction, simpler in fabrication process and better in performance. However, its SS greater than 60 mV/decade is a grave concern. Therefore, in various possible devices, tunnel FETs (TFETs) have fascinated device and research community due to its potential advantage of SS less than 60 mV/decade at 300 K, extremely low OFF-state current (in the order of 10^{-16} A/μm), robustness against SCEs, and its ability to combat the fundamental 'Boltzmann Tyranny' of conventional FETs [3, 4].

The main limitation with the Si-TFET is low ON-state current because of poor band-to-band tunnelling (BTBT) efficiency. However, the presence of doped source/drain region in conventional TFET also demands a complex thermal budget due to expensive thermal annealing, ion implantation, and RDFs. Moreover, the demand of higher doping concentration in JL TFET (JLTFET), and abrupt doping profile at junctions in these devices further exaggerate the SCEs and RDFs. Therefore, to overcome these drawbacks of Si-TFET and JLTFET, we have investigated the performance of an electrically doped TFET based on polarity bias concept. It overcomes these limitations by reducing the fabrication complexity. However, same metal work function is applied at controlling gate (CG) and polarity gate (PG) terminals, to make the layer underneath CG and PG of intrinsic nature. Further, the PG concept is applied at source side to create a p^+ region, so that, the whole device looks like a n^+–i–p^+ gated structure as similar to conventional TFET. It is important to note that the significant improvement in I_{ON}/I_{OFF} ratio (in the order of 10^{10}), abruptness in point slope (<12 mV/decade) and low OFF-state current (<1 fA) for the proposed device is achieved due to change in the BTBT phenomenon by the combined effect of work function and polarity bias concept. Further, the impact of low bandgap material at the source side is investigated for improving the ON-state current and SS.

2. Device structure and simulation parameters: Fig. 1 shows the cross-sectional view of the proposed polarity controlled electrically doped TFET. The parameters used in our simulation are: Si film thickness (T_{body}) = 10 nm, heavily n-type doped silicon concentration = 1×10^{19} cm^{-3}, effective oxide thickness = 0.8 nm, and control/polarity gate length (L_{CG}/L_{PG}) = 50 nm with a work function of 4.72 eV as similar to [5]. The basic fundamental approach is used to convert n^+–n^+–n^+, (drain, channel and source) into n^+–i–p^+ (TFET). In the proposed structure, first, the work function of PG/CG = 4.72 eV is used to make the layer underneath PG and CG of intrinsic nature. Furthermore, for creating a $p+$ source region, sufficient negative voltage is applied at PG terminal ($V_{PG} = -1.2$ V) to achieve the carrier concentration in the order of 10^{19} cm^{-3}. In addition, S/D contact is made up of nickel silicide (NiSi) with a barrier height of 0.45 eV [6]. In the source side, spacer thickness (L_{gap}, S) is kept 5 nm between CG and PG. The simulations are performed by using 2D Silvaco ATLAS simulator [7]. In this regards, the Shockley–Read–Hall and Auger recombination models are considered due to the presence of high impurity in the channel and minority recombination effects. The non-local BTBT model is used to take into account tunnelling mechanism given in [3, 7]. Bandgap narrowing model is activated due to high doping concentration in the channel. Also, the interface trap on BTBT in TFETs is activated by using quantum confinement model [8]. The mesh is carefully refined in the tunnelling zone to make a trade-off between accuracy and numerical efficiency. The nonlocal model uses the Wentzel–Kramer–Brillouin approximation to calculate the tunnelling probability [3]. The trap-assisted tunnelling is also activated given by Schenk. Since, NiSi contacts are used at the drain and source sides [6], so, we have enabled the universal Schottky tunnelling model.

3. Results and discussion: The carrier concentration and energy band diagram under equilibrium, OFF state, and ON state conditions are shown in Figs. 2*a*–*f*. Fig. 2*a* shows the behaviour of electron and hole concentrations in the thermal equilibrium along X-cut line of the proposed device. From the carrier concentration profile, we analysed that the proposed device exhibits like a n^+–i–p^+ doped device structure which is similar to the conventional TFET. The reason is that the work function of CG/PG (4.72 eV) is greater than 4.5 eV, which results in intrinsic

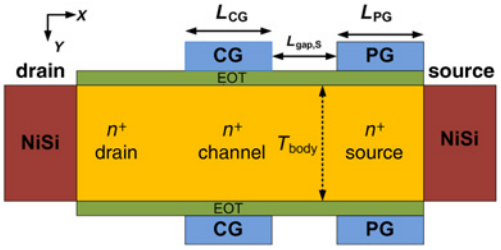

Fig. 1 *Cross-sectional view of the proposed polarity controlled electrically doped TFET*

nature of silicon body beneath CG/PG. Furthermore, when a $V_{PG} = -1.2$ V is used, it converts intrinsic region underneath PG into p^+ region. Hence, the proposed structure shows abruptness as required for TFET. While in Fig. 2*c*, the hole concentration is more than the electron concentration in the channel region, therefore, negligible current flows in OFF state. Its main reason is that at $V_{CG} = 0$ V, there is no accumulation of electron in the channel region. From Fig. 2*e*, the carrier concentration profile along the X-cutline near the surface of a Si film in the ON state is equivalent to the conventional TFET [3, 8], except fall down at the source contact due to NiSi. As the gate voltage increases, there is an accumulation of electrons in the channel region, and electron concentration reaches in the order of $10^{19}/cm^3$.

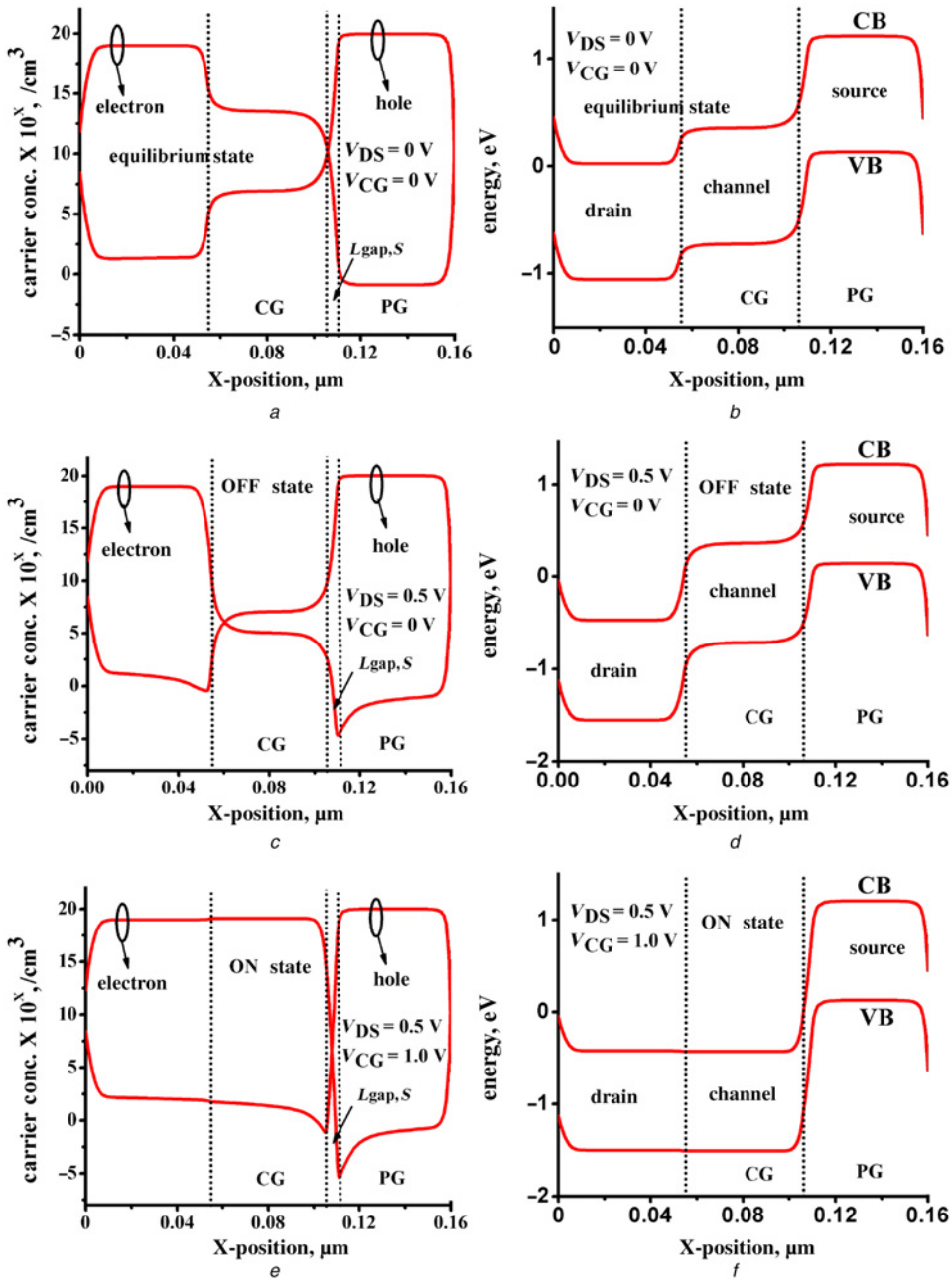

Fig. 2 *Carrier concentration and energy band diagram at various conditions (equilibrium state, OFF state and ON state)*
a Carrier concentration in equilibrium state
b Energy band in equilibrium state
c Carrier concentration in OFF state
d Energy band in OFF state
e Carrier concentration in ON state
f Energy band in ON state

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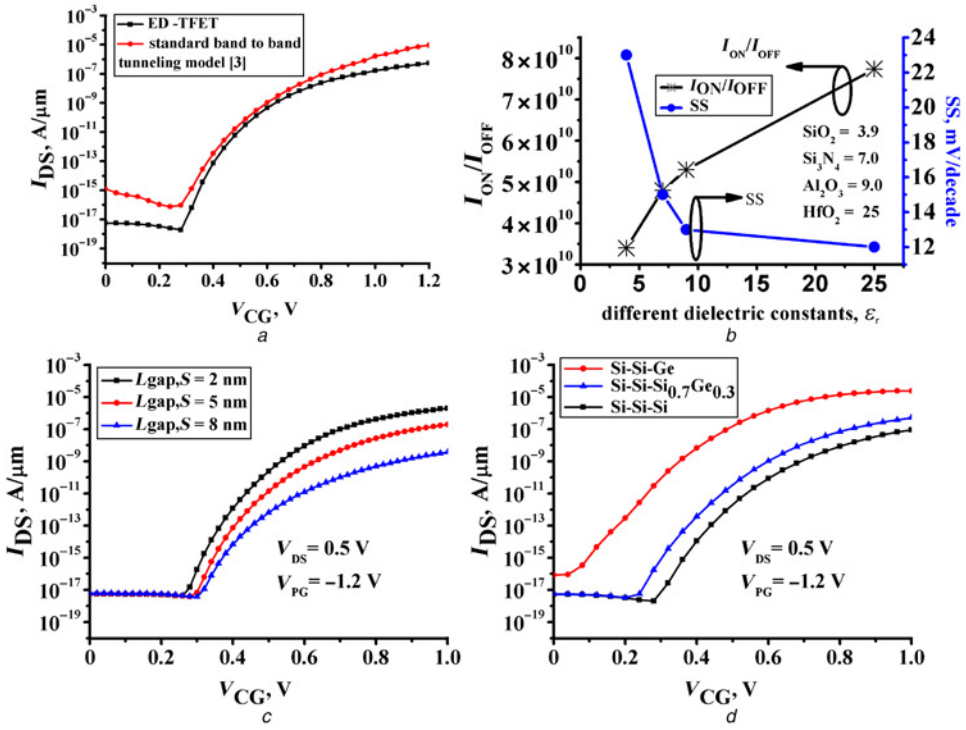

Fig. 3 *Comparative transfer characteristics of proposed and conventional TFET, ION/IOFF ratio and SS along dielectric constant, transfer characteristics of proposed device with L_{gap}, S, and with different combination of hetero materials*
a Transfer characteristics of proposed and conventional TFET
b I_{ON}/I_{OFF} ratio and SS of the proposed device for different dielectric constant values ranging from 3.9 to 25;
c Transfer characteristics with different spacer thickness, and
d With different combination of hetero materials (at source side) for the proposed device

To further analyse the tunnelling phenomenon of the proposed device, energy band diagram in thermal, OFF and ON states is shown in Figs. 2*b*, *d* and *f*. In thermal equilibrium condition, high energy barrier width is maintained at drain-channel and source-channel regions, and similar to conventional TFET [3, 8]. In OFF state, it is well understood that the probability of electron tunnelling from the valence band (VB) of p^+ to the conduction band (CB) of intrinsic region is negligible because of a high energy barrier width between channel and source junctions as depicted in Fig. 2*d*. While in case of ON state, as the CG voltage increases, the electron concentration increases in the channel region and corresponding CB and VB of the intrinsic region gets aligned with the CB and VB of n^+ region; as a result, energy barrier width is reduced at the source/channel interface, which provides higher electron tunnelling probability from the VB of p^+ region into the CB of intrinsic region as shown in Fig. 2*f*. The transfer characteristics of the proposed device and conventional TFET are shown in Fig. 3*a*. It is well understood that the behaviour of proposed and conventional TFET has followed the same trend, as in [3]. It can be clearly seen that the behaviour of ON-state current of the proposed device is one order of magnitude less than that of conventional TFET. Its main reason is due to high ON-state resistance offered by source-side spacer resistance (R_{gap}, S) of the proposed device as compared to the conventional TFET.

In [3], it has been studied that the use of high-k dielectric material for TFET improves the SS and ON-state current. However, it can lead to defects at the dielectric/Si interface, therefore, the direct contact of high-k dielectric material with the Si channel is avoided. Fig. 3*b* shows the effect of different dielectric constants on the I_{ON}/I_{OFF} ratio and SS of the proposed device. It can be seen that the higher dielectric constant gives a higher I_{ON}/I_{OFF} ratio and improved SS. The reason is that it offers a high gate coupling due to high-k dielectric material of high dielectric constant value ranging from 3.9 to 25 for SiO_2 to HfO_2, respectively. To analyse the SS, the point SS is defined as the inverse of maximum slope of the log of the drain current versus gate voltage [3]. The point SS of $\simeq$12 mV/decade and the highest I_{ON}/I_{OFF} ratio of $\simeq 7.8 \times 10^{10}$ is achieved with a high-k dielectric material (HfO_2) for the proposed device. However, for the case of HfO_2, 2.6×10^2 times improvement in I_{ON}/I_{OFF} ratio is achieved for the proposed device as compared to [2]. In addition to this, the 12 mV/decade point SS of the proposed device is near to 11 mV/decade of the conventional TFET [3], and better than point SS of 45 mV/decade as depicted in [9].

The other high-k dielectric materials with smaller dielectric constants (such as Si_3N_4, Al_2O_3) than that of HfO_2, also shows point SS of $\simeq$17 and $\simeq$13 mV/decade, respectively, which is far better than the point SS of Si_3N_4 (86 mV/decade), and Al_2O_3 (80 mV/decade) of [9]. However, for the case of Al_2O_3, $\simeq 1.34 \times 10^2$ times improvement in I_{ON}/I_{OFF} ratio of the proposed device is obtained, as compared to [9]. Fig. 3*c* shows the impact of source-side spacer thickness ($L_{gap,S}$) on the transfer characteristics of the proposed device. As the $L_{gap,S}$ increases, it reduces the abruptness of the source-channel junction gradient; hence, it leads to the increased tunnelling width, and also reduces the tunnelling efficiency due to shift in the source-channel tunnelling path from the gate field [8]. Moreover, as the $L_{gap,S}$ increases, it reduces the ON-state current and results in poor SS due to the increased energy barrier width, which is similar in trend with the previously published results [3, 8]. Therefore, smaller spacer thickness should be preferred to achieve better tunnelling efficiency; as a result, good SS and ON-state current can be achieved (as shown in Fig. 3*c*). To further improve the ON-state current of the proposed device, we have analysed the behaviour of transfer characteristics with different combination of hetero materials at the source side in Fig. 3*d*. As a result, the narrow-bandgap material is preferred at source side to achieve more ON-state current. From Fig. 3*d*, when the narrow-bandgap material (Ge −0.67 eV) is used at the source side (see the Si–Si–Ge combination), it gives maximum ON-state

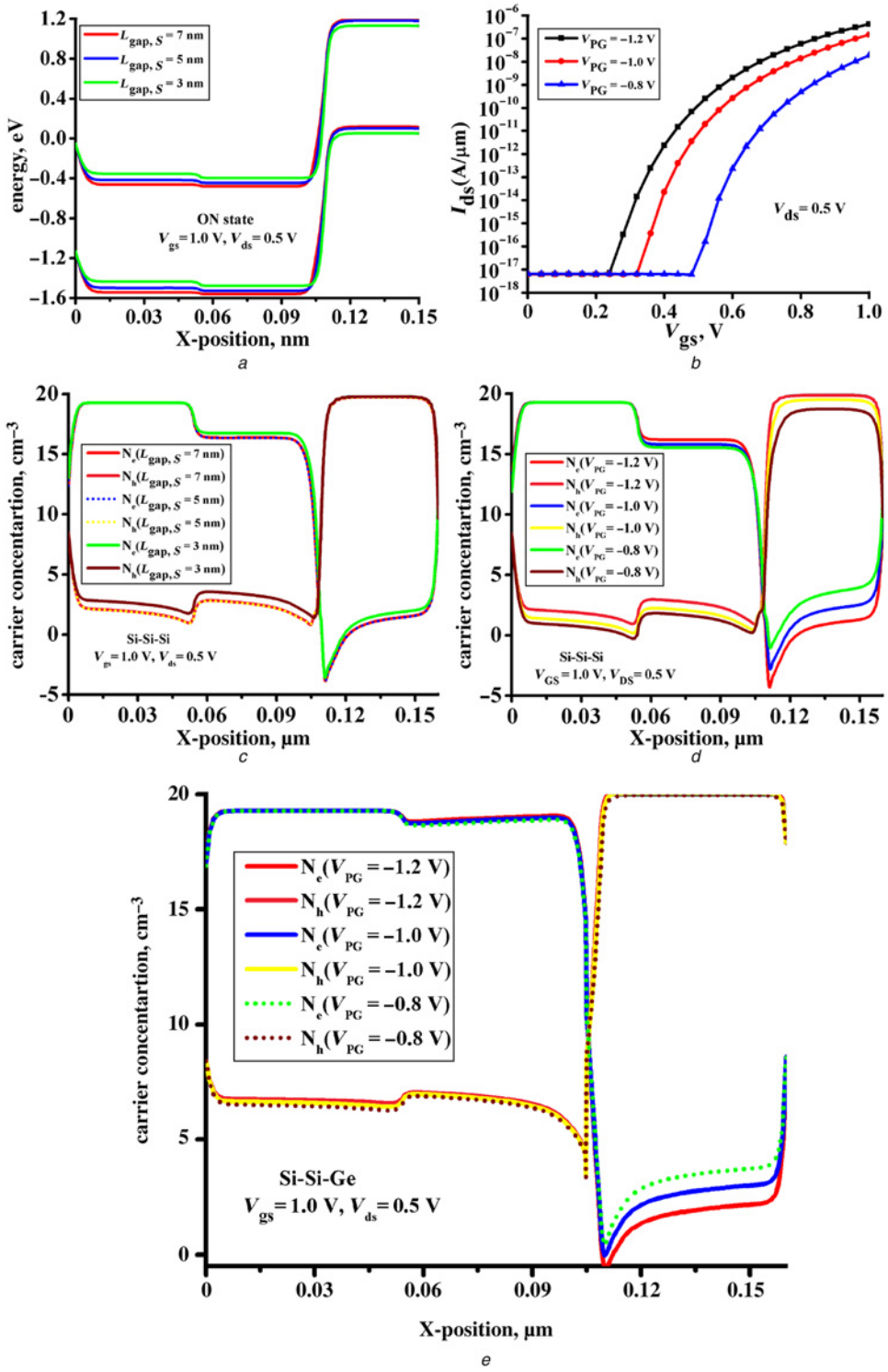

Fig. 4 *Energy band with variation in L_{gap}, S, transfer characteristics with different V_{PG}, carrier concentration of conventional EDTFET with variation in L_{gap}, S, and V_{PG}, and carrier concentration profile of hetero EDTFET with different V_{PG}*
a CB and VB energies of proposed EDTFET with different $L_{gap,S}$
b Transfer characteristics of EDTFET at different polarity bias (V_{PG})
Carrier concentration profile of EDTFET at different
c $L_{gap,S}$ (in case of Si–Si–Si device)
d Polarity bias V_{PG}
e Polarity bias V_{PG} (in case of Si–Si–Ge device)

current (order of 10^{-5} A/μm), as compared to Si–Si–$Si_{0.7}Ge_{0.3}$ (order of 10^{-6} A/μm), and Si–Si–Si (order of 10^{-7} A/μm).

Fig. 4*a* shows the CB and VB energies of proposed EDTFET along the X-position at different spacer length. It can be noticed from this figure that as the spacer length decreases, a more band bending takes place at the source–channel interface; as a result more number of electrons can tunnel from source to channel. However, Fig. 4*b* shows the transfer characteristics of proposed

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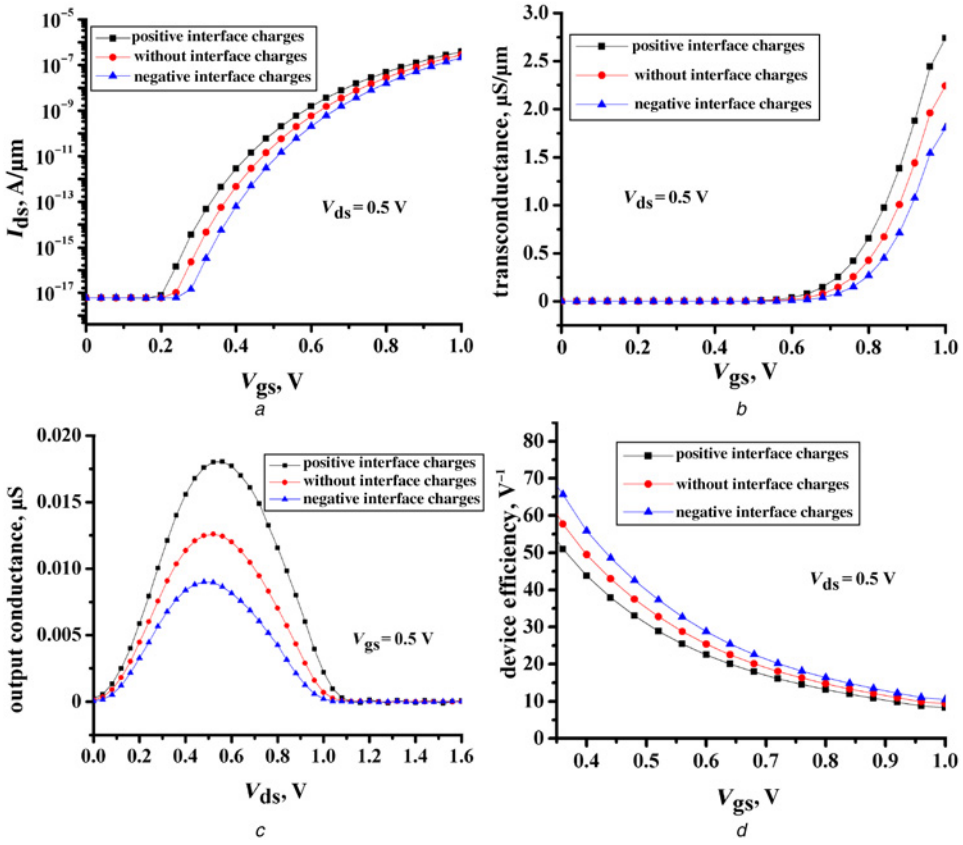

Fig. 5 *Impact of ITCs on*
a Transfer characteristics
b Transconductance
c Output conductance
d Device efficiency of proposed EDTFET as a function of gate bias

EDTFET with different polarity bias (V_{PG}). It can be seen from this figure that as the bias over the source side decreases, drain current reduces significantly. Therefore, in case of Si source device, this bias has significant impact on the electrical characteristics of the device. Fig. 4*c* represents the concentration profile of EDTFET along the X-position with different spacer length. It is apparent from this plot that as the spacer length changes, a variation in concentration profile occurs. Apart from this, Figs. 4*d* and *e* show the carrier concentration of EDTFET of Si–Si–Si and Si–Si–Ge devices at different V_{PG}, respectively. It can be analysed from these figures that as the V_{PG} decreases, the carrier concentration decreases. However, in case of Si–Si–Si device, there is a significant reduction in its concentration profile with different V_{PG}. On the other hand, there is a very small change in its characteristics with different V_{PG} in case of Si–Si–Ge device.

The interface trap charges (ITCs) are also one of the reasons for degradation in the performance of the device. These trap charges generally arise due to stress and process induced damages during fabrication process [10, 11]. To analyse the impact of ITCs on device performance, Fig. 5*a* shows the transfer characteristics of proposed device with different trap charges in logarithmic scale. It can be noticed that the increase (decrease) in ON-state current of proposed device is achieved for the case of positive (negative) trap charges. However, a small variation in case of positive (negative) trap charge is observed with respect to zero (without) interface charges. Figs. 5*b–d* show the transconductance, conductance, and device efficiency of proposed device with different ITCs. It is also apparent from these plots that variation in case of positive (negative) trap charge is observed with respect to zero (without) interface charges. Therefore, small variation in its I_{ds}–V_{gs}, g_m, g_{ds}, and device efficiency ensures improved device performance for analogue/radio frequency applications. However, the improved ON-state current, small leakage current, and steep SS of the proposed device makes it as a suitable choice for dynamic configurability.

4. Conclusion: We discussed the basic operation and estimated the performance of a polarity controlled electrostatically doped TFET. The TCAD simulation shows improved characteristics including improved ON current, and lower SS. The high-*k* dielectric material raises I_{ON}/I_{OFF} ratio ($\simeq 7.8 \times 10^{10}$), and gives a minimum point SS of 12 mV/decade. The behaviour of the proposed device shows, it as a potential candidate to replace or complementary the MOSFET technology, particularly for low standby power applications.

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