Performance investigation of hetero material (InAs/Si)-based charge plasma TFET

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The charge plasma-based tunnel field-effect transistor (TFET) has been seen as the potential candidate to replace the conventional TFET as it offers fabrication simplicity and its proficiency to be used for ultra-low-power applications. A charge plasma TFET (CPTFET) with hetero materials for enhancement of device performance is presented. For this, a narrow bandgap material (InAs) is used instead of silicon in source region for reducing the lateral tunnelling distance at the source/channel interface. The reduced tunnelling width at the source/channel junction enables higher band-to-band tunnelling generation rate, thus the device offers higher ON-state current. In this context, a comparative study of CPTFET and hetero junction charge plasma TFET (H-CPTFET) has been performed in terms of transfer characteristic (I_{ds}–V_{gs}), transconductance (g_m), gate-to-drain capacitance (C_{gd}), cut-off frequency (f_T) and gain-bandwidth product. In addition to this, the effect of variation in channel length (L_g) and drain to source voltage (V_{ds}) on the DC and analogue/radio frequency performance of H-CPTFET is also analysed.

1. Introduction: Continuous down scaling of conventional metal oxide semiconductor field-effect transistor (MOSFET) provides improvement in terms of current driving capability, high speed, compactness of equipment, cost effectiveness and analogue/ radio frequency (RF) figures of merit [1, 2]. Although, it provides such advantages, it also suffers from unacceptable increment in leakage current, short channel effects (SCEs), drain-induced barrier lowering effect and theoretical limitation on the sub-threshold swing of 60 mV/decade [3–6]. As a promising alternative of MOSFET, tunnel field-effect transistor (TFET) is explored widely at simulation as well as experimental level. It offers very low leakage current, sub-threshold slope below $\left(\ln\left((kT/q)\right)\right)$ and has ability to operate at very low supply voltage as it adopts band-to-band tunnelling (BTBT) process for the flow of carriers unlike thermionic emission over the barrier as in the case of traditional MOSFETs [7]. Further, fabrication of TFET is compatible with the existing CMOS process flow [8] and it is very rigid to SCEs due to inter band tunnelling-based working principle. Despite having these benefits, random dopant fluctuations (RDFs) [9, 10] and precise control on the doping concentration are major problems of conventional TFETs which occur due to the inherent process of diffusion due to non-ideal doping profile. Hence, the formation of ultra sharp junction is a challenging task for semiconductor devices and also the physical doping requires a high thermal budget due to expensive thermal annealing technique. To address this problem, arisen due to diffusion process, charge plasma TFET (CPTFET) based on work function engineering is presented in [11–13] where, metal contacts with work function 3.9 and 5.93 eV are located over the lightly doped silicon thin film for the formation of $N+$ drain and $P+$ source region, respectively. Implying this concept provides simpler fabrication process with cost effectiveness in nanoscale devices and immunity towards RDFs [14, 15]. Still, lower ON-state current (I_{ON}) remains the problem in physically doped TFET and severely degraded in the case of CPTFET due to the presence of barrier between gate and metal electrode used for formation of intrinsic and $P+$ region, respectively.

In consideration of aforementioned problems, we propose a hetero junction charge plasma TFET (H-CPTFET) which employs a narrow bandgap material in the source region and comparatively high bandgap material in channel and drain region rather than employing a single material throughout the body. This provides a narrow tunnelling junction at the source/channel interface which results in better band-to-band tunnelling generation rate and hence achieves higher ON-state current. For better analysis of the improvement in device performance, the proposed device is compared with the conventional CPTFET. The electrical properties of semiconductor devices differ from material to material, i.e. semiconductors (Si,Ge) exhibit indirect BTBT [16], while compound materials (InAs, SiGe) show direct BTBT phenomena [17]. In this concern, using low bandgap material in the source region may overcome the issue related to low ON-state current in the case of H-CPTEFT. Regarding this, DC characteristics in terms of transfer characteristics ($I_{ds} - V_{gs}$) and analogue/RF parameters followed by transconductance (g_m), gate to drain capacitance (C_{gd}), cut-off frequency (f_T) and gain-bandwidth product (GBP) are analysed for both conventional (CPTFET) and proposed device (H-CPTFET) in detail. The impact of channel length (L_g) and drain voltage (V_{ds}) variation is also presented for analysing the above-mentioned performance metrics of H-CPTFET device.

This paper is organised as follows: Section 2 consists the description of device structure and simulation parameters. Section 3 is dedicated for comparative performance analysis of conventional CPTFET and H-CPTFET. Along with this, proposed device is tested for different channel length (L_g) and drain voltage (V_{ds}). Finally, summary of the important findings of this investigation is enlightened in Section 4.

2. Device structure and simulation parameters: The cross-sectional view of the conventional CPTFET and hetero material (Si/InAs)-based charge plasma TFET (H-CPTFET) are shown in Figs. 1*a* and *b*, respectively. The physical dimensions of both the devices considered in simulation are listed in Table 1. All the structural dimensions of both the devices are same except that Silicon is used as whole intrinsic body in CPTFET whereas, in the case of H-CPTFET, InAs is employed in the source region while considering silicon (Si) in drain and channel region. The $N+$ type drain and $P+$ type source are created by using work function engineering over the intrinsic body, where the concentration is kept as $n_i = 10^{15}$ cm^{-3}. To induce the plasma of

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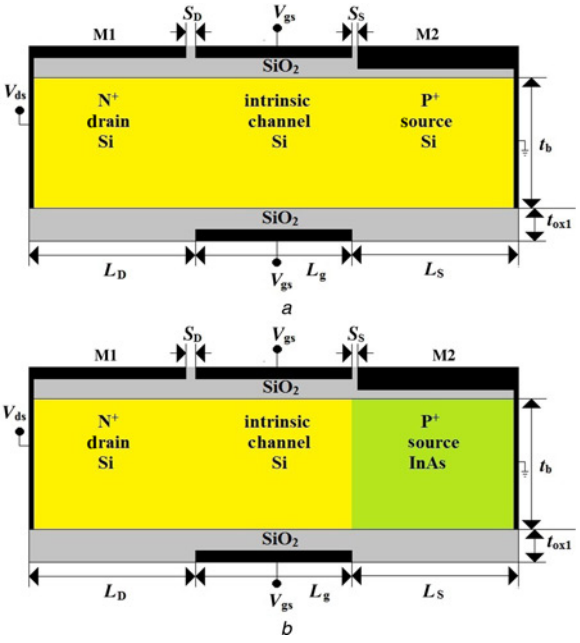

Fig. 1 *Cross-sectional view of*
a Conventional CPTFET
b Hetero material-based CPTFET (H-CPTFET)

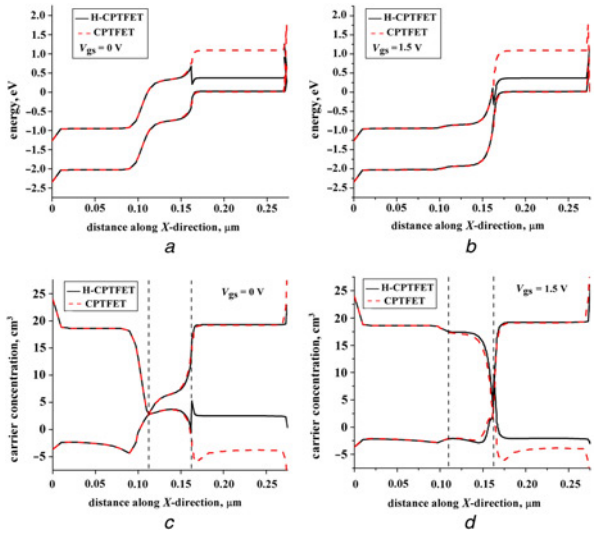

Fig. 2 *Comparision of H-CPTFET and CPTFET*
a Energy-band diagram in OFF state (V_{gs} = 0.0 V, V_{ds} = 1.0 V)
b Energy-band diagram in ON state (V_{gs} = 1.5 V, V_{ds} = 1.0 V)
c Carrier concentration in OFF state (V_{gs} = 0.0 V, V_{ds} = 1.0 V)
d Carrier concentration in ON state (V_{gs} = 1.5 V, V_{ds} = 1.0 V)

hole in the source region, a high work function metal platinum (ϕ_{M2} = 5.93 eV) is considered as source electrode (M2) while a low work function metal hafnium (ϕ_{M1} = 3.9 eV) is considered as drain electrode (M1). To avoid the chance of silicide formation a oxide layer (SiO_2) of 3 nm has been considered between drain electrode and silicon body. Further, to achieve a desired carrier concentration at source region, a thin SiO_2 of 0.5 nm is introduced between source electrode and body [11].

To process the simulation of the device, bandgap narrowing model is been used for the contraction of bandgap. Most dominant model for ON-state analysis of TFET is based on BTBT model. Therefore, non-local BTBT model has been employed to incorporate the features of TFET. Along with these, field-dependent mobility, concentration-dependent mobility, Shockley read hall (SRH) recombination model and Fermi-Dirac statistics are also employed [18]. All the simulations have been carried out using 2D-ATLAS, Silvaco (Version 5.19.20.R) [19].

3. Results and discussion

3.1. DC analysis: This section carries the analysis of energy bands and carrier concentration under OFF state and ON state. The impact of hetero material used in the proposed device can be seen in Figs. 2*a* and *b* where it is clearly observed that the bandgap at the source region is narrowed down due to the presence of lower bandgap material (InAs) in the source region.

Table 1 Physical parameters of the device used in the simulation

Parameters	Values
channel length (L_g)	50 nm
body thickness (t_b)	10 nm
oxide thickness (t_{ox1})	3 nm
gate oxide material	SiO_2
drain electrode work function (ϕ_{M1})	3.9 eV
source electrode work function (ϕ_{M2})	5.93 eV
gate source spacing (S_S)	3 nm
gate drain spacing (S_D)	15 nm

Under OFF-state of the device, the tunnelling barrier width between source and channel is wide enough, hence the charge carriers are unable to tunnel from valence band of source to conduction band of channel region (Fig. 2*a*). Now from Fig. 2*b*, it is notified that, with the application of positive gate bias the barrier height is much reduced at the source/channel junction to let the charge carriers cross the barrier easily, as a result of this, tunnelling probability increases at the same junction which leads to improvement in I_{ds}.

In charge plasma concept, the usage of metal electrodes with different work functions distributes the charge carriers near to the surface depending upon the employed work function. The metal electrode platinum as a source electrode with oxide thickness of 0.5 nm maintains the similar majority carrier concentration in the source region, while minority carriers are distributed differently for both OFF and ON state conditions (Figs. 2*c* and *d*). On the other hand, hafnium as a drain electrode with oxide thickness of 3 nm provides similar carrier concentration (majority and minority) in drain/channel region for both the devices in the same figures. When the positive gate voltage (V_{gs}) is applied, electron can tunnel from valence band of source region to conduction band of channel region, hence it results in increment of carrier concentration in the channel region. Since, the source region is made of low bandgap material, electrons can easily cross the tunnelling width when compared with conventional CPTFET and the same behavior

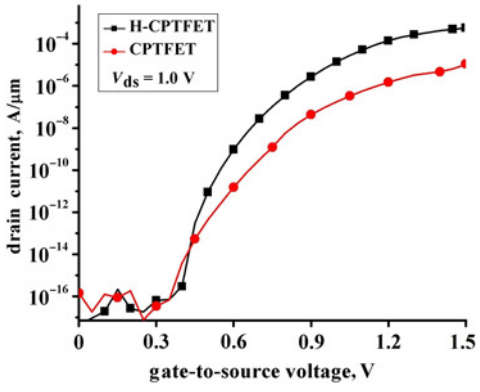

Fig. 3 $I_{ds} - V_{gs}$ *characteristics of H-CPTFET and CPTFET*

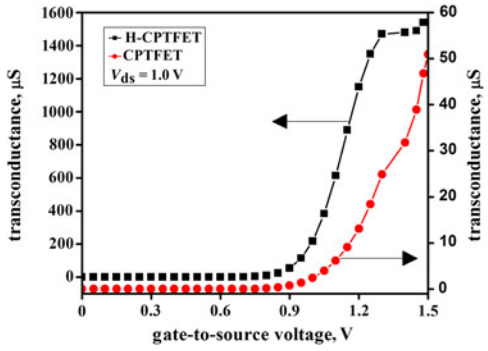

Fig. 4 *Transconductance (g_m) of H-CPTFET and CPTFET*

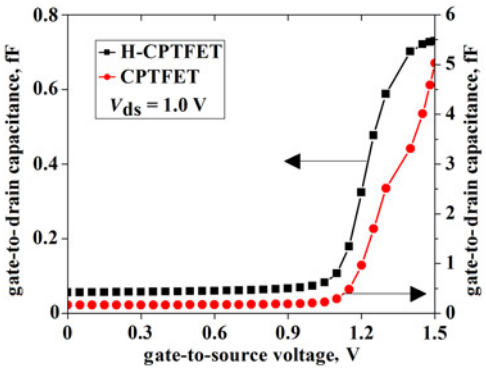

Fig. 5 *Gate-to-drain capacitance (C_{gd}) of H-CPTFET and CPTFET*

can be interpreted by carrier concentration profile of both the devices (Fig. 2*d*).

3.2. Comparative study of DC and analogue/RF parameter: This section presents the comparative study of DC and analogue/RF parameters of H-CPTFET and CPTFET. Fig. 3 shows the behavior of drain current (I_{ds}) with respect to gate voltage (V_{gs}) for both H-CPTFET and CPTFET where it can be observed that H-CPTFET shows a significant improvement in its ON-state drain current (I_{ds}) when compared with CPTFET. The improvement of drain current in H-CPTFET over CPTFET is due to the presence of low bandgap material (InAs) in the source region of H-CPTFET [20]. For gate voltage $V_{gs} = 1.5$ V, ON-state drain current (I_{ds}) is recorded $\sim 5.7 \times 10^{-4}$ A/μm for H-CPTFET and $\sim 1.1 \times 10^{-5}$ A/μm for that of CPTFET. These values have been estimated keeping drain voltage $V_{ds} = 1.0$ V for both the devices.

The spacer width (S_S/S_D) between the gate electrode and source/drain electrodes has to be chosen carefully, as it is the controlling factor for tunnelling of electrons at either of the junctions. The decrement in source spacer width (S_S) increases the tunnelling of charge carriers at the source/channel interface, which enhances ON-state drain current (I_{ds}) [21].

Fig. 4 shows the transconductance (gm) of the two devices conventional CPTFET and proposed H-CPTFET. Transconductance is the electrical characteristic relating the current through the output of a device to the voltage across the input of a device which basically shows the ability of the device to convert gate voltage into drain current [22] and is formulated as (1)

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{1}$$

Drain current for the proposed device H-CPTFET is higher than CPTFET due to the presence of hetero materials in the device, wherein the low bandgap material in the source region significantly reduces the energy barrier at the source/channel junction and enhances the current drivability as shown in Figs. 2*b* and 3, respectively. This increased drain current for H-CPTFET reflects as improved gm for H-CPTFET when compared with CPTFET as depicted in Fig. 4. This signifies that the proposed device has better sensitivity for converting gate voltage into drain current and provides the higher efficiency.

The parasitic capacitances, i.e. gate to source capacitance (C_{gs}), gate to drain capacitance (C_{gd}), and the sum of C_{gd} and C_{gs} which can be defined as gate-to-gate capacitance (C_{gg}) influence the electrical behavior and circuit-level performance of the device. At low frequencies, parasitic capacitance can be ignored, but in high-frequency circuits applications it plays a major role. Parasitic capacitance between the output and the input can act as a feedback path, causing the circuit to oscillate at high frequency and leading to parasitic oscillations which results in signal distortion. Therefore, these unwanted capacitances must be removed or if in case they exist they must be low enough to provide applicability in RF circuits. Among all the parasitic capacitances (C_{gs}, C_{gd} and C_{gg}), C_{gd} (Miller capacitance) is the most dominant one which limits the performance of the device in high-frequency analysis and the expression for C_{gd} can be defined as

$$C_{gd} = \frac{\partial Q_g}{\partial V_d} \tag{2}$$

where Q_g is gate charge and V_d is drain voltage.

Fig. 5 illustrates the gate to drain capacitance of conventional and proposed device where it can be seen that H-CPTFET (proposed device) exhibits much lesser capacitance than that of CPTFET (conventional) due to reduction in density of state (DOS) which weakens the capacitive coupling at the gate drain interface [23] which supports its applicability in high-frequency applications. Further to this, it is observed that the gate to drain capacitance increases for higher value of gate to source voltage due to reduction of barrier between channel and drain by the formation of inversion layer.

Cut-off frequency (f_T) and GBP are the important parameters for the analysis of high-frequency responses. f_T can be defined as frequency at which short circuit current gain falls to unity and useful for measurement of device speed (transit delay ($\tau = 1/f_T$)). The mathematical expression for cut-off frequency (f_T) and GBP can be represented by

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \simeq \frac{g_m}{2\pi(C_{gg})} \tag{3}$$

$$\text{GBP} = \frac{g_m}{20\pi C_{gd}} \tag{4}$$

where C_{gd} is the gate to drain capacitance, C_{gs} is the gate to source capacitance and the sum of C_{gd} and C_{gs} is collectively called gate-to-gate capacitance (C_{gg}).

The variation of cut-off frequency (f_T) with respect to gate voltage (V_{gs}) for both the devices can be observed in Fig. 6. The increment of f_T at lower gate voltages is due to enhancement in g_m with respect to V_{gs}. However, f_T decreases beyond a certain voltage after attaining peak due to combined effect of increased C_{gg} and the reduction in transconductance (g_m) which is caused by the decrement in mobility [24]. The parameter f_T of H-CPTFET is higher than that of CPTFET due to employment of low bandgap material at source region which leads to enhancement in drain current, this in turn provides higher g_m. Thus, with the collective improvement in g_m and reduction in C_{gd}, increment in f_T is observed as shown in Fig. 6.

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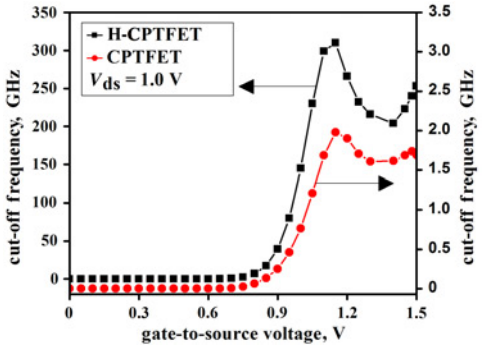

Fig. 6 *Cut-off frequency (f_T) of H-CPTFET and CPTFET*

Fig. 7 shows the variation of GBP for H-CPTFET and CPTFET with respect to gate voltage (V_{gs}). As the gate voltage increases, the initial increment in GBP is observed due to significant growth in transconductance (g_m), whereas it decreases for larger values of gate voltage due to increment in parasitic capacitance and thus H-CPTFET shows higher GBP when compared with CPTFET, which indicates better performance of H-CPTFET in high-frequency applications.

3.3. Effect of channel length variation on H-CPTFET: This section presents the effect of channel length (L_g) variation in the device performance characteristics. In this concern, channel lengths (L_g) of 40, 50, 60, 70 and 90 nm are considered for simulation. Fig. 8 depicts the variation of drain current (I_{ds}) of H-CPTFET with respect gate voltage (V_{gs}) at different channel lengths (L_g) and observed that the I_{ds} shows small changes with the variation in L_g. This is because the drain current (I_{ds}) is more sensitive towards barrier resistance at source/channel junction, rather than the variation in channel resistance, which shows its susceptibility towards the variation in barrier resistance instead of channel resistance of the effective bandgap at the source/channel interface [25]. By this optimisation performed, it is obtained that, no such noticeable effect takes places on drain current with decrement in L_g below 50 nm, though there is a small reduction in drain current for $L_g > 50$ nm which can be seen in Fig. 8.

Charge carriers increases at the source side by increasing gate-to-source voltage (V_{gs}) through band-to-band tunnelling mechanism. Due to increased rate of tunnelling of charge carriers with decrement in L_g at the source/channel junction provides increment in g_m which can be seen in Fig. 9. The increase in drain current for lower L_g also assists in improvement of g_m as depicted in Fig. 9 where it is observed that, as the L_g increases the g_m decreases. Large g_m is obtained for lower L_g, whereas no significant improvement is noticed for $L_g < 50$ nm as there is no change in drain current for $L_g < 50$ nm.

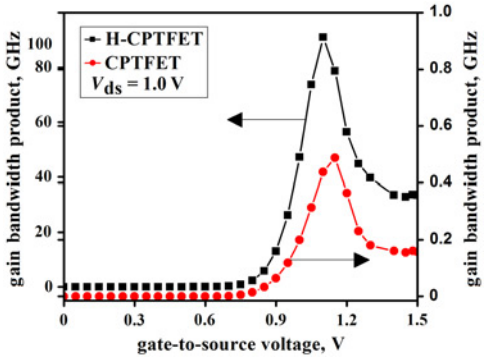

Fig. 7 *GBP of H-CPTFET and CPTFET*

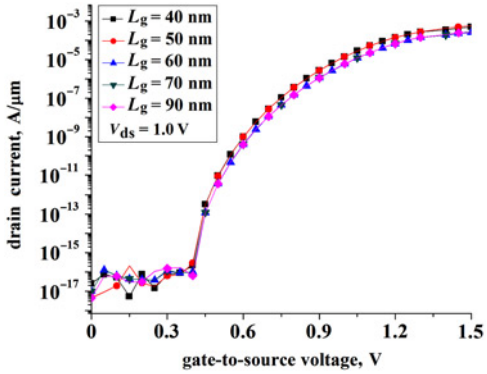

Fig. 8 *$I_{ds} - V_{gs}$ for channel length (L_g) variation of H-CPTFET*

Fig. 10 depicts the variation of C_{gd} of H-CPTFET as a function of V_{gs} at different channel lengths (L_g). It is observed that the value of C_{gd} for all channel lengths (L_g) follow the same trend up to $V_{gs} = 1.2$ V and after 1.2 V, there is decrement in C_{gd} with down scaling of the device and the lowest C_{gd} is obtained for $L_g = 40$ nm. The reason behind the reduction in C_{gd} with down scaling of the L_g is shortening of inversion layer formed within channel region [26].

The behavior of cut-off frequency (f_T) as a function of gate voltage (V_{gs}) for different channel lengths (L_g) is shown in Fig. 11. The f_T of the device depends upon the combined variation of g_m and C_{gd}. As we observed in prior Figs. 9 and 10, that with the down scaling of the channel length (L_g), there is an enhancement in transconductance (g_m) and degradation in the gate to drain capacitance (C_{gd}), which provides high cut-off frequency (f_T) as shown in Fig. 11. However, superior performance of the device is measured at $L_g = 40$ nm and higher f_T is observed due to relatively large g_m and small C_{gd} when compared with other lengths (50, 60, 70 and 90 nm). Further, it is also observed that f_T for $L_g \leq 50$ nm shows early growth as compare to other channel lengths due to early improvement in g_m (Fig. 9).

The evaluation of GBP for different channel length (L_g) with respect to gate voltage (V_{gs}) is shown in Fig. 12. Down scaling of the channel length (L_g) results into enhanced transconductance (g_m) and reduced gate to drain capacitance (C_{gd}). Therefore, the dependency of GBP on both these parameters as per the relation (GBP $\propto g_m/C_{gd}$), it can be observed that if channel length (L_g) reduces, there is an improvement in GBP and the higher GBP is achieved at channel length (L_g) 40 nm. From this analysis of L_g optimisation, it is found that device performance enhances for smaller L_g and the best results are obtained for $L_g \leq 50$ nm, whereas performance degrades for $L_g > 50$ nm. Along with that, further

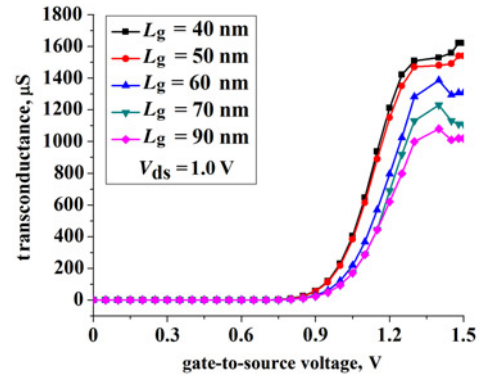

Fig. 9 *Transconductance (g_m) for different channel length (L_g) of H-CPTFET*

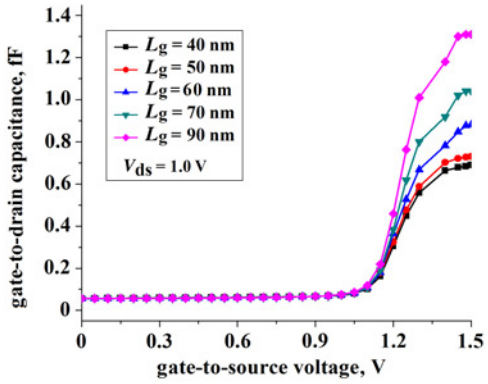

Fig. 10 *Gate-to-drain capacitance (C_{gd}) for different channel length (L_g) of H-CPTFET*

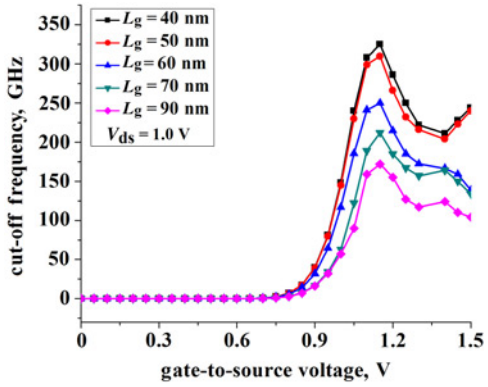

Fig. 11 *Cut-off frequency (f_T) for different channel length (L_g) of H-CPTFET*

reduction in channel length will lead to fabrication complexity in nanoscale devices Therefore, keeping this into consideration, $L_g = 50$ nm is chosen as the optimised value in further calculations which will provide better drain current as well as practical feasibility for the device.

3.4. Effect of drain voltage variation for H-CPTFET: In this section, performance of the proposed device is investigated for various values of drain voltage (V_{ds}) ranging from 0.4 to 1 V. The variation of transfer characteristics of the device for the aforementioned drain voltages (V_{ds}) can be studied by Fig. 13. The increment in drain voltage (V_{ds}) shows little deviation in drain current. The I_{ds} for $V_{ds} = 1$ V is higher compared with other lower V_{ds}.

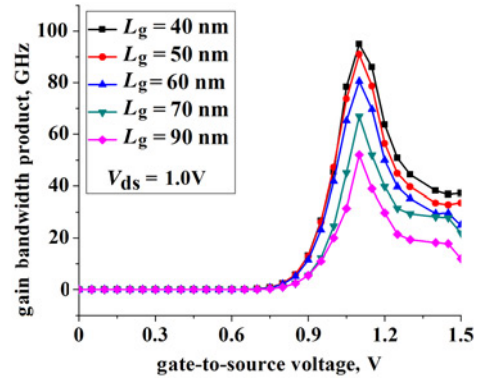

Fig. 12 *GBP for different channel length (L_g) of H-CPTFET*

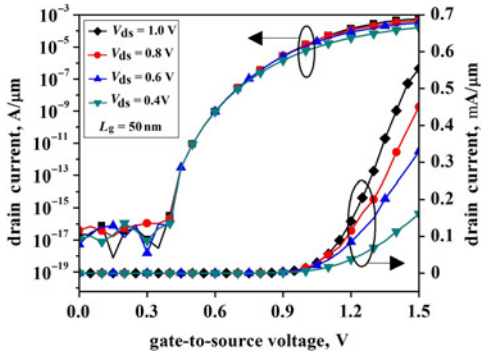

Fig. 13 *I_d–V_{gs} characteristic for drain voltage (V_{ds}) variation of (log scale: left, linear scale: right) H-CPTFET*

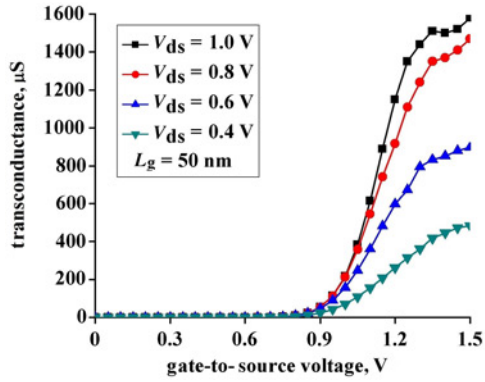

Fig. 14 *Transconductance (g_m) for different drain voltage (V_{ds}) of H-CPTFET*

For lower value of V_{gs}, there is no significant change occurs in drain current with V_{ds}. However, for higher value of V_{gs}, I_{ds} increases with V_{gs}. For this, the impact of increased I_{ds} is reflected as increased in g_m of the device as shown in Fig. 14 for different values of v_{ds} and v_{gs}. Further in Fig. 15, it is shown that gate-to-drain capacitance (C_{gd}) decreases with increasing drain voltage (V_{ds}) of H-CPTFET due to weakening of inversion layer from drain to source region.

Cut-off frequency (f_T) and GBP are strongly affected with the variation in drain voltage (V_{ds}) which can be seen from Figs. 16 and 17, respectively. f_T increases for greater V_{ds} due to reduction in C_{gd}. Cut-off frequency attains peak at $V_{gs} = 1.2$ V and falls after a certain voltage (Fig. 16) due to the combine effect of

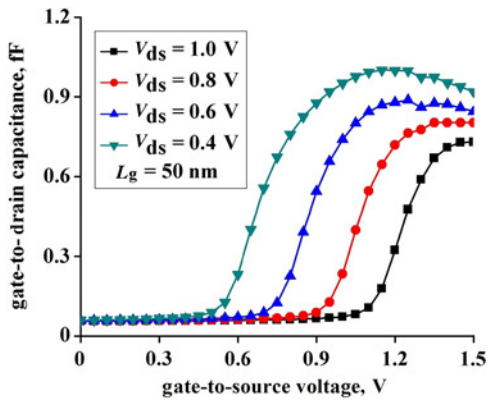

Fig. 15 *Gate-to-drain capacitance (C_{gd}) for different drain voltage (V_{ds}) of H-CPTFET*

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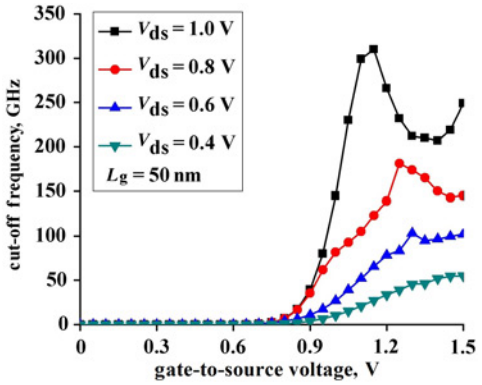

Fig. 16 *Cut-off frequency (f_T) for different drain voltage (V_{ds}) of H-CPTFET*

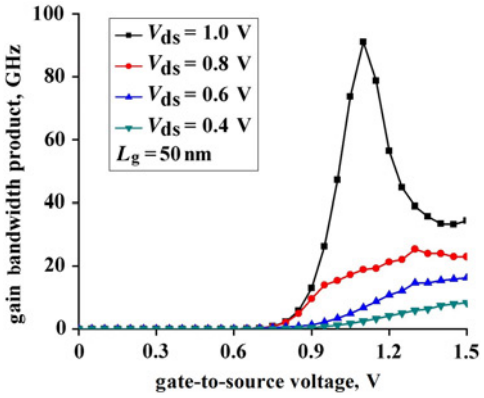

Fig. 17 *GBP for different drain voltage (V_{ds}) of H-CPTFET*

falling g_m and rising C_{gd} at higher V_{gs}, which ensures the usability of device for low power RF circuit applications.

Now looking into Fig. 17, we observe that GBP increases with increase in drain voltage (V_{ds}) due to reduced capacitance at higher V_{ds}. Here, GBP achieves maximum value at $V_{gs} = 1.2$ V and degrades for higher V_{gs}. Thus, it is apparent that f_T and GBP reaches to peak value at lower V_{gs} which enables its utility in low power RF applications.

4. Conclusion: In this paper, a comparative study of the conventional CPTFET and Hetero charge plasma TFET (H-CPTFET) is explored by using 2D-ATLAS Silvaco (Version 5.19.20.R) simulations. It is shown that the usage of hetero material in the device enables the lowering of bandgap at the source/channel interface which increases the tunnelling rate of charge carriers and hence improves the drain current (I_{ds}) and transconductance (g_m), resulting in better current driving capability of the device. The proposed device (H-CPTFET) resolves the fabrication issues of doping profile complexity, thermal budget and is also cost effective. Furthermore, the analogue/RF parameters are investigated with various channel length (L_g) and drain voltage (V_{ds}) of channel length (L_g) and drain voltage (V_{ds}) is performed where it is shown that $L_g = 50$ nm and $V_{ds} = 1$ V provides better performance for DC as well as analogue/RF figure of merits. Cut-off frequency (f_T) and GBP attains peak at lower V_{gs} which signifies the usability of the device for low power analogue and CMOS applications. Hence, the work presented in this paper shows the potentiality of the device to provide better DC and analogue/RF performances.

5 References

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