Effect of high-*k* dielectric on the performance of Si, InAs and CNT FET

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The important issue of selection of gate dielectrics to reduce short channel effects (SCEs) is presented along with the study of different channel materials in transistors. A comparative study of performance was carried out of silicon dioxide (SiO_2), aluminium oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3) and titanium dioxide (TiO_2) as gate dielectrics for Si double gate field-effect transistor (FET), Si gate all around (GAA) nanowire FET (NWFET), indium arsenide GAA NWFET and carbon nanotube (CNT) FETs within non-equilibrium Green's function formalism. Simulated results show that TiO_2 is better gate dielectric as compared with SiO_2, Al_2O_3, HfO_2 and La_2O_3, with near ideal subthreshold swing (60 mV/decade), lower I_{off}, improved drain-induced barrier lowering and high transconductance (g_m). Also, the gate capacitance (C_g), cut-off frequency (f_T) and switching time (τ) improve with the high-*k* dielectric materials. Furthermore, the study of different channel material shows that CNT has better SCEs, smaller C_g with τ ranging from 13.5 to 12.5 fs suitable for digital applications and f_T of about 7–9 THz.

1. Introduction: Reducing size of transistors with reliability in functionality is the essence of rapid progress in complementary metal–oxide–semiconductor (MOS) technology. The silicon (Si) technology has been in the long run from the existence of electronic devices, but the momentum of its advancement has been slowed down by issues related to scaling. Today, the devices are available in nanometre regime, but with the shrinking size of Si-based field-effect transistors (FETs), the reliability and performance of these Si-based MOSFET is a matter of concern. In addition to their limitation in fabrication and scaling for threshold voltage, gate oxide thickness, leakage current etc., the appearance of short channel effects (SCEs) such as drain-induced barrier lowering (DIBL), subthreshold swing (SS) and gate leakage current in transistors further complicates the process of scaling [1]. Various solutions have been proposed to overcome these limitations. Use of new channel materials such as the III–V compound semiconductors could be a better option than Si. Carbon nanotube (CNT) is another fascinating material which can further extend the scaling because of its higher mobility and improved gate capacitance [2, 3]. Different FET structures such as multigate nanowire (NW) structures are also being explored to have a better gate control for improved subthreshold characteristics [4]. Apart from channel material, different gate dielectrics were also explored. Conventionally, Si dioxide (SiO_2) has been the gate dielectric material in FETs, but with the scaling down of gate dielectric thickness, SiO_2 has no longer remained the preferred choice because of the tunnelling leakage current, oxide breakdown and reliability issue associated with it. To overcome the drawbacks associated with thinner SiO_2, the alternative oxides with high permittivity were proposed. In fact, alternative dielectric with high-*k* happens to be one of the most intensively researched topics since last decade in electronics because of its ability to substantially reduce the limitations in scaling. A good number of promising results have been obtained by several research groups dealing with high-*k* dielectric materials such as hafnium silicate, lanthanum oxide (La_2O_3), titanium dioxide (TiO_2), yttrium oxide, aluminium oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide [5–11]. It has been experimentally found that TiO_2 is ahead in the race for replacement of SiO_2 as the gate dielectric. Moreover, the chemical stability and non-toxicity of TiO_2 makes it suitable for electronic industry [12].

The primary objective of this Letter is to study the relative performance of ultra-thin Si double gate FET (DGFET), Si NWFET, indium arsenide (InAs) NWFET and CNT FET with different gate dielectrics in terms of improvement in SCEs. The non-equilibrium Green's Function (NEGF) formalism along with the self-consistent solution of two-dimensional (2D) Poisson–Schrödinger equations has been employed to carry out the simulation [13]. In addition to the SCEs, the relative study of AC performance parameters such as gate delay, cut-off frequency and gate capacitance have been carried out for better understanding of channel material.

Section 2 describes the structure of the device. Section 3 deals with the simulation approach and the analytical expressions. Section 4 presents the results obtained and the discussion. Section 5 is the conclusion section providing a brief summary of the outcomes of the simulation.

2. Device structure: The longitudinal section of the FET is shown in Fig. 1*a*. The ultra-thin DGFET is shown in Fig. 1*b*. The channel is sandwiched between two insulators with two gates allowing a better gate control over the potential barrier to have reduced SCE's. The length (L_g) and thickness (T_{ch}) of the channel are 10 and 5 nm, respectively, and the length of drain and source are 10 nm each. We have considered the device to operate in the ballistic regime. An intrinsic channel of Si is present in between two highly doped source/drain regions with n-type doping density of 10^{20} cm^{-3}. The DG structure provides better electrostatics as compared with the bulk MOSFET [14].

The cross-sectional view of the gate all around (GAA) NWFET is illustrated in Fig. 1*c* where the channel is surrounded by dielectric with gate on multiple sides. It provides better gate control over the channel as compared with the DGFET in suppressing gate leakage current [15]. Two NWFETs with Si and InAs as channel materials are considered in simulation. The doping density of source and drain regions are kept same as that in DGFET.

The CNT FET is shown in Fig. 1*d* with single-walled CNT of chirality (13, 0) having a bandgap of 0.75 eV, as the channel material and dielectric surrounded on all sides. The source and drain regions are doped with donor molar fraction of $f = 2 \times 10^{-3}$. The length of source, drain and channel are same in all the FETs. Also a constant dielectric thickness of 1 nm is considered in all the FETs.

3. Theoretical formulation: The quantum transport simulations of our devices are carried out using NEGF formalism with self-consistent solution of Poisson–Schrödinger equation and

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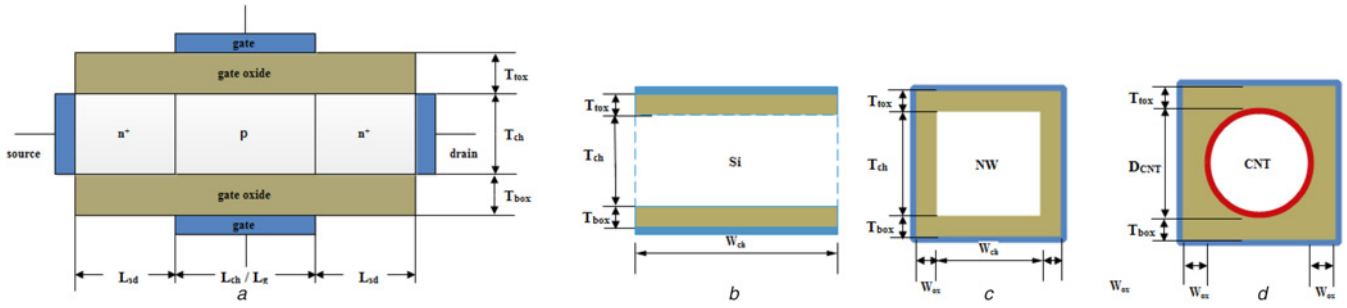

Fig. 1 *Longitudinal section of*
a all the FETs
Transverse section of
b Si DGFET
c NWFET
d CNT FET

open boundary conditions. For Si and InAs FETs, we have used effective mass Hamiltonian in mode space approach, whereas for CNT FET a nearest neighbour tight-binding Hamiltonian for π-orbital electrons have been used in real space approach [16–19].

The most important parameter of NEGF formalism is GF which is given as [16]

$$\boldsymbol{G}(E) = [E\boldsymbol{I} - \boldsymbol{H} - \boldsymbol{\Sigma}_{\mathrm{S}} - \boldsymbol{\Sigma}_{\mathrm{D}}]^{-1} \tag{1}$$

where $\boldsymbol{H}$ represents the Hamiltonian of the respective devices. $\boldsymbol{\Sigma}_{\mathrm{S}}$ and $\boldsymbol{\Sigma}_{\mathrm{D}}$ are the source and drain self-energy matrices, respectively.

After obtaining the GF, the electron concentration in CNT FET is given as

$$n(\boldsymbol{r}) = 2\int_{E_i}^{+\infty} \mathrm{d}E\Big[\big|\psi_{\mathrm{S}}(E,\ \boldsymbol{r})\big|^2 f(E - E_{F_{\mathrm{S}}}) + \big|\psi_{\mathrm{D}}(E,\ \boldsymbol{r})\big|^2 f(E - E_{F_{\mathrm{D}}})\Big] \tag{2}$$

and the hole concentration is given as
(see (3))
where $\boldsymbol{r}$ specifies the coordinates of atomic site of each carbon atom in space, $E_{F_{\mathrm{S}}}(E_{F_{\mathrm{D}}})$ and f are the source and drain Fermi level and the Fermi–Dirac occupation factor, respectively. The term $|\Psi_{\mathrm{S}}|^2(|\Psi_{\mathrm{D}}|^2)$ represents the probability that the states injected by the source (drain) reach the carbon site $\boldsymbol{r}$.

In case of Si and InAs FETs, since we are using effective mass approximation, the 3D electron density is given by [17]

$$n^{3\mathrm{D}}(x,\ y,\ z) = \sum_{v,i}\left[\left(\int_{E_i} n_i(E_l)\mathrm{d}E_l\right)|\psi_{iv}|^2\right] \tag{4}$$

where $\int_{E_i} n_i(E_l)\mathrm{d}E_l$ is the 1D (2D) electron density of each subband i in NWFETs (DGFETs) and the summation is over every conduction band valley v and subband i.

The 3D electron density obtained from the above equations is fed to Poisson equation to obtain the electrostatic potential $\Phi(x, z)$ self-consistently. The self-consistent solution of Poisson–Schrödinger is obtained numerically by using Newton–Raphson iteration method [17–19]. Once the self-consistent solution is achieved, the drain current for CNTFET is obtained by using the formula
(see (5))
where Tr is the trace operator. Similarly, the drain current for Si and InAs FETs is obtained as

$$I_{\mathrm{D}} = \frac{2q}{h}\sum_i \int_{-\infty}^{+\infty} \mathrm{d}E\left\{\begin{array}{l}\mathrm{Tr}\Big[(\boldsymbol{\Sigma}_{\mathrm{S},i} - \boldsymbol{\Sigma}_{\mathrm{S},i}^{\dagger})\boldsymbol{G}_i(\boldsymbol{\Sigma}_{\mathrm{D},i} - \boldsymbol{\Sigma}_{\mathrm{D},i}^{\dagger})\boldsymbol{G}_i^{\dagger}\Big] \\ \times\Big[f(E - E_{F_{\mathrm{S}}}) - f(E - E_{F_{\mathrm{D}}})\Big]\end{array}\right\} \tag{6}$$

where i represents the subbands. $\boldsymbol{G}_i$, $\boldsymbol{\Sigma}_{\mathrm{D},i}$ and $\boldsymbol{\Sigma}_{\mathrm{S},i}$ are GF, drain and source self-energy matrices, respectively, for subband 'i'.

One of the most necessary parameter for numerical simulation is the band alignment between the semiconductor and the gate dielectric, i.e. conduction band offset (CBO). The CBO values are obtained by the method of charge neutrality levels as in [20–26]. In our simulation, we have taken CBO of 1.2 eV for TiO_2/Si interface [24–26].

4. Results and discussion: The different dielectrics with their relative dielectric constants used as gate insulator in the device are listed in Table 1 [20–26]. The simulation study of GAA Si NW, InAs NW, Si DG and CNT FETs in the ballistic regime has been carried out using NanoMOS, Multigate NW FET and Nano Technology Computer Aided Design (TCAD) Versatile Device Simulator (ViDES) simulators [27–29]. Chirality of (13, 0) has

Table 1 Relative dielectric constant and energy bandgaps of different gate dielectric materials [20–26]

Sl. no.	Gate dielectric material	Dielectric constant, k	Energy bandgap, eV
1	SiO_2	3.9	9
2	Al_2O_3	8	8.8
3	HfO_2	25	6
4	La_2O_3	30	6
5	TiO_2	80	3.5

$$p(\boldsymbol{r}) = 2\int_{E_i}^{+\infty} \mathrm{d}E\Big\{\big|\psi_{\mathrm{S}}(E,\ \boldsymbol{r})\big|^2\Big[1 - f(E - E_{F_{\mathrm{S}}})\Big] + \big|\psi_{\mathrm{D}}(E,\ \boldsymbol{r})\big|^2\Big[1 + f(E - E_{F_{\mathrm{D}}})\Big]\Big\} \tag{3}$$

$$I_{\mathrm{D}} = \frac{2q}{h}\int_{-\infty}^{+\infty} \mathrm{d}E\Big\{\mathrm{Tr}\Big[(\Sigma_{\mathrm{S}} - \Sigma_{\mathrm{S}}^{\dagger})G(\Sigma_{\mathrm{D}} - \Sigma_{\mathrm{D}}^{\dagger})G^{\dagger}\Big]\Big\}\Big[f(E - E_{F_{\mathrm{S}}}) - f(E - E_{F_{\mathrm{D}}})\Big] \tag{5}$$

been chosen for CNT to have a similar bandgap with Si and InAs NW [30].

Fig. 2 shows the transfer characteristics of Si DGFET, Si NWFET, InAs NWFET and CNT FET for different gate oxides by varying gate voltage from 0 to 1 V at drain voltage $V_D = 0.5$ V. The drain current has been normalised for a fair comparison between DGFETs and GAA NWFETs. It is observed that the drain current of Si DGFET is smaller as compared with its counterpart GAA NWFET. The drain current plots of all FETs show an increase in drain current with higher gate dielectric materials. In all the graphs, the drain current is higher in case of TiO_2 than the other dielectrics. The higher dielectric constant results in higher gate capacitance which in turn increases the inversion charge. The increase of inversion charge results in higher drain current. Fig. 2 also shows that the on-state drain current (I_{on}) is higher in CNT FET as compared with the other FETs. The Si DGFET has lowest I_{on} current among all the FETs considered.

To have a better understanding, the conduction band edges of the FETs for various dielectrics are also plotted in Fig. 3. It can be seen from the graph that the conduction band edge is lower in case of higher gate dielectric materials. The conduction band edge of FETs with SiO_2 as gate dielectric is higher as compared with that of La_2O_3 and TiO_2. Low conduction band edge energy implies that the conduction occurs at lower energies which make TiO_2 and La_2O_3 better candidates for gate dielectric. Although the gate leakage current associated with TiO_2/Si interface is a matter of concern [31, 32], new reports suggest that low gate leakage current is possible with TiO_2 as gate dielectric in Si MOS systems by using sol–gel spin-coating technique to prepare high-k TiO_2 films on Si substrate [12, 33].

From the transfer characteristics, the variations of SS, DIBL and I_{off} for the transistors with different dielectrics are plotted in Fig. 4. SS plotted in Fig. 4*a* is an important figure of merit which determines how low in power the device technology can be. This parameter quantifies how abruptly the transistor turns on with increasing gate voltage by measuring the amount of gate voltage required to change the drain current by one order of magnitude in logarithmic scale. A smaller value of SS ensures quick turn on or off of the transistor. The graph of SS shows improvement in SS with the use of higher gate dielectrics as reported in [34], while the comparison between different channel FETs shows that CNT FET has better SS characteristics. With CNT as the channel material and TiO_2 as gate dielectric, we obtain almost an ideal value of 60 mV/decade. A comparison between the Si DGFET and Si NWFET shows that the Si NWFET has lower SS as compared with its DG FET configuration implying that GAA NWFETs have superior SS characteristics in comparison with DG FETs.

DIBL is another SCE caused by lowering of source-junction potential barrier due to drain voltage. The source-junction potential barrier is then controlled by both gate and drain voltages which lead to threshold voltage variation with drain voltage. It is always desired to have a lower value of DIBL. The variation of DIBL with gate dielectric material is plotted in Fig. 4*b*. As seen from the graph, DIBL improves with the high-k dielectrics. When comparing the different channel materials and FETs structure, it is observed that CNT exhibits lowest value of DIBL among the channel materials, whereas Si NWFET has lower value of DIBL than Si DGFET implying better immunity to DIBL.

Fig. 4*c* shows I_{off} variation with respect to different gate dielectric materials. Among the dielectrics considered in all the FETs, TiO_2 exhibits lower I_{off} as compared with other dielectrics, whereas Si exhibits lowest I_{off} value of 2.2×10^{-8} A/m while InAs has the highest value of 2×10^{-2} A/m among the channel materials. The high value of I_{off} current in InAs is due to its smaller bandgap as compared with that of Si [30]. Whereas the high value of leakage current in CNT is due to bound states in

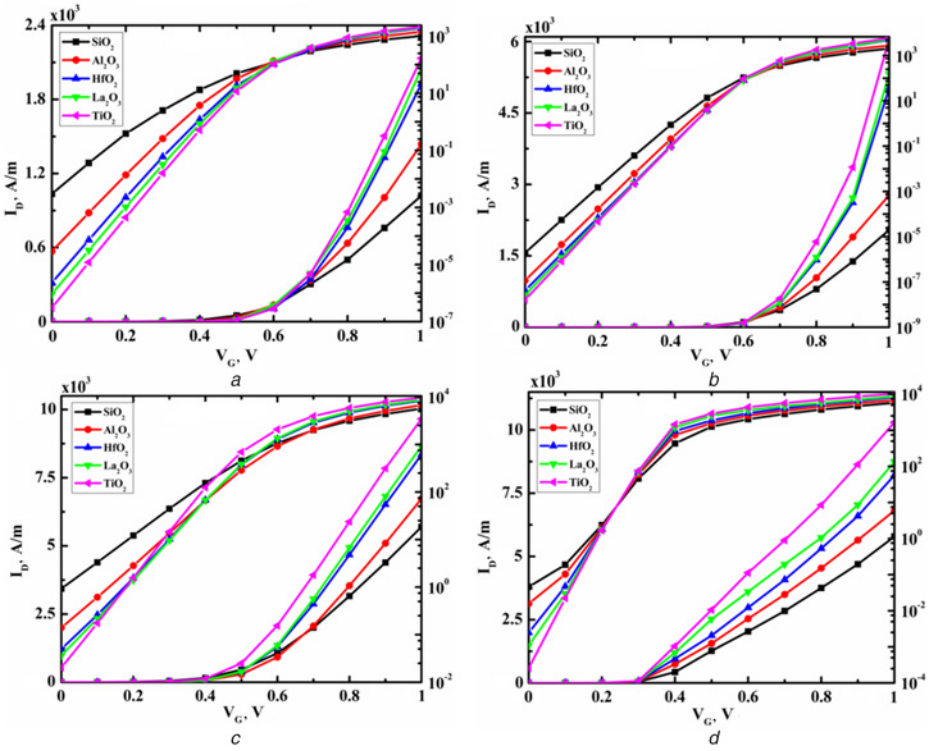

Fig. 2 *Transfer characteristics of*
a Si DG
b Si NW
c InAs NW
d CNT FETs for different dielectrics in linear and logarithmic scales

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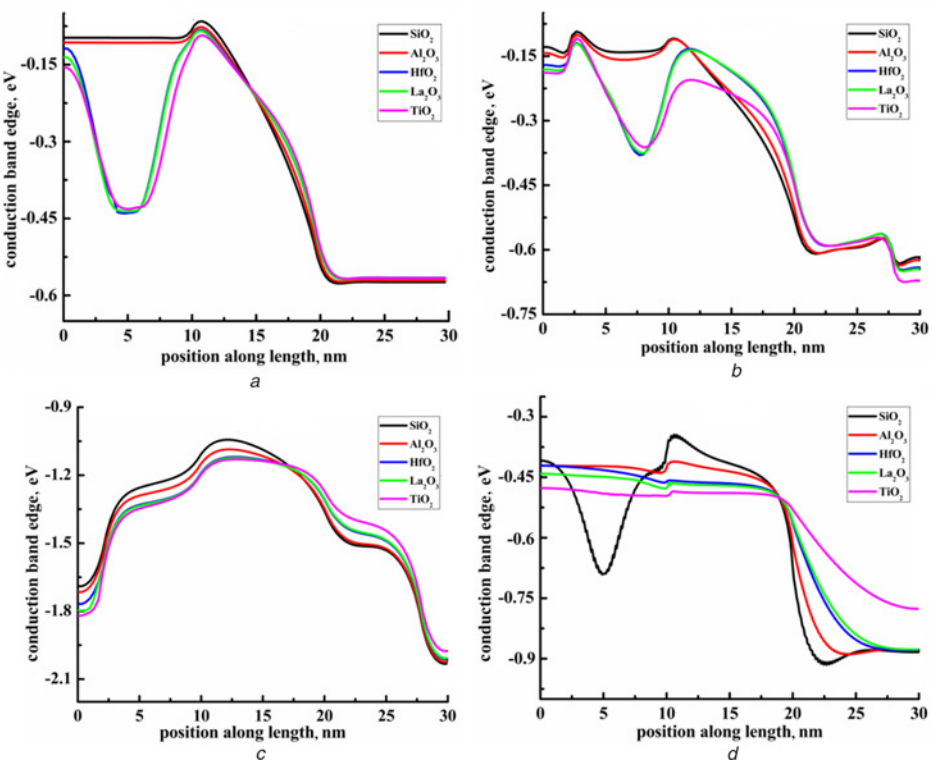

Fig. 3 *Conduction band edge of*
a Si DG
b Si NW
c InAs NW
d CNT FETs at different positions along the length of transistor

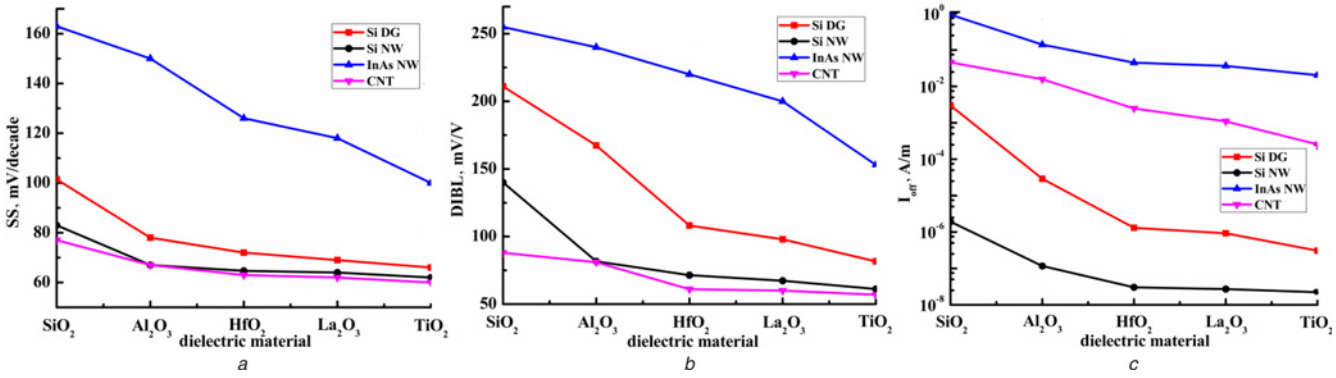

Fig. 4 *Variations of SS, DIBL and I_{off} for the transistors with different dielectrics*
a SS
b DIBL
c I_{off}

the valence band which are occupied by holes tunnelling from drain [35]. Another interesting observation is that Si GAA FET has lower I_{off} current as compared with its DGFET counterpart because of its better gate control over the channel.

In Fig. 5*a*, the comparison of I_{on} versus gate dielectric materials for different channel material and FET structure is plotted. The rising trend of I_{on} with higher values of dielectric constant is observed in all the FETs with different channel materials and structure. The higher on current implies better performance. In all the FETs, highest on current is obtained for TiO_2 as gate dielectric. Among the channel materials the order of increasing I_{on} is Si DGFET, Si NWFET, InAs NWFET and CNT FET. CNT FET shows the highest I_{on} value of 1.03×10^4 A/m, whereas Si DGFET shows the highest I_{on} of 2.1×10^3 A/m for TiO_2 as gate dielectric. The higher I_{on} of CNT can be attributed to the higher mobility of about 5000 cm^2/Vs in CNT as compared with that of Si and InAs [36]. The comparison between the Si DGFET and Si GAA NWFET shows that higher on current is obtained for GAA NWFET.

The on-state to off-state drain current ratio (I_{on}/I_{off}) variation with different gate dielectric materials is plotted in Fig. 5*b*. The plot shows that I_{on}/I_{off} ratio improves with the higher value of relative dielectric constant of gate oxide in all the FETs which indicates TiO_2 to be better substitute for SiO_2 as dielectric. Moreover, the comparison between different channel materials shows that CNT has better I_{on}/I_{off} ratio. This is due to higher on current in CNT.

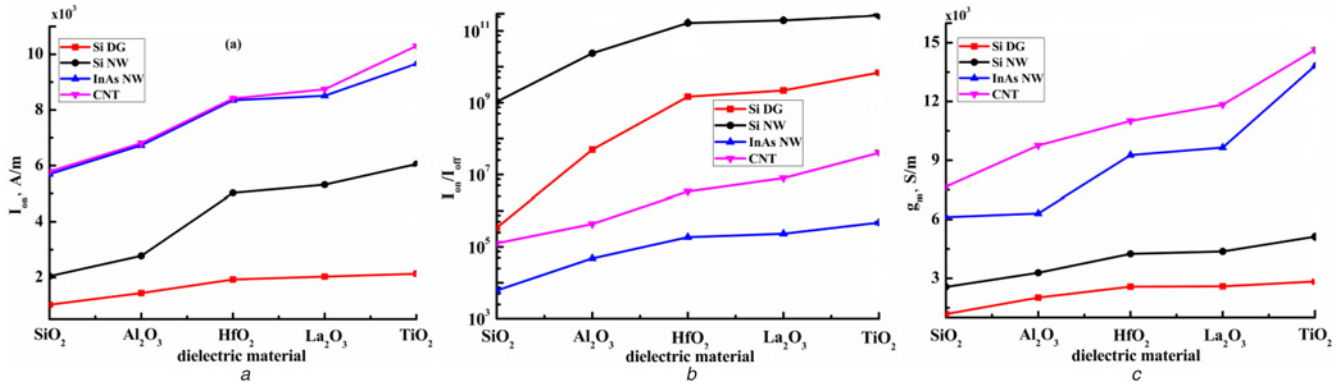

Fig. 5 *Variations of I_{on}, I_{on}/I_{off} ratio and transconductance g_m for the transistors with different dielectrics*
a I_{on}
b I_{on}/I_{off} ratio
c Transconductance g_m

The Si NWFET has higher I_{on}/I_{off} ratio than the Si DGFET indicating better gate control of channel in GAA NWFETs.

The influence of using different gate dielectric materials on the transconductance parameter is addressed next. This is shown in Fig. 5*c*, where transconductance as a function of different gate dielectric materials are plotted for different FETs. It is generally desired to have larger value of g_m in transistor as the larger g_m implies greater gain it is capable of delivering. As the gate oxide relative permittivity increases from SiO_2 to TiO_2, the transconductance increases irrespective of the channel material and FETs structure asserting the fact that TiO_2 is better gate dielectric. It is also clear from the graph that CNT FET has better transconductance than Si and InAs FETs. Moreover, the comparison between Si DGFET and Si NWFET shows that GAA structure is better than DGFET in terms of transconductance.

Fig. 6 plots the variation of equivalent oxide thickness (EOT) as a function of different gate oxides at 1 nm oxide thickness. The EOT for a high-k gate dielectric with permittivity $\varepsilon_{high\text{-}k}$ and thickness $T_{high\text{-}k}$ is defined as

$$\text{EOT} = T_{high\text{-}k}\frac{\varepsilon_{SiO_2}}{\varepsilon_{high\text{-}k}} \tag{7}$$

with ε_{SiO_2} being the permittivity of SiO_2. It implies that a high-k gate dielectric of permittivity $\varepsilon_{high\text{-}k}$ and thickness $T_{high\text{-}k}$ is equivalent to an oxide layer of permittivity ε_{SiO_2} and thickness EOT. If $\varepsilon_{SiO_2}/\varepsilon_{high\text{-}k} \ll 1$, the physical thickness of the high-k gate dielectric $T_{high\text{-}k}$ is much thicker than EOT, thus significantly reducing the gate tunnelling current. From the graph, it is observed that EOT is lowest for the gate oxide material with highest relative permittivity. Thus, TiO_2 has smallest EOT of 0.048 nm.

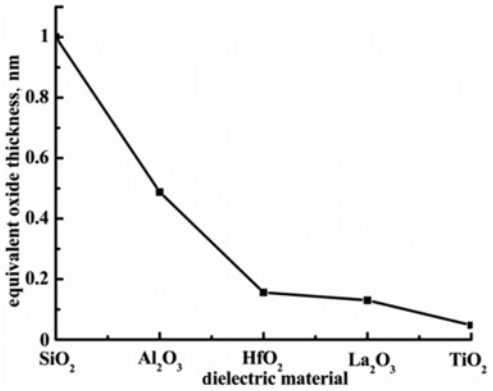

Fig. 6 *EOT versus different gate dielectric materials*

The study of AC performance metrics is as important as the study of SCEs to have a clear picture of comparison between different FETs and also between different dielectrics. Here, we evaluate the high-frequency and switching performance parameters for the FETs. The cut-off frequency f_T is defined as

$$f_T = \frac{g_m}{2\pi C_G}\Big|_{V_D=V_{DD}} \tag{8}$$

where C_g, g_m and V_{DD} are differential gate capacitance, transconductance and supply voltage of 0.5 V, respectively. C_g as a function of dielectric material is shown in Table 2(a) for different FETs. C_g is computed as the derivative of channel charge with respect to the applied gate voltage. A lower value of C_g is desirable for better performance. It is seen that C_g increases for higher-k dielectrics for each channel material and the comparison between different channel materials shows that C_g is lowest for CNT. Moreover, it is also observed that Si NWFET has lower C_g than that of Si DGFET in the range of nF/m. The corresponding f_T is shown in Table 2(b). The f_T shows an increasing trend with the use of higher dielectrics irrespective of channel material. The increase in f_T can be attributed to increase in g_m with high-k dielectric

Table 2 (a) C_g, (b) f_T and (c) τ as a function of dielectric materials

Gate dielectric	Si DG	Si NW	InAs NW	CNT
(a) Differential gate capacitance C_g, F/m				
SiO_2	3.197×10^{-5}	4.946×10^{-9}	5.799×10^{-9}	1.573×10^{-10}
Al_2O_3	3.293×10^{-5}	5.466×10^{-9}	6.012×10^{-9}	1.971×10^{-10}
HfO_2	4.146×10^{-5}	6.933×10^{-9}	6.209×10^{-9}	2.135×10^{-10}
La_2O_3	4.592×10^{-5}	7.068×10^{-9}	6.401×10^{-9}	2.251×10^{-10}
TiO_2	4.805×10^{-5}	8.333×10^{-9}	6.802×10^{-9}	2.576×10^{-10}
(b) Cut-off frequency f_T, Hz				
SiO_2	5.855×10^{6}	8.252×10^{10}	1.679×10^{11}	7.746×10^{12}
Al_2O_3	9.747×10^{6}	9.567×10^{10}	1.673×10^{11}	7.879×10^{12}
HfO_2	9.886×10^{6}	9.760×10^{10}	2.374×10^{11}	8.206×10^{12}
La_2O_3	8.991×10^{6}	9.856×10^{10}	2.399×10^{11}	8.374×10^{12}
TiO_2	9.395×10^{6}	9.796×10^{10}	3.234×10^{11}	9.038×10^{12}
(c) Intrinsic switching delay τ, s				
SiO_2	1.566×10^{-8}	1.208×10^{-12}	5.093×10^{-13}	1.35×10^{-14}
Al_2O_3	1.145×10^{-8}	9.847×10^{-13}	4.460×10^{-13}	1.44×10^{-14}
HfO_2	1.076×10^{-8}	6.903×10^{-13}	3.719×10^{-13}	1.27×10^{-14}
La_2O_3	1.129×10^{-8}	6.645×10^{-13}	3.716×10^{-13}	1.26×10^{-14}
TiO_2	1.125×10^{-8}	6.882×10^{-13}	3.520×10^{-13}	1.25×10^{-14}

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materials. Among the different channel materials considered, CNT has the highest f_T in terahertz (THz) regime making it potential candidate for THz applications. InAs NW and Si NWFETs also show an f_T in 10^{11} and 10^{10} Hz range, whereas Si DGFET shows an f_T of about 10^7 Hz.

Another important digital application performance metric is intrinsic delay or switching time τ, which is given as $\tau = C_g V_{DD}/I_{on}$. The τ is the measure of time an inverter takes to switch, when its output drives another inverter. In Table 2(c), the τ calculated is shown as a function of gate dielectric materials for different FETs. The delay decreases for the increasing relative permittivity of the gate oxide in all the FETs. With TiO_2 as the gate dielectric, the delay is less in all the FETs as compared with that using SiO_2. It is also observed that CNT has the least delay of all the FETs with different channel materials.

5. Conclusion: The effect of high-*k* gate dielectric materials on the short channel parameters has been investigated for Si DGFET, Si NWFET, InAs NWFET and CNT FETs using extensive numerical simulations. From the results obtained in the previous section, we can conclude that SCEs such as DIBL, SS, g_m, I_{on}, I_{off} and I_{on}/I_{off} ratio improves with the high-*k* dielectric materials and multigate FETs because of better electrostatic control of gate over the channel. The results indicate that TiO_2 as the gate dielectric can significantly reduce SCEs making it a possible candidate for replacing SiO_2. The results also show that CNT FETs are less affected by SCEs in comparison with Si and InAs FETs though the leakage current is higher in CNT which leads to lower I_{on}/I_{off} ratio. Furthermore, it is observed that the gate capacitance increases with higher dielectrics because of direct relationship between relative dielectric constant and capacitance. The cut-off frequency increases with higher dielectrics because of increase in the value of g_m and the intrinsic delay also reduces. We have also observed that CNT FETs are advantageous over Si DGFET, Si NWFET and InAs NWFET due to their least gate capacitance and hence lesser delay and improved cut-off frequency, which shows its potential in THz applications.

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