# Multi-valued logic design methodology with double negative differential resistance transistors

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Multi-valued logic (MVL) is one of the promising alternatives of binary logic since it has a high-logic density, which brings a vision of simpler circuit structure. Based on a novel concept as double negative differential resistance field effect transistor and its analytic description, a design methodology utilising the mechanism of monostable-to-multistable transition logic element (MMLE) for MVL is proposed in this study. The basic ternary logic gates are designed as a complete logic set, and a compact ternary four-input full adder is constructed as an example of function circuits. Comparing with binary circuit and ternary circuit based on conventional design, the circuit shows advantage in device cost and other properties. The results verify that this MMLE design methodology has a good information load ability, which will have a brilliant prospect in MVL circuits.

**1. Introduction:** As the rapid development of semiconductor industry, the feature size of IC has shrunk into nanometer. However, many problems, such as interconnect limitation and power dissipation, appear [1], since it has closed to silicon device's physical limitation. Besides the further scale down, one of alternative approaches is multi-valued logic (MVL) circuits [2]. The binary logic has only two steady values (0 and 1) in the Boolean space, while MVL has more states. For example, ternary logic has three steady values (0, 1 and 2). That means the MVL can load larger logic density, and therefore its circuits are promising to deal with more information than the binary logic circuits in the same scale or to reduce circuit complexity [3] on same function.

Except few current mode circuits, such as the MVL states were defined in terms of an integral multiple of reference current [4], most MVLs are realised on the voltage mode. In this mode, multi-threshold COMS logic [5] and negative differential resistance (NDR) logic are the common ones. For the former, as a recent development, carbon nanotube field effect transistor (FET) was employed to design multiple thresholds because of its low power and high performance [6–8]. However, the logic states of the multi-threshold FET-based MVL circuits are decided by the threshold voltages of FETs, hence multiple specifications of transistors must be involved. Predictably, with the logic states increasing in MVL circuits, more specifications of transistors are needed. It will increase the difficulties in device selection and the complexity of circuits. For the latter, more logic states are easy to be realised. For example, using NDR devices, even an eight-value circuit was designed with few devices [9]. The reason of NDR-based circuits more robust is that NDR devices are tend to reach the steady states than the unsteady states [10]. Because of this advantage, the NDR-based MVL occupies the dominant position.

Traditionally, resonant tunnelling diode (RTD) is the representative of NDR devices. Based on it, many MVL circuits work were reported. Such as, multiple-valued quantisers were designed with RTD in [11]. The operating principle of RTD-based MVL circuits was proposed in [12]. A high testability level and low hardware cost test model for multi-valued RTD circuits was implemented in [13]. However since RTD devices have the vertical superlattice structure consisting of different kinds of materials, they are hard to be integrated and scaled down. This drawback severely hinders RTD's application in VLSI, and becomes an obstacle for MVL's development.

As a novel material, graphene has been widely used in various areas. It is a low-dimensional structure and its energy band can be modulated by many methods [14]. So graphene is suitable for constructing a planar superlattice [15] with NDR phenomenon [16], solving the integration problem bothering RTD. As our previous work reported [17], it is possible to build a double NDR (DNDR) FET utilising the non-uniform ribbon width graphene nanoribbon (GNR) channel. Basing on this FET with two NDR regions, compact MVL circuits needing fewer devices and having higher integration are hopeful.

In this Letter, the analytic description of DNDR device is given and the corresponding circuit design methodology based on the mechanism of monostable-to-multistable transition logic element (MMLE) is proposed. The complete set of ternary logic gates is built and a more complex circuit, a four-input ternary full adder (TFA) with four inputs (three addends and one carry input) and 2 outputs (one sum and one carry output), is designed. The results show the designed circuits need few devices comparing with the binary circuits. That verifies our methodology has good information load ability.

The rest of this Letter is organised as follow. Section 2 presents the operation principle of the DNDR GNRFET. Section 3 gives the design methodology of ternary logic gates. The complete design of a TFA is described and discussed in Section 4. The conclusion is drawn in Section 5, respectively.

**2. Operation principles:** Through the tunnelling design by the energy band modulation methods on GNRFET, multiple NDR regions can be realised in one device. For example, Fig. 1*a* gives a proposed device structure by us, whose details can be found in [17]. Fig. 1*b* shows the symbol of that DNDR FET, which combines the features of NDR devices and field effect devices. As a FET like device, the three terminals are named as the source, the drain and the gate. The output characteristic of DNDR FET is given in Figs. 1*c* and *d*. Fig. 1*c* shows the case that the gate-source voltage is 0*V*, two NDR regions are obviously illustrated. The key parameters of it are the following: the first peak current ($I_{p1}$) and the corresponding drain-source voltage ($V_{p1}$), the first valley current ($I_{v1}$) and the corresponding




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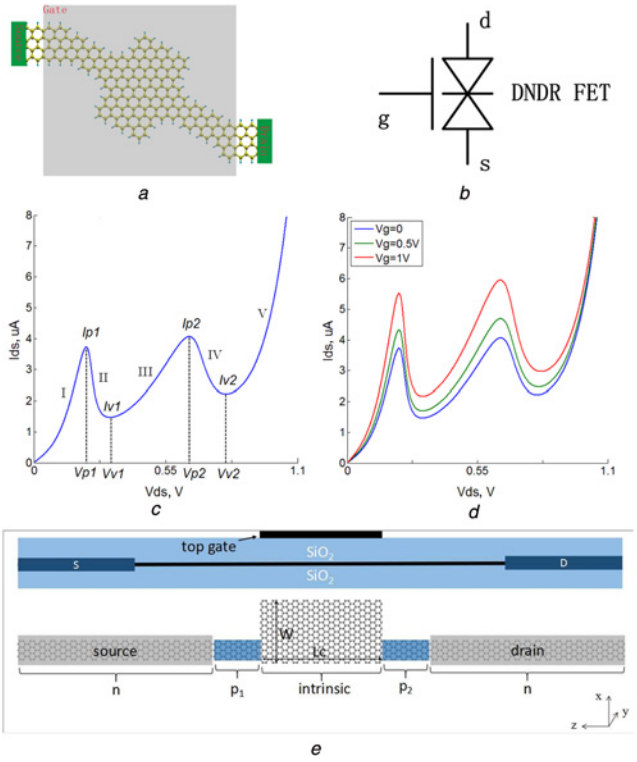


**Fig. 1** *Symbol, structure and characteristic of DNDR FET*
*a* Structure of GNRFET
*b* Symbol and terminals of DNDR FET
*c* Output characteristic when the gate voltage is 0V, key parameters are labelled on the curve
*d* Output characteristic regulated by the gate voltage
*e* Structure of DNDR FET in our on-going work

drain-source voltage ($V_{v1}$), and the same parameters for the second NDR region $I_{p2}$, $V_{p2}$, $I_{v2}$ and $V_{v2}$. Generally, $I_{p2}$ is a little higher than $I_{p1}$. The output curve can be divided into five segments by these parameters. Three of them have positive differential resistances (donated as I, III and V) and the rest two have NDRs (donated as II and IV). If a positive gate-source voltage is applied, the channel current increases, respectively, as shown in Fig. 1*d*.

It is worth to be mentioned that for the aspect of circuit design, the double NDR regions phenomenon is the essential of DNDR device. Not only the structure in Fig. 1*a*, all devices who can give the above output characteristic are rationally choice. Moreover, even nowadays nano devices are not as mature and stable as silicon devices, (the stability of DNDR is improved by the structure in one of our on-going work, shown in Fig. 1*e*), the exploration for their future circuit applications should not be postponed.

To describe DNDR in circuit design, the following compact model is proposed

$$I = A_1 \ln\left(\frac{1+e^{((B-C+n_{11}V)q/kT)}}{1+e^{((B-C-n_{11}V)q/kT)}}\right)\left(\frac{\pi}{2}+\arctan\left(\frac{C-n_{11}V}{D}\right)\right) + A_2 \ln\left(\frac{1+e^{((B-C+n_{12}V)q/kT)}}{1+e^{((B-C-n_{12}V)q/kT)}}\right)\left(\frac{\pi}{2}+\arctan\left(\frac{C-n_{12}V}{D}\right)\right) + H\left(e^{(n_2qV/kT)}-1\right) \quad (1)$$

Equation (1) is a phenomenological formula derived from a RTD compact model [18] that only had one NDR region. We develop it to describe two NDR peaks, as the first and the second items in the right side of (1). The third item is the thermal current. In the equation, $A_1$ and $A_2$ are the parameters decided by the gate voltage $V_g$. They are in direct proportion to ($V_g$–$V_{th}$) when $V_g$ is above $V_{th}$, where $V_{th}$ is the threshold voltage of DNDR FET. When $V_g$ is under $V_{th}$, $A_1 = 0.0026$, $A_2 = 0.0026$. $V$ is the source – drain voltage across FET. The peak voltages are decided by $n_{11}$ and $n_{12}$, as $n_{11} = 0.5$, $n_{12} = 0.2$. $B = 0.035$, $C = 0.139$, $D = 0.01$, $H = 2.7\times10^{-7}$, and $n_2 = 0.25$ are the fitting parameters. This equation is compact and compatible for mainstream SPICE-liked circuit design platforms. Specially, we implemented this model with Verilog-A, and simulated circuits in HSPICE.

The three steady states of ternary logic can be described by a MMLE. In this structure, two DNDR FETs are connected in series and driven by a switching bias voltage $V_{bias}$, as shown in Fig. 2*a*. As a comparison, traditionally, four RTDs are needed for this circuit, which shows our DNDR circuit's advantage in integration. The MMLE changes from monostable state to multistable state periodically with the oscillating supply voltage $V_{bias}$, it can be illustrated by sweeping the load curve over the driver curve from low $V_{bias}$ to high $V_{bias}$ as Fig. 2*b*. When a low $V_{bias}$ is applied, the load curve and the driver curve have only one intersection point. It means the MMLE has only one stable operation point, which is a monostable state, and load FET and driver FET both work in Segment I. With the increase of $V_{bias}$, the load curve moves and three intersection points appear. It means the MMLE has three steady states, as the low, medium and high voltage values in $V_{out}$. They are the logic '0', '1' and '2', respectively.

The states of MMLE are decided by the peak currents of every DNDR FET. In a MMLE there are four peak currents, as the $I_{p1}$ and $I_{p2}$ of the load FET (named as $I_{p11}$ and $I_{p12}$), and the $I_{p1}$ and $I_{p2}$ of the driver FET (named as $I_{p21}$ and $I_{p22}$). According to the sequence of these four peak currents changing form low to high, states transition happens in corresponding FETs one after another. Specifically, if they have the relation as $I_{p11} < I_{p12} < I_{p21} < I_{p22}$, when the rising edge of $V_{bias}$ arrives, the load FET works in Segment V, and the driver FET works in Segment I. Hence the operation point of MMLE is 'low', and the logic value showed in $V_{out}$ is '0'. If $I_{p11} < I_{p21} < I_{p12} < I_{p22}$ or $I_{p21} < I_{p11} < I_{p22} < I_{p12}$, the load and the driver FETs both work in Segment III, so the operation point is 'medium', and the logic value is '1'. If $I_{p21} < I_{p22} < I_{p11} < I_{p12}$, the load FET works in Segment I and the driver FET works in Segment V, the operation point is 'high', and the logic value is '2'. Since the peak currents of driver FET are decided by

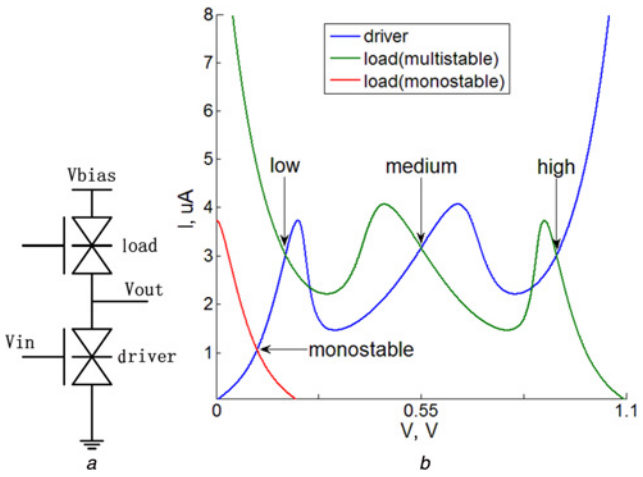


**Fig. 2** *Analysis of MMLE*
*a* Circuit of MMLE. It is constructed by a driver DNDR FET and a load one
*b* Function of MMLE. The MMLE circuit is in the monostable (red) and the multistable (green) phase, with $V_{bias} = 0.22$ V and $V_{bias} = 1.1$ V, respectively

its gate voltage, the logic function of MMLE is controlled by the gate voltage, similar as normal FET circuits.

By the way, in order to make the MMLE working in the multi-stable state, $V_{bias}$ is set as 1.1 V in our designed ternary circuits. The voltage levels for three logic values are appointed as Table 1.

**3. Complete set of ternary logic gates:** The basic operations of ternary logic can be defined as following, where $X, Y = \{0, 1, 2\}$ [19],

$$\begin{aligned} \overline{X} &= 2 - X \\ X + Y &= \max\{X, Y\} \\ X \cdot Y &= \min\{X, Y\} \end{aligned} \tag{2}$$

Beside the above NOT, OR and AND operations, the literal operation as (3) is introduced into ternary basic operations, in order to make up a complete set of ternary logic

$${}^{i}X^{i} = \begin{cases} 2, (X = i) \\ 0, (X \neq i) \end{cases} \tag{3}$$

where $i = \{0,1,2\}$. Implementing these operations by DNDR FETs, all ternary logic can be designed.

Ternary inverter is the simplest ternary gate. In fact, it is a MMLE with a stable gate voltage of FET1, shown as Fig. 3*a*. The gate terminal of FET2 is the input port of inverter. When input is '0', the operation point of MMLE is 'high', FET1 works in Segment V and FET2 works in Segment I, so the output is '2'. When input is '1', the operation point is 'medium', and FET1 and FET2 both work in Segment III, hence the output is '1'. When input is '2', the operation point is 'low', FET1 works in Segment I and FET2 works in Segment V, and the output is '0'. The simulation results in Fig. 3*b* confirm the function of our design. It is worth to be mentioned that since all the biases are set as $V_{bias}$, as the DC in Fig. 3*a* and the following circuits, a voltage reference can supply it. Not too much cost is added.

**Table 1** Logic values corresponding voltage lecel level

| Logic value | Voltage level, V |
|---|---|
| 0 | 0–0.2 |
| 1 | 0.4–0.6 |
| 2 | 0.9–1.1 |

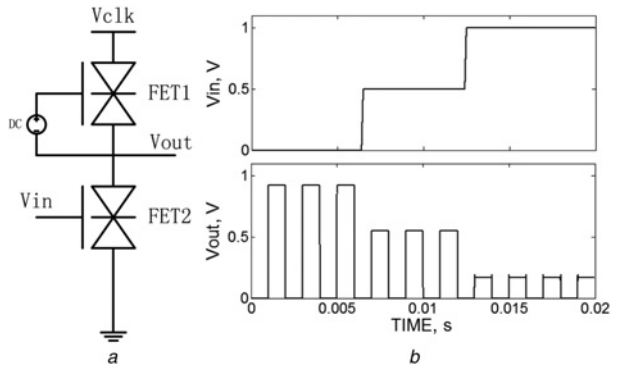


**Fig. 3** *Designed inverter*
*a* Circuit of ternary inverter
*b* Its simulated function

The designed NOR gate is shown in Fig. 4*a*. According to our MMLE methodology, in this circuit the driver part is in parallel. The two input control the DNDR processes of the drivers. The increase of each input voltage lead to the driver's peak current rise and change MMLE's state. The simulation results in Fig. 4*b* confirm the function of our design.

To design NAND and literal gate compactly, MOSFET is introduced here. As a rapidly developing graphene device, graphene FET (GFET) [20] is planar and is compatible with our DNDR GNRFET. Using it in the circuits, no other material or complex procedure is added. The merit of our design is not influenced by it. The NAND gate shows in Fig. 5*a*. It is constructed by 3 DNDR FETs and 2 GFETs as switch. When an input is '0', the corresponding GFET works in the cut-off state and the current of this branch is near zero. When an input is '1' or '2', the GFET turns on and the current of this branch is decided by the corresponding DNDR FET, the whole circuit works as a MMLE. The simulation results in Fig. 5*b* confirm the function of our design.

Literal gates of ternary logic have three forms, the '0' literal gate, the '1' literal gate and the '2' literal gate. As the representative of them, the circuit of '1' literal gate is illustrated in Fig. 6*a*. That is constructed by two MMLEs and 1 GFET. The simulation results in Fig. 6*b* confirm the function of our design.

In a short, from the above basic logic gates, one can see MMLE is the idea of our design methodology for ternary circuits.

**4. Ternary full adder:** As a relative complex function, a TFA is designed to verify our methodology's ability in function circuits. The TFA has four inputs and two outputs, and its circuit structure is showed in Fig. 7, in which $x$, $y$ and $z$ are the three addends, $C_i$ is the carry input, $S$ and $C_o$ are the sum and the carry output,

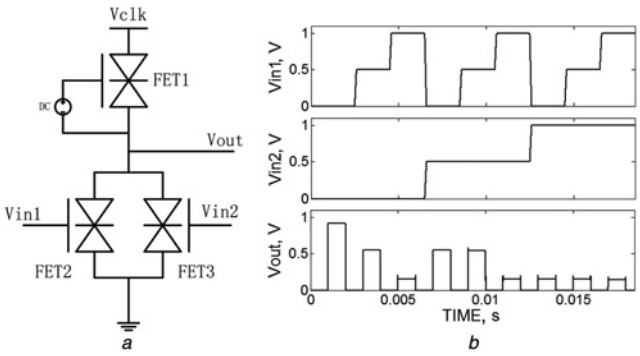


**Fig. 4** *Designed NOR gate*
*a* Circuit of ternary NOR gate
*b* Its simulated function

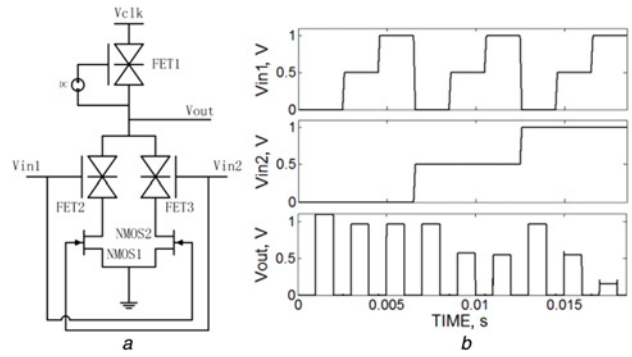


**Fig. 5** *Designed NAND gate*
*a* Circuit of ternary NAND gate
*b* Its simulated function




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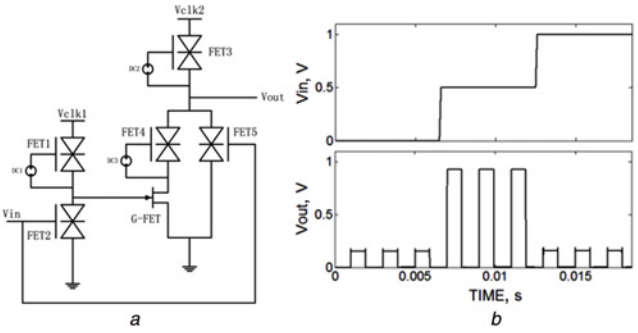


**Fig. 6** *Designed '1' literal gate*
*a* Circuit of '1' literal gate
*b Its simulated function*

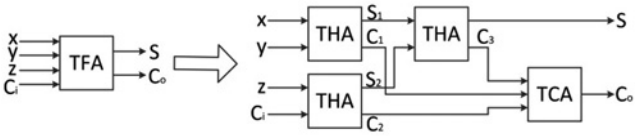


**Fig. 7** *Structure of TFA. It is constituted by 3 THAs and 1 TCA. $S_1$, $S_2$ and S are the sum of 3 THAs, S also is the sum output of TFA. $C_1$, $C_2$ and $C_3$ are the carry output of 3 THAs*

respectively. The full adder is constituted by three ternary half adders (THAs) and 1 ternary carry signal adding module (TCA).

The Karnaugh map of the sum of THA is shown in Fig. 8*a*. Following it, the sum circuit of THA can be directly designed by (4) with basic NDNR ternary logic gates. However, in this way the circuit is relative complex. The biggest advantage of MVL, dealing with high logic density with fewer devices, is impaired, especially with big data width. Hence obeying our MMLE methodology, another design is proposed. The Karnaugh map of the sum of THA is transformed to the forms in Fig. 8*b*. Besides the forms of symmetry about diagonal, more important, all of the three parts' logic values increase with the increase of the sum of $x$ and $y$. By the virtue of these two features, the corresponding Karnaugh maps can be realised by MMLE type structures

$$S = x \cdot {}^0y^0 + {}^0x^0 \cdot y + {}^1x^1 \cdot {}^1y^1 + 1 \cdot {}^2x^2 \cdot {}^2y^2 \qquad (4)$$

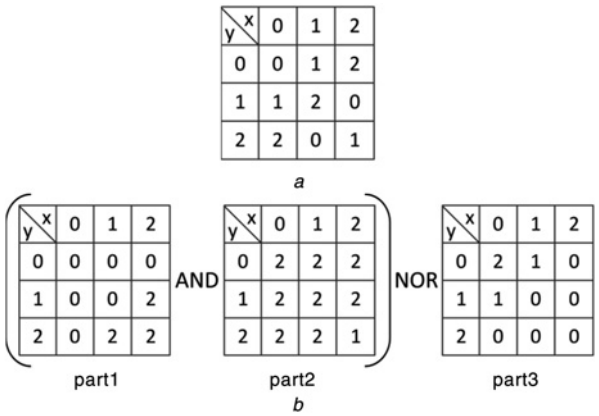


**Fig. 8** *Sum circuit of THA can be directly designed by (4) with basic NDNR ternary logic gates, which are suitable for our MMLE methodology*
*a* Karnaugh map of the sum of THA
*b* It can be decomposed to the forms

The circuit of the sum of THA is designed as Fig. 9. In which, part2 and part3 have the same circuit structure like NOR gate, while their logic functions are implemented, respectively, by applying different gate voltages on load FETs.

The Karnaugh map of the carry of THA is shown in Fig. 10*a*, which also follows the MMLE methodology. The circuit structure is shown in Fig. 10*b*.

As shown in Fig. 7, the function of TCA is to count the sum of three carry signals from the three THAs. Since the carry signals only have two states (0 and 1), and at any time there are two carry signals can be logic '1' at most according to the logic function of TFA, TCA's truth table is simplified as Table 2. Following it, the circuit of TCA is designed as Fig. 11, using six DNDR FETs.

Combining the THAs and the TCA following Fig. 7, the whole TFA is got. Fig. 12*a* gives the simulation results at 1.1 V clock supply, which verify our design's correctness. The stability of this DNDR circuit is tested as Fig. 12*b*. Without loss of generality, two glitches are added in one input as $X$ at the first two periods, meantime $Y$ is '2' and the other input is '0'. In this case, the

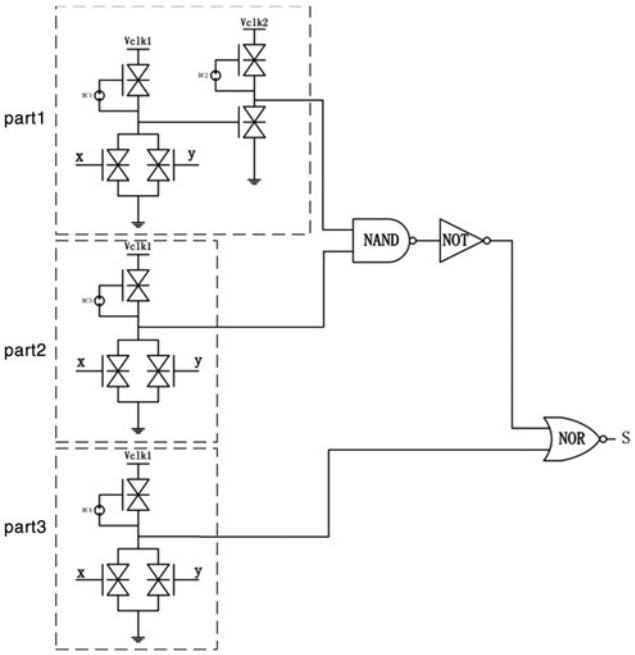


**Fig. 9** *Circuit of the sum of THA. It is designed with Fig. 8b. The circuits of NAND, NOT and NOR gates are given in Section 3*

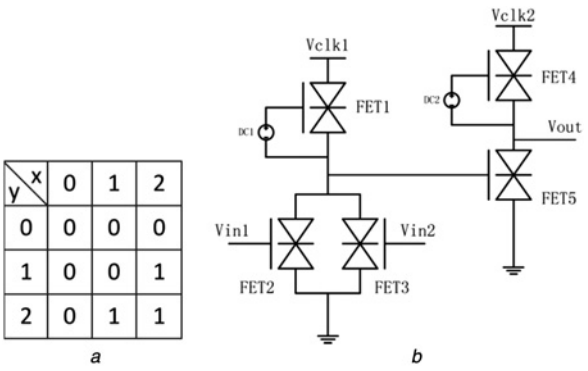


**Fig. 10** *Function of TCA is to count the sum of three carry signals from the three*
*a* Karnaugh map of the carry of THA
*b* Principle of methodology of MMLE-based ternary circuit

**Table 2** Truth table of TCA

| $C_1$ | $C_2$ | $C_3$ | $C_o$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 2 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 2 |
| 1 | 1 | 0 | 2 |

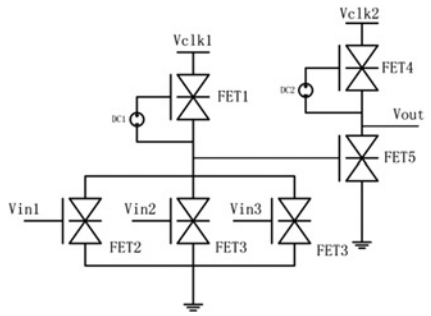


**Fig. 11** *Circuit of TCA. It also bases on MMLE, where the driver is 3 DNDR FETs in parallel*

output maintains steady. That should be owed to the good stability of DNDR FET, in which state transition occurs at the edge of clock voltage. Hence if the clock keeps stable, the status and output of circuit will remain even the input changes. Besides that, the noise margin is explored. Different from the standard voltage values as 0, 0.5 and 1 V for '0', '1'and '2', at the fourth period in Fig. 12*b*, the voltage of $X$ is set as 0.2 V, and the voltage of $Y$ is set as 0.85 V. The output is correct as $X$ = '0' and $Y$ = '2'. At the fifth period, the voltage of $X$ and $Y$ is set as 0.4 and 0.6 V, the output is correct as they both represent '1'. From above one can see that the noise margin of this circuit is as 0–0.2 V represents '0', 0.4–0.6 V represents '1', and 0.85–1 V represents '2'. It is a wide range considering the voltage scale and logic numbers.

Fig. 13 gives the device cost comparison between our TFA and the binary full adder, while the TFA without MMLE methodology is also illustrated as a reference. The binary full adder follows the construction presented in [21], and the other TFA uses conventional design following the basic ternary logic expression. Loading the same amount of information, obviously our methodology needs the fewest devices. Furthermore, with the expansion of information, the gap between them increases continuously. Specifically, at the information amount as $2\times10^{16}$, our MMLE TFA saves 19.8% devices to the binary full adder. At the amount as $2\times10^{64}$, our MMLE TFA saves 25.3% devices. That means our method shows better performance in large scale of data, which is benefit for complex circuit design and integration.

It is interesting that the rough TFA without logic improvement even costs more devices than the binary ones. The reason is without improvement, the ternary logic expressions are more complex than the binary ones, since normal logic expressions have been optimised for the binary logic. It uncovers that besides multi-valued devices, corresponding multi-valued design methodologies are also critical for the development of MVL.

The simulation results about delay and average power of two kinds of DNDR FET-based TFAs are showed in Table 3. Our proposed TFA is 54.5% shorter in time delay at 1 MHz clock, and 64.3% less in power. Those also verify our methodology's advantage. By the way, with the development of graphene and other novel nanoscale devices, there is a big room to improve their

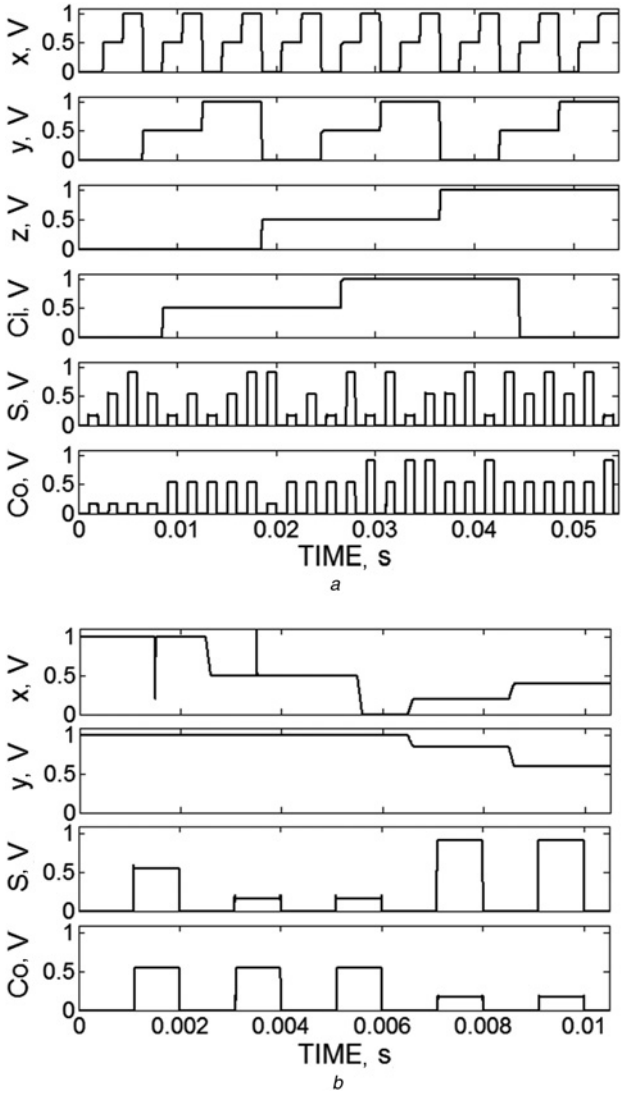


**Fig. 12** *Device cost comparison between our TFA and the binary full adder*
*a* Simulation results of the whole TFA
*b* its stability analysis

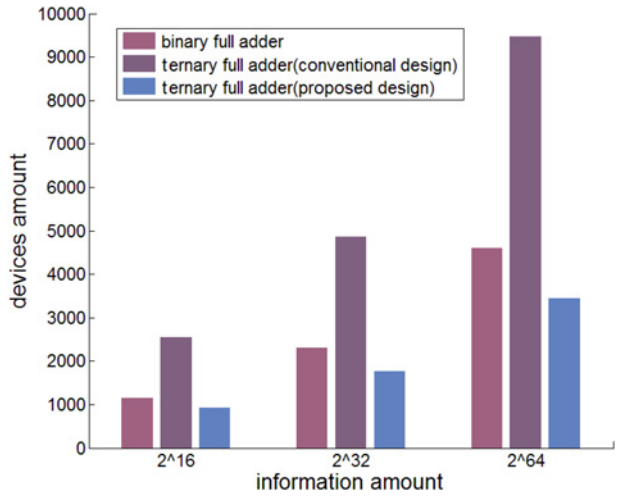


**Fig. 13** *Comparison of the devices number used in the TFA with the binary full adder and the TFA based on conventional design under different amounts of information*




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**Table 3** Delay and average power of two TFAs

| Ternary full adder | Delay, nS | Average power, mW |
|---|---|---|
| conventional design | 110 | 25.774 |
| proposed design base on MMLE | 50 | 9.19 |

device performance and circuit capability in near future, and so circuit's delay and power consumption can be further decreased.

**5. Conclusion:** In this Letter, a MMLE-based design methodology for ternary logic circuit is proposed. With a novel concept as DNDR FET, complete set of ternary logic gates are constructed and a TFA is designed as the example of function circuits. The device cost comparisons with the binary circuits show our methodology is superior in logic density and information load ability. Its circuit performance is also better than the conventional ternary method. We hope it can promote the blossom of MVL and open a new door for the future development of high density integrated circuits.

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