

PSOI pLDMOS with n-buried layer

Lijuan Wu , Yue Song, Hang Yang, Limin Hu, Bing Lei, Na Yuan, Yinyan Zhang, Zhongjie Zhang

School of Physical and Electronic Science, Changsha University of Science and Technology, Changsha 410114, People's Republic of China

✉ E-mail: 413675452@qq.com

Published in Micro & Nano Letters; Received on 7th April 2017; Revised on 7th May 2017; Accepted on 23rd May 2017

Partial-silicon (Si)-on-insulator p-channel lateral double-diffused metal–oxide–semiconductor field-effect transistor with n-buried layer (NBL PSOI pLDMOS) is proposed. One feature of the device is an Si window under the drain offers a heat conduction path to alleviate the self-heating effect. Meanwhile, a fully depleted NBL on the bottom surface of the Si layer provides a large amount of ionised donors to enhance the electric field of the buried oxide (BOX) layer. The NBL can prevent the substrate leakage phenomenon of the PSOI pLDMOS. There is a triple reduced surface field structure in the p-drift region. Some equipotential lines spread into the p-substrate through the Si window. Furthermore, the assistant depletion caused by the NBL increases the p-drift region concentration, which achieves a lower specific on-resistance ($R_{on,sp}$). With 20 μm p-drift region length and 1 μm BOX thickness, the NBL PSOI pLDMOS obtains a higher breakdown voltage (BV) of 289 V, which is increased by 88.9 and 43.8% compared with the Con SOI and NBL SOI pLDMOS, respectively. The $R_{on,sp}$ is decreased by 82.3 and 17.2%, respectively. The figure of merit ($\text{FOM} = \text{BV}^2/R_{on,sp}$) is 1.65 MW cm^{-2} . A lower maximum surface temperature of 312.3 K is obtained.

1. Introduction: In high-side switch applications, the p-channel lateral double-diffused metal–oxide–semiconductor field-effect transistor (pLDMOS) has more advantages than the n-channel LDMOS (nLDMOS) such as dispensability of a charge pump for gate driving [1, 2]. However, the mobility of electrons is pretty much higher than that of the holes, which results that the specific on-resistance ($R_{on,sp}$) of the pLDMOS is much higher than that of the nLDMOS [3].

We must design some new structures for the pLDMOS to improve the relationship between the breakdown voltage (BV) and $R_{on,sp}$ [3]. Reduced surface field (RESURF) technology is one of the most common methods for the design of the lateral high-voltage devices with low on-resistance [4, 5]. Compared to single or double RESURF, triple RESURF technology is more effective to optimise the relationship between the BV and $R_{on,sp}$ [5–8]. For silicon (Si)-on-insulator (SOI) pLDMOS, enhancing the electric field of the buried oxide (BOX) layer with the ENhanced Dielectric layer Field (ENDIF) rule can solve the problem of low BV [9, 10], and introducing interface charges to increase the electric field of the BOX is one of the most effective methods [11, 12]. Moreover, SOI pLDMOS also suffers from the self-heating effect (SHE). Partial-SOI (PSOI) technology can be used to solve the SHE, and it is a pretty good way for increasing BV due to the presence of an Si window [12–14].

On the basis of the research of the PSOI nLDMOS with buried n-type layer [14], we introduce an n-buried layer in the PSOI pLDMOS (NBL PSOI pLDMOS) in this Letter. The working mechanism of the proposed NBL PSOI pLDMOS is discussed and the electrical characteristics of the device are analysed seriously.

2. Structures and mechanism: Fig. 1b shows the NBL SOI pLDMOS is introduced an NBL in the p-drift region, compared with the conventional SOI pLDMOS (Con SOI pLDMOS) which is shown in Fig. 1a. The NBL, p-drift region, and n-top layer constitute a triple RESURF structure to improve the BV and reduce the $R_{on,sp}$. Fig. 1c depicts the schematic representation of the proposed NBL PSOI pLDMOS structure with an NBL on the bottom surface of the Si layer. In contrast to the NBL SOI pLDMOS, the proposed NBL PSOI pLDMOS has an Si window under the drain.

As shown in Fig. 1c, for the NBL PSOI pLDMOS, the Si window can provide a heat conduction path to solve the SHE. Owing to the presence of the Si window, the fully depleted NBL and the p-substrate can be depleted with each other, leading to a higher doping concentration of the NBL. Moreover, more electric fields are introduced in the substrate so that a higher BV is obtained. Like the NBL SOI pLDMOS, the NBL provides a large amount of ionised donors to enhance the electric field of the BOX. However, the NBL PSOI pLDMOS has a higher n-buried concentration than the NBL SOI pLDMOS, which leads to a better efficiency in depletion of the drift region.

Finally, it gets a lower $R_{on,sp}$ than the Con SOI and NBL SOI pLDMOS. Moreover, the NBL can also prevent the substrate leakage phenomenon of the PSOI pLDMOS. Fig. 1d shows the vertical electric field distribution under the source ($x = 0.01 \mu\text{m}$, along the AA' line) of the NBL PSOI pLDMOS, where E_I is the electric field value of the BOX. The vertical electric field distribution below the surface at the middle ($x = 15 \mu\text{m}$, along the BB' line) of the NBL PSOI pLDMOS is shown in Fig. 1e, where E_{II} is the electric field value of the BOX. Moreover, we can see there are three electric field peaks in the drift region. The substrate is connected to the drain for the pLDMOS.

3. Results and discussion: The simulated device parameters using device simulator Medici are listed in Table 1.

Fig. 2a shows the influence of the p-drift region concentration (P_d) and NBL concentration (N_n) on the BV and $R_{on,sp}$ for the NBL PSOI pLDMOS when the NBL thickness (T_n) is 0.5 μm and the Si window length (L_w) is 12 μm . According to the RESURF theory, the maximum BV is reached when breakdown occurs in the bulk, whereas premature breakdown occurs at the surface for a too low or too high P_d . Therefore, when T_n is 0.5 μm , L_w is 12 μm , and N_n is constant, as P_d increases, the BV first increases and then decreases. Meanwhile, the $R_{on,sp}$ with the increasing of P_d has been reduced. Obviously, the optimal value of the BV increases first and then decreases with the increasing of N_n . When T_n is 0.5 μm , N_n is $7 \times 10^{16} \text{ cm}^{-3}$, and P_d is $13 \times 10^{15} \text{ cm}^{-3}$, the maximum BV of the NBL PSOI pLDMOS is 297 V, the $R_{on,sp}$ is 55.5 $\text{m}\Omega \text{ cm}^2$ and the figure of merit (FOM) is 1.59 MW cm^{-2} . When T_n is 0.5 μm , N_n is $8 \times 10^{16} \text{ cm}^{-3}$, and P_d is $15.5 \times 10^{15} \text{ cm}^{-3}$, the BV of the NBL PSOI pLDMOS is 289 V which is

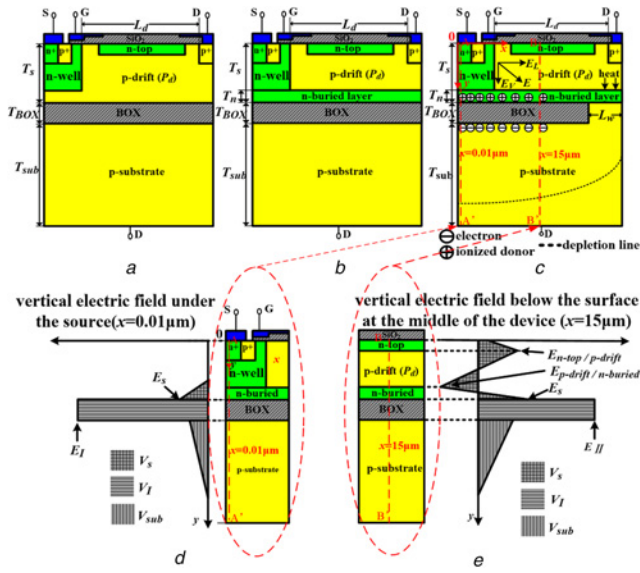


Fig. 1 Structures of the Con SOI pLDMOS, NBL SOI pLDMOS, and NBL PSOI pLDMOS with its mechanism and vertical electric field distributions
a Con SOI pLDMOS
b NBL SOI pLDMOS
c NBL PSOI pLDMOS with its mechanism
d Vertical electric field distribution under the source ($x=0.01 \mu\text{m}$) of the NBL PSOI pLDMOS
e Vertical electric field distribution below the surface at the middle ($x=15 \mu\text{m}$) of the NBL PSOI pLDMOS

Table 1 Device parameters used in the simulations

Device parameters	NBL PSOI pLDMOS	Unit
length of drift region, L_d	20	μm
thickness of Si layer, T_s	3	μm
thickness of BOX, T_{BOX}	1	μm
thickness of NBL, T_n	0.5	μm
length of Si window, L_w	12	μm
thickness of n-top layer, T_{top}	0.5	μm
doping of n-top layer, N_{top}	5×10^{16}	cm^{-3}
P-substrate concentration, P_{sub}	8×10^{14}	cm^{-3}
P-drift region concentration, P_d	optimised	cm^{-3}
doping of NBL, N_n	optimised	cm^{-3}

slightly lower than 297 V, but the $R_{\text{on,sp}}$ is $50.6 \text{ m}\Omega \text{ cm}^2$ which is lower than $55.5 \text{ m}\Omega \text{ cm}^2$ and the FOM is 1.65 MW cm^{-2} .

Fig. 2b shows the influence of T_n on the BV, $R_{\text{on,sp}}$, and FOM for the NBL PSOI pLDMOS when L_w is $12 \mu\text{m}$. With the increasing of T_n , the BV and FOM decrease. Moreover, the $R_{\text{on,sp}}$ increases. Finally, we choose the optimal parameters when the FOM becomes the maximum value, that is, T_n is $0.5 \mu\text{m}$, P_d is $15.5 \times 10^{15} \text{ cm}^{-3}$, and N_n is $8 \times 10^{16} \text{ cm}^{-3}$. Later, we will discuss the influence of the window length on the BV, $R_{\text{on,sp}}$, electric field, potential, and maximum surface temperature (T_{max}) for the Con SOI, NBL SOI, and NBL PSOI pLDMOS.

Fig. 3 plots the equipotential contours for the Con SOI, NBL SOI, and NBL PSOI pLDMOS at breakdown. We can observe that the equipotential contours of the NBL PSOI pLDMOS ($L_w = 12 \mu\text{m}$, $BV = 289 \text{ V}$) are the most uniformly distributed as shown in Fig. 3c, whereas those of the Con SOI pLDMOS are the most unevenly distributed as shown in Fig. 3a. For the NBL SOI or NBL PSOI pLDMOS, the NBL which is completely depleted can help to deplete the drift region, modulate the drift region electric field, and make the equipotential contours distribution more uniform. The fully depleted NBL offers a large number of ionised donors to enhance the electric field of the BOX. Therefore, the BV is

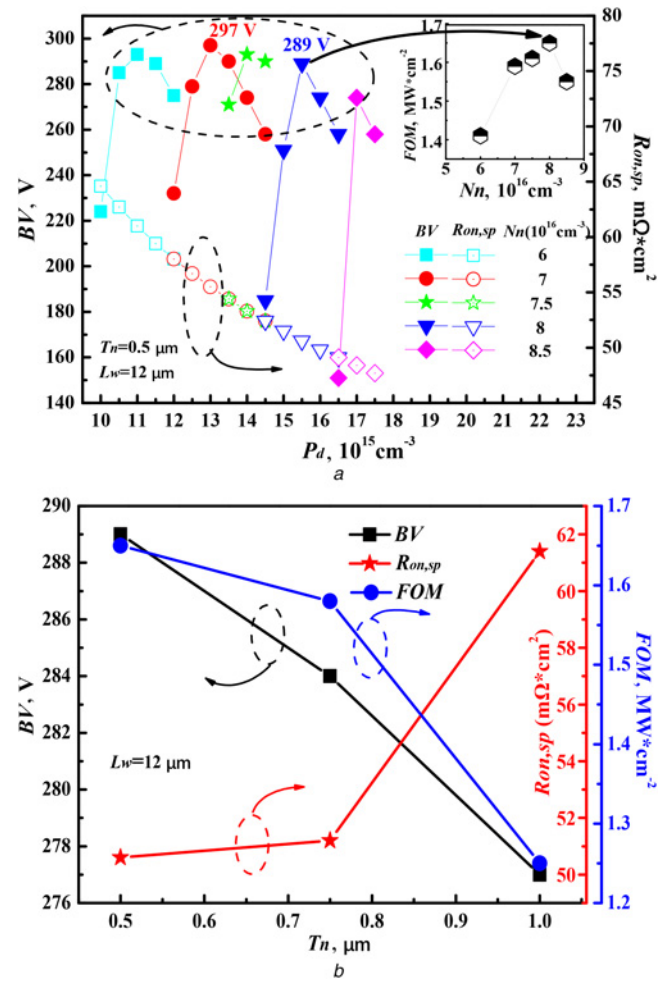


Fig. 2 BV, $R_{\text{on,sp}}$, and FOM against P_d , N_n , and T_n for the NBL PSOI pLDMOS
a BV, $R_{\text{on,sp}}$, and FOM against P_d and N_n when T_n is $0.5 \mu\text{m}$ and L_w is $12 \mu\text{m}$
b BV, $R_{\text{on,sp}}$, and FOM against T_n when L_w is $12 \mu\text{m}$

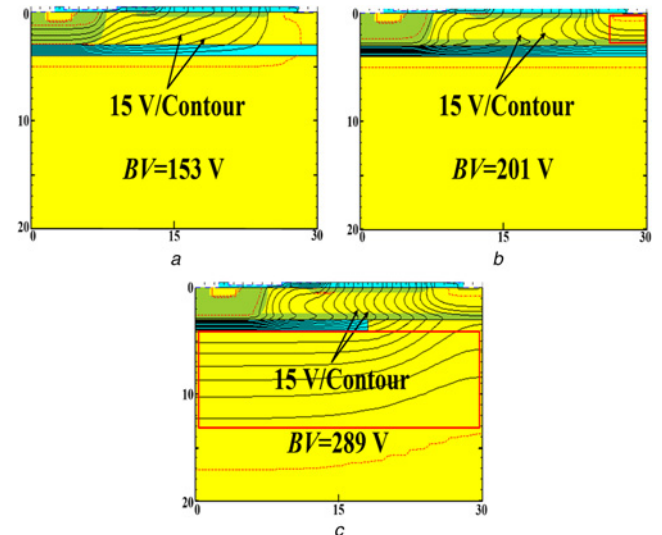


Fig. 3 Equipotential contours for the three devices at breakdown
a Con SOI pLDMOS
b NBL SOI pLDMOS
c NBL PSOI pLDMOS

improved and the $R_{\text{on,sp}}$ is reduced compared with the Con SOI pLDMOS. The equipotential contours distribution of the NBL SOI pLDMOS is shown in Fig. 3b. Furthermore, compared with

the NBL SOI pLDMOS, the NBL depletes with the substrate due to the presence of the Si window. Moreover, some equipotential lines spread into the p-substrate, resulting in the substrate sharing the BV for the NBL PSOI pLDMOS. Consequently, the NBL PSOI pLDMOS can achieve a higher BV than the NBL SOI pLDMOS.

Fig. 4a depicts the vertical electric field distributions along the y -direction under the source ($x=0.01\text{ }\mu\text{m}$) for the three devices.

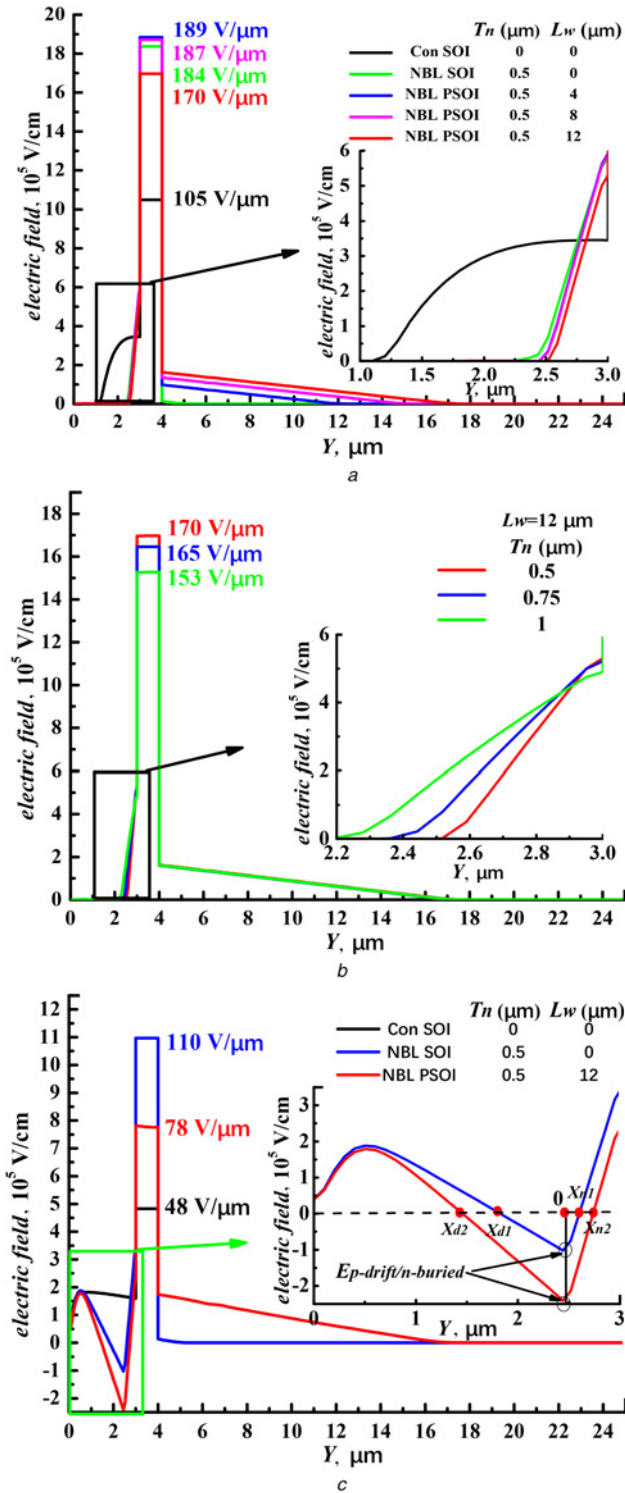


Fig. 4 Electric field distributions along the y -direction at breakdown
a Under the source for the three devices
b Under the source for the NBL PSOI LDMOS at L_w is $12\text{ }\mu\text{m}$
c Below the surface at the middle of the device for the three devices at x is $15\text{ }\mu\text{m}$

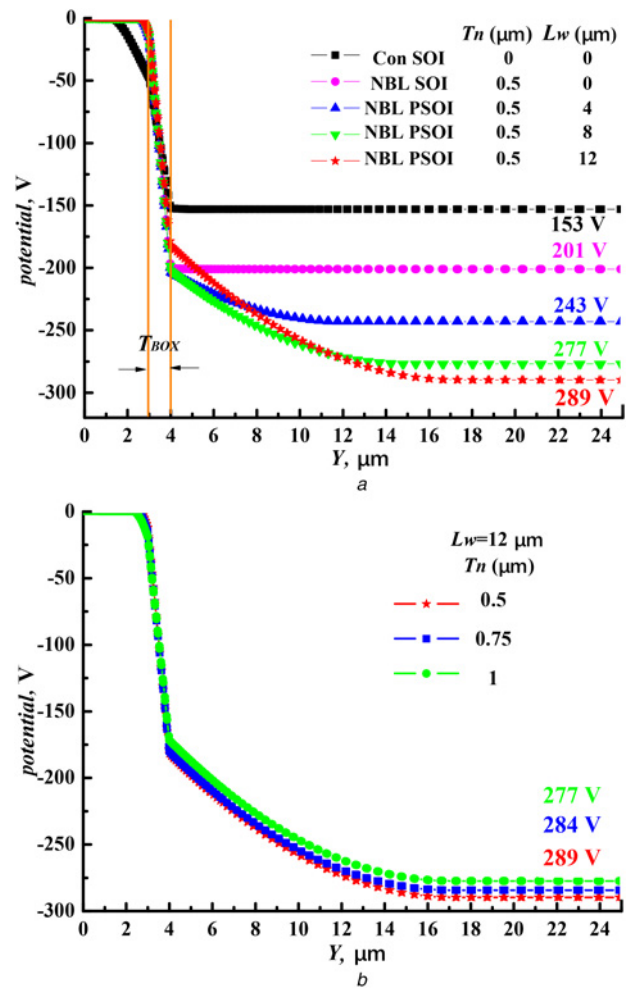


Fig. 5 Distributions of the vertical potential
a Three devices
b NBL PSOI pLDMOS at $L_w = 12\text{ }\mu\text{m}$

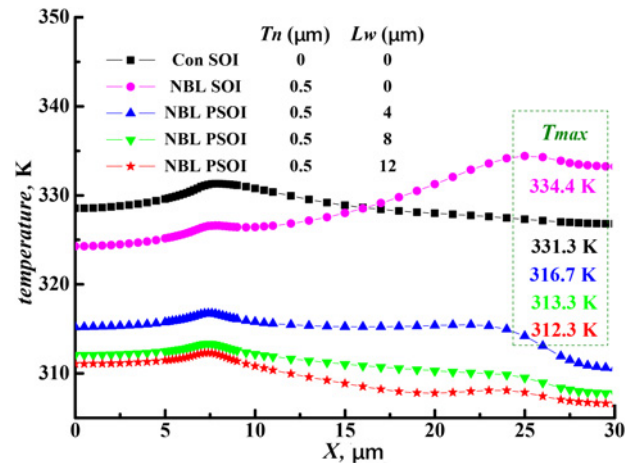


Fig. 6 Surface temperature of the Con SOI, NBL SOI, and NBL PSOI pLDMOS ($V_g = -15\text{ V}$, $T_{sub} = 300\text{ K}$, and $P = 1\text{ mW}$)

We can see the substrate of the Con SOI or NBL SOI pLDMOS hardly shares the BV. The vertical BV of the Con SOI pLDMOS is shared by the drift region and BOX. For the NBL SOI pLDMOS, the BOX mainly sustains the BV, because the NBL offers a large number of ionised donors to enhance the electric field of the BOX. For the NBL PSOI pLDMOS, as the length

Table 2 Parameters comparison for the three devices

Structure type	BV, V	ΔBV , %	P_d , 10^{15} cm^{-3}	$R_{on, sp}$, $\text{m}\Omega \text{ cm}^2$	$\Delta R_{on, sp}$, %	FOM, MW cm^{-2}	T_{max} , K	ΔT_{max}
Con SOI pLDMOS	153	88.9	1	286	82.3	0.082	331.3	19
NBL SOI pLDMOS	201	43.8	11	61.1	17.2	0.66	334.4	22.1
NBL PSOI pLDMOS	289	—	15.5	50.6	—	1.65	312.3	—

of the Si window (L_w) increases, the vertical electric field of the BOX reduces. At the same time, the substrate continues to participate in exhaustion and shares the BV, so the BV of the device is mainly shared by the BOX and substrate. When $L_w = 12 \mu\text{m}$, the vertical electric field and the vertical distance enclose the area to reach the maximum, that is, the BV reaches the maximum. When L_w is $>12 \mu\text{m}$, the ENDIF effect of the NBL becomes weaker so that the BV begins to decrease. The inset of Fig. 4a shows the vertical electric field distributions in the p-drift region at breakdown for the three devices. Fig. 4b shows the comparison of the vertical electric fields at the same Si window length ($L_w = 12 \mu\text{m}$) when T_n is different for the NBL PSOI pLDMOS.

According to the RESURF theory, the doping concentration of the NBL required for the device to reach the highest BV will decrease with the increasing of T_n . Moreover, the edge of the depletion layer in the n-well will be widened, which can be seen in the inset of Fig. 4b. As T_n increases, the fully depleted NBL provides the BOX with reduced ionised donors and the electric field of the BOX decreases continuously. In Fig. 4c, it is easy to understand there is only a double RESURF structure in the Con SOI pLDMOS, because it has only an n-top layer, not NBL. For the NBL SOI pLDMOS, the n-top layer, p-drift region, and NBL form a triple RESURF structure. Therefore, the vertical electric field has an extra electric field peak between the p-drift region and NBL, so that the vertical electric field is optimised. In addition, we can see in the inset of Fig. 4c that the electric field peak formed between the p-drift region and NBL of the NBL PSOI pLDMOS is higher than that of the NBL SOI pLDMOS.

As shown the inset of Fig. 4c, the position of the interface of the NBL and p-drift region at $x = 15 \mu\text{m}$ is set to 0 point. According to the Poisson equation, the electric field value reaches the maximum at 0 point. The maximum electric field value (E_{max}) can be expressed as

$$|E_{max}| = |E_{p\text{-drift}/n\text{-buried}}| = \frac{q}{\epsilon_s} N_n x_n = \frac{q}{\epsilon_s} P_d x_d \quad (1)$$

where $E_{p\text{-drift}/n\text{-buried}}$ is the peak of the electric field between the p-drift region and NBL; q is the charge density; ϵ_s is the dielectric coefficient of the Si layer; N_n is the doping concentration of the N region; P_d is the doping concentration of the P region; x_n is the width of the depletion region of the N region, and x_d is the depletion region width of the P region. Here, N_n denotes the doping concentration of the NBL; P_d denotes the doping concentration of the p-drift region; x_n is the width of the NBL depletion region; and x_d represents the depletion region width of the p-drift region. P_{d1} , x_{d1} , N_{n1} , and x_{n1} are the p-drift region concentration, p-drift region depletion region width, NBL concentration, and NBL depletion region width of the NBL SOI pLDMOS, respectively. Similarly, P_{d2} , x_{d2} , N_{n2} , and x_{n2} are the p-drift region concentration, p-drift region depletion region width, NBL concentration, and NBL depletion region width of the NBL PSOI pLDMOS, respectively.

It is clear that x_{n2} is larger than x_{n1} , x_{d2} is larger than x_{d1} , as shown in the inset of Fig. 4c. Moreover, we know N_{n2} is larger than N_{n1} , P_{d2} is larger than P_{d1} . According to (1), the peak value of the electric field can be obtained by integrating the region concentration and depletion region width. Therefore, it is easy to find that the electric field peak value $E_{p\text{-drift}/n\text{-buried}2}$ of the NBL PSOI pLDMOS is higher than the electric field peak value $E_{p\text{-drift}/n\text{-buried}1}$ of the NBL SOI pLDMOS.

Fig. 5a shows the distributions of the vertical potential for the three devices. The BV of the NBL PSOI pLDMOS is shared by the BOX and substrate. Whereas the substrate does not participate in the withstand voltage for the NBL SOI pLDMOS, because of no Si window, which results that the BV is almost sustained by the BOX and the BV is lower than that of the NBL PSOI pLDMOS. For the Con SOI pLDMOS, there are no Si window and NBL, so the substrate does not participate in depletion and no ENDIF effect for the BOX, which leads to a further reduction in the BV compared with the NBL PSOI pLDMOS. In the simulated results, for the NBL PSOI pLDMOS, as L_w increases, the BV increases. The BV increases to the optimal value of 289 V when $L_w = 12 \mu\text{m}$ and $T_n = 0.5 \mu\text{m}$. We can observe in Fig. 5b the potential decreases with the increasing of T_n at the same Si window length for the NBL PSOI pLDMOS.

Fig. 6 depicts the thermal characteristics of the three devices. The temperature of the bottom of the substrate is maintained at 300 K, and the gate voltage (V_g) is -15 V for all simulations. For the NBL SOI pLDMOS, due to the introduced NBL in the p-drift region and no Si window, the cross-sectional area of the drift region becomes narrow and the device thermal resistance increases. So that the maximum surface temperature (T_{max}) of the NBL SOI pLDMOS is slightly higher than that of the Con SOI pLDMOS when power consumption (P) is $1 \text{ mW}/\mu\text{m}$. However, the maximum surface temperature of the NBL PSOI pLDMOS is lower than that of the Con SOI and NBL SOI pLDMOS because of the presence of the Si window when P is $1 \text{ mW}/\mu\text{m}$. As L_w increases, the T_{max} of the NBL PSOI pLDMOS decreases, and the T_{max} is 312.3 K when L_w is $12 \mu\text{m}$.

The optimal values of the BV, $R_{on, sp}$, P_d , FOM, and T_{max} for the three devices are listed in Table 2. Compared to the Con SOI and NBL SOI pLDMOS, the NBL PSOI pLDMOS increases the BV by 88.9 and 43.8% and reduces the $R_{on, sp}$ by 82.3 and 17.2%. Moreover, it exhibits the higher FOM value and lower T_{max} than those of the Con SOI and NBL SOI pLDMOS.

4. Conclusion: A triple RESURF structure in the novel NBL PSOI pLDMOS modulates the electric field distribution and an Si window below the drain reduces the device surface temperature. A higher BV is obtained for the NBL PSOI pLDMOS compared with the NBL SOI pLDMOS. Meanwhile, the NBL assists in depletion of the drift region to increase the drift region concentration, resulting in a lower $R_{on, sp}$. Finally, the NBL PSOI pLDMOS achieves a higher BV of 289 V with the drift region length (L_d) of $20 \mu\text{m}$ and the BOX thickness (T_{BOX}) of $1 \mu\text{m}$. Compared to the Con SOI and NBL SOI pLDMOS, the BV is increased by 88.9 and 43.8%, respectively. Moreover, the $R_{on, sp}$ is lower than that of them. The figure of merit (FOM = $BV^2/R_{on, sp}$) is 1.65 MW cm^{-2} . Furthermore, a lower T_{max} of 312.3 K at $P = 1 \text{ mW}/\mu\text{m}$ is obtained.

5. Acknowledgment: This work was supported by the National Natural Science Foundation of China (grant no. 61306094).

6 References

- [1] Podgaynaya A., Rudolf R., Pogany D., *ET AL.*: 'Experimental and theoretical analyses of the electrical SOA of rugged p-channel LDMOS', *IEEE Electron Device Lett.*, 2010, **31**, (12), pp. 1440–1442

- [2] Zhou K., Luo X.R., Xu Q., *ET AL.*: 'A RESURF-enhanced p-channel trench SOI LDMOS with ultralow specific on-resistance', *IEEE Trans. Electron Devices*, 2014, **61**, (7), pp. 2466–2472
- [3] Luo X.R., Tan Q., Wei J., *ET AL.*: 'Ultralow ON-resistance high-voltage p-channel LDMOS with an accumulation-effect extended gate', *IEEE Trans. Electron Devices*, 2016, **63**, (6), pp. 2614–2619
- [4] Appels J.A., Vaes H.M.J.: 'High voltage thin layer devices (RESURF devices)'. Proc. IEDM, Washington, DC, USA, December 1979, vol. **25**, pp. 238–241
- [5] Qiao M., Wang Y.R., Zhou X., *ET AL.*: 'Analytical modeling for a novel triple RESURF LDMOS with N-top layer', *IEEE Trans. Electron Devices*, 2016, **62**, (9), pp. 2933–2939
- [6] Xiang F., Wang Z., Wen H.J., *ET AL.*: 'A novel triple RESURF LDMOS with partial N⁺ buried layer'. Proc. IEEE ICSICT, Xi'an, China, 2012, pp. 1–3
- [7] Qiao M., Li Y.F., Zhou X., *ET AL.*: 'A 700 V junction-isolated triple RESURF LDMOS with N-type top layer', *IEEE Electron Device Lett.*, 2014, **35**, (7), pp. 774–776
- [8] Wang Z., Lu M.T., Zhou X., *ET AL.*: 'A novel triple-RESURF SON LDMOS and its analytical model'. Proc. IEEE EDSSC, Chengdu, China, 2014, pp. 1–2
- [9] Wu L.J., Hu S.D., Zhang B., *ET AL.*: 'A new SOI high voltage device based on E-SIMOX substrate', *J. Semicond.*, 2010, **31**, (4), p. 044008
- [10] Hu Y., Wang H., Du C.X., *ET AL.*: 'A high-voltage (>600 V) N-island LDMOS with step-doped drift region in partial SOI technology', *IEEE Trans. Electron Devices*, 2016, **63**, (5), pp. 1969–1976
- [11] Zhang B., Li Z.J., Hu S.D., *ET AL.*: 'Field enhancement for dielectric layer of high-voltage devices on silicon on insulator', *IEEE Trans. Electron Devices*, 2009, **56**, (10), pp. 2327–2334
- [12] Wu L.J., Hu S.D., Zhang B., *ET AL.*: 'Partial-SOI high voltage P-channel LDMOS with interface accumulation holes', *Chin. Phys. B*, 2011, **20**, (10), p. 107101
- [13] Park J.M., Grasser T., Kosina H., *ET AL.*: 'A numerical study of partial-SOI LDMOSFETs', *Solid-State Electron.*, 2003, **47**, (2), pp. 275–281
- [14] Hu Y., Huang Q.J., Wang G.F., *ET AL.*: 'A novel high-voltage (>600 V) LDMOSFET with buried N-layer in partial SOI technology', *IEEE Trans. Electron Devices*, 2012, **59**, (4), pp. 1131–1136