Analysis of trap-assisted tunnelling in asymmetrical underlap 3D-cylindrical GAA-TFET based on hetero-spacer engineering for improved device reliability

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Published in Micro & Nano Letters; Received on 6th May 2017; Revised on 19th June 2017; Accepted on 4th July 2017

A unique design for an asymmetrical underlap (AU) cylindrical-gate-all-around (GAA)-*n*-tunnel field effect transistor (TFET) based on hetero-spacer engineering with trap-assisted tunnelling (TAT) for reliability concern is proposed and validated. Here, DC and analogue performances such as I_{ON}, I_{OFF}, SS, $I_{ON}/I_{OFF,}$ C_{gs}, and C_{gd} have been investigated, while included TAT model and compared the examined device with AU GAA-TFET based on homo-spacer (HS) dielectric. On the basis of observation, the proposed device increases ON current as high as 2.1×10^{-6} A/μm, which corresponds to 1024 times improvement in I_{ON}/I_{OFF} when compared with device based on HS. It also suppresses ambipolar behaviour with fast switching ON–OFF transition due to low leakage current (I_{OFF}). These performances are mainly produced due to AU and low-*k* spacer dielectric which is replaced by high-*k* dielectric over source side spacer of the device, whereas drain side spacer is placed with high-*k* material along with increase in series resistance across drain–channel junction caused by drain underlap. Low-*k* spacer reduces the fringing field, and the depletion does not form at the source–gate edge, hence high source–channel tunnelling junction.

1. Introduction: Very large-scale integration applications of nanotechnology while scaling semiconductor devices continuously follow Moore's law in order to achieve high speed, high density, and low-power consumption. However, due to nanoregime scaling, short channel effects (SCEs) are the major factor to deteriorate the device performance for low-power applications. Hence, supply voltage (V_{DD}), threshold voltage (V_{th}), and OFF voltage (V_{OFF}) must be reduced and simultaneously overdrive factor (V_{DD}–V_{OFF}) must be high to meet the best device performance. Furthermore, the subthreshold slope (SS) of the conventional metal–oxide–semiconductor field effect transistor (MOSFET) is limited to 60 mV/decade ($SS = (kT/q) \times \ln 10$) at room temperature governed by thermionic emission over a thermal barrier. Thus, the devices based on the inter-band tunnelling (BT) are the most demanding device over conventional MOSFET for indirect-bandgap material such as silicon (Si) [1, 2]. In this regard, one of the novel device design that excited a lot of research interest for low-power dissipation is the tunnel FET (TFET). This is because the SS of the TFET is not limited to 60 mV/dec at room temperature when compared with the conventional MOSFET. It is based on an unconventional current mechanism of BTBT. Here, BTBT means flow of drain current in *n*-channel-TFET occurs due to tunnelling of charge carriers from valence band of the source to the conduction band of the channel region. Also here, transport of charge carriers are assumed to be ballistic, which can enhance the operating speed. Here, ballistic movement in TFET represents flow of charge carriers in a well-mannered path without mutual scattering between them. Therefore, it exhibits the extraordinary properties of high immunity to SCEs, low leakage (OFF state) current, and low subthreshold swing [2–6].

TFET is basically a gated voltage transistor working under reverse bias at low voltage (< 1 V). For TFET, International Technology Roadmap for Semiconductors-2018 targets for low power of 0.57 V, which is most important for low dynamic power of circuits and low-power module of system-on-chip applications [7]. However, these transistors have some limitations such as low ON current (I_{ON}) and severe ambipolar characteristics. This is due to BTBT at both source–channel and drain–channel junctions. The I_{ON} of the TFET is varying with the variation in the BTBT probability (T_{WKB}), which is defined by the Wentzel–Kramers–Brillouin (WKB) approximation

$$I_{ON} \propto \simeq \exp\left(\frac{-4\lambda\sqrt{2m^*}\sqrt[3]{E_g}}{3q\hbar\left(E_g + \Delta\emptyset\right)}\right) \quad (1)$$

Here, λ is the geometrical dependent tunnelling length and m^* is the effective carrier mass. E_g is the energy bandgap, q is the electron charge carrier, and $\Delta\emptyset$ represents energy difference between the valence band of the source and the conduction band of the channel. WKB current equation suggests that an improvement in I_{ON} can be made by reducing λ, m^*, and E_g [8].

In this phenomenon, many researchers have worked on different structures, e.g. Boucart and Ionescu [9] reported double-gate TFET with high-*k* gate dielectric to achieve volume inversion and fringing field effect. In [10], Lee *et al.* studied and predicted that hetero-gate dielectric plays an important role for improved device performance. Although, they were not analysed the effects of hetero-spacer (HTS) on the device performance. In addition to this Anghel *et al.* [11] and Chattopadhyay *et al.* [12] analysed that low-*k* spacer with high-*k* gate dielectric are responsible to enhance ON current. However, above structures are based on planar configuration. This limits channel length to 40 nm in further scaling of their devices due to SCEs such as drain-induced barrier lowering, subthreshold leakage, and power dissipation [13, 14]. It can be also getting suffered from hot carrier effects. TFETs have high electric field in the channel especially in the tunnelling region at the source end due to enhanced source side electric fields than conventional MOSFET. In addition, low E_g materials are studied and presented by Kim *et al.* [15], where authors proposed germanium-based source. Moreover, it causes high leakage current known as OFF state current (I_{OFF}) due to their large intrinsic charge carrier concentration. Hence, low ON current and ambipolar behaviour are the two major hurdles in the device performance for low-power applications.

In this regard, few recent works studied and implemented with gate-all-around (GAA)-based structures. Motivated by its property of low screening length, volume inversion, and enhanced electrostatic control of the gate over the channel. Since for GAA structure,

doi: 10.1049/mnl.2017.0311

gate is wrapped around all sides of the channel. In this concern, in [8], Jhan *et al.* reported nanowire TFET with high I_{ON}. Lee *et al.*, in another work predicted that drain underlap (DU) on GAA-TFET improves the I_{OFF}. However, authors also found that when channel length (L_{ch}) scales below 40 nm, it causes gradual decrease in I_{ON} with increase in I_{OFF} and thus leads to the degradation of I_{ON}/I_{OFF} with adversely high subthreshold swing [16]. We have also reported in [17], a detail investigation on three structures of cylindrical (Cyl)-GAA-TFET based on spacer engineering. Although, we have not examined the considered device for trap-assisted tunnelling (TAT) model, which are analysed and investigated in this work.

Previously, most of the simulated work has been studied and presented while assuming ideal direct tunnelling for semiconductor body without any defects. Thus, not adequately explained and considered non-idealities behaviour within the semiconductor body. Note that during the device fabrication, it induces phonons and radiation that damage the results in conception of interface defects AT causes reduction in device reliability and lifetime [18–20]. Thus, large disparity was observed between experimental and simulation results and the device reliability issue becomes a major concern. In this Letter, we report for the first time Cyl-GAA-TFET based on HTS engineering with asymmetry in underlap, while incorporating TAT physical model during three-dimensional (3D) simulation. This is because it includes experimental non-idealities such as defects and phonons on tunnelling zone using trap analysis of charge carriers. To calibrate the models, the GAA-TFET has been designed with the same device parameters as shown in experimental work of [19]. In our proposed device, asymmetrical underlap means drain underlap only and the HTS dielectric comprises different spacer dielectric at the drain and source sides, i.e. low-k spacer is placed over source side of the gate and high-k spacer is placed across drain side to improve the fringing field across the surface. Here, we investigate the device performance in terms of DC and AC characteristics such as I_{ON}, I_{OFF}, SS, and I_{ON}/I_{OFF} with associated gate–source (C_{gs}) and gate–drain capacitance (C_{gd}). All the capacitances are extracted from the small-signal AC simulations at a moderate frequency of 1 MHz. The proposed channel length is considered as 25 nm. The proposed device also supports for fabrication by reducing the complexity of process of fabrication. This is because of its structure having all-around Cyl symmetry across the source, drain, and channel. Hence, it can be easily processed when compared with other existing GAA structures of [4, 8, 10].

The rest of this Letter is organised as follows. Section 2 provides the structure, design parameters, and models used for simulation. The effect of HTS on the performance characteristics of the examined 3D GAA-TFET with trap-assistant tunnelling is provided in Section 3. Finally, the conclusions are presented in Section 4.

2. Device structure and design parameters: Spacers are basically insulator required for isolation to prevent carrier leakage over gate edge. The device structures along with various device parameters are shown in Figs. 1*a* and *b*. It shows the cross-sectional and 3D view of DU Cyl-GAA-*n*TFET with HTS. Here, DU means drain underlap only, while HTS means low-k spacer dielectric (Si dioxide) is placed over source region and high-K spacer (HfO_2) over drain region. To evaluate the merits of the proposed HTS-based GAA-TFET, it has been compared with the homo-spacer (HS) dielectric of GAA-TFET with the same device geometry. Here in HS, high-k spacer dielectrics (HfO_2) are placed over both sides of the gate, i.e. source and drain. For fair comparisons, we have used the same geometrical structure and device parameters such as gate work function, doping concentrations, and gate dielectric with the same gate–source voltage (V_{GS}) scale for both the structures. The threshold voltage (V_T) is extracted using constant current method (10^{-9} A/μm).

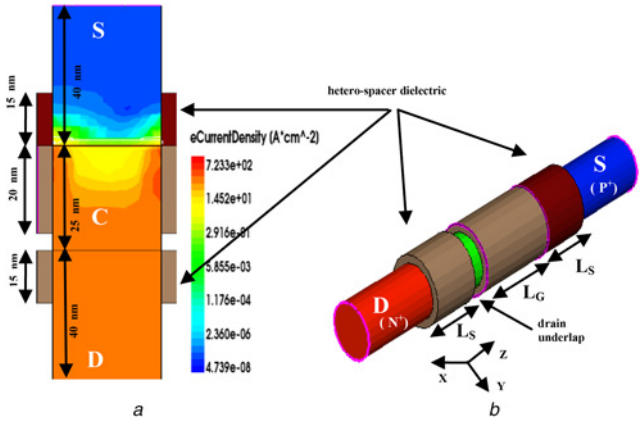

Fig. 1 *Device structures along with various device parameters*
a Cross-sectional view
b 3D view of DU-Cyl-GAA-TFET with HTS along channel length direction with magnitude of electron (e) current density. Here, S – source, D – drain, and C – channel, gate length (L_G) = 20 nm, spacer width (L_S) = 15 nm, oxide thickness (t_{ox}) = 2 nm, and thickness of high-k dielectric (t_{HfO_2}) = 2 nm are used

The average SS (SS_{AVG}) is calculated as

$$SS_{AVG} = \frac{(V_T - V_{OFF})}{\log(I_{V_T}) - \log(I_{V_{OFF}})} \quad (2)$$

Here, V_{OFF} is the gate–source voltage from which the drain current starts to take off (source–channel tunnelling), I_{V_T} is the drain current of the device at $V_{GS} = V_T$, and $I_{V_{OFF}}$ is the drain current at $V_{GS} = V_{OFF}$ [21].

The physical models comprising the device simulations based on BTBT are Kane's model, Schenk model, Hurkx BTBT model, and the dynamic non-local BTBT model. Here, non-local TAT model and non-local BTBT model was used with field-dependent mobility, and bandgap narrowing model performed using Synopsys Sentaurus Technology computer aided design (TCAD) tool at 300 K [22].

However, TAT model included effects of trap charges, i.e. band tails, defect AT. It may exist during fabrication process such as heavy doping and phonons. Hence, it also contributes to slightly larger SS. Although the given effects are minimised when compared with improved DC/analogue characteristics achieved in DU GAA-HTS. Note that dynamic non-local model offers the possibility to use three tunnelling paths such as TAT, direct tunnelling path, and non-local TAT model. In all the cases, default parameters for Si are used in order to achieve high thermal stability and consistency. This is because Si act as a masking layer to prevent the diffusion of the dopants in the region it protects. When adding the TAT model to the physics of the simulation, a tail at lower gate voltage appears due to the dominant TAT component at low electric field [23–26].

In this case, when the TAT model is included, the simulations are much closer to the experimental data. To calibrate the non-local BTBT model, mass of electron (m_e) and mass of hole (m_h) for Si are taken as 0.24 and 0.34, respectively. $A_{path} = A = 4 \times 10^{14}$ cm^{-3} s^{-1} and $B_{path} = B = 1.9 \times 10^7$ V cm^{-1}, where A and B are material dependent parameters. The values of other parameters for the non-local model are kept to their default value as projected for Si. Since the tunnelling process is non-local; therefore, the mesh was carefully refined in the applied zone, where tunnelling can take place in order to assure both convergence and correct simulation of the device. Asymmetrical doping profiles are used for all regions to make abrupt junction. P-type source (1×10^{20} cm^{-3}),

N-type drain (1×10^{18} cm^{-3}), and P-type channel region (5×10^{17} cm^{-3}) as shown in Fig. 1*b*. Owing to the increased oxide capacitance, HfO_2 is used as a gate dielectric ($k = 21$) with gate work function = 4.53 eV and thickness of high-k dielectric (t_{HfO_2}) = 2 nm are used.

3. Results and discussion: In GAA structures, gate is wrapped around all sides over the channel, which may contribute depletion of the source/drain toward gate. Thus, spacer engineering plays an important role to prevent carrier leakage over gate edge. Fig. 2 shows the comparison of the transfer characteristics of n-channel DU GAA-TFETs with varying spacer dielectric. The ON current (I_{ON}) and I_{ON}/I_{OFF} for DU GAA-TFET with HTS are 6 and 1024 times when compared with HS dielectric at $V_{GS} = 1.5$ V. The experimental results are also studied and found that I_{ON} and I_{ON}/I_{OFF} for GAA-HTS are 7 and 83× times when compared with [27]. Also, low gate–drain capacitance of 1.75 fF can be extracted using AC simulation with low subthreshold swing of 52 mV/decade as shown in Table 1. Fig. 3*a* shows the OFF state operation of TFET, where no BTBT occurs, since the potential barrier exists between the source and the channel, whereas during ON state, the gate voltage pulls down the energy band of the channel region and width of the tunnelling barrier reduces. Therefore, charge carriers can tunnel from the valence band of the source to the conduction band of the channel region as shown in Fig. 3*b*. This optimised result is obtained due to the implementation of HTS, i.e. low-k spacer placed at the source side, which reduces the fringing fields, and the depletion zone does not form at the source–gate edge. Hence, the suppression of the depletion zone results in the high source–channel tunnelling

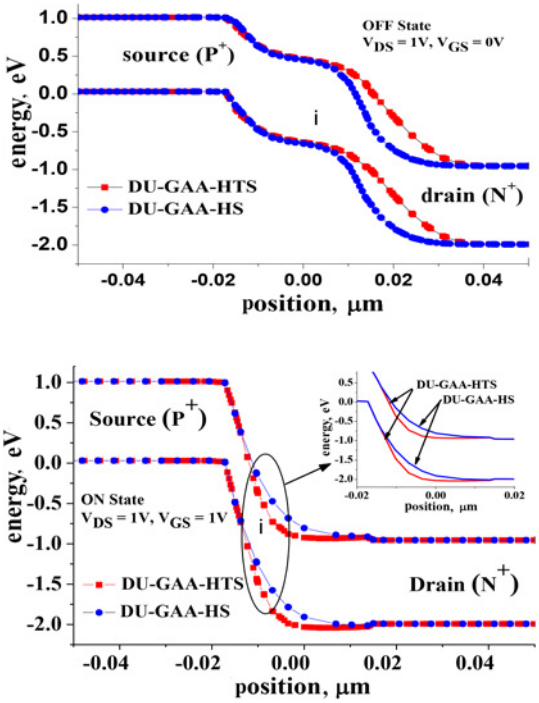

Fig. 3 *Comparison of energy band diagram for DU Cyl-GAA with HTS and HS dielectric in the case of*
a OFF state
b ON state. The inset shows the position of band bending between the valence band of the source and conduction band of the channel during tunnelling of charge carriers

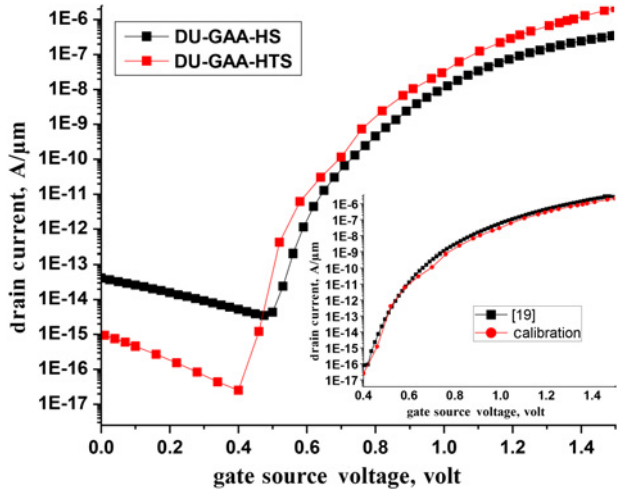

Fig. 2 *Transfer characteristics of DU GAA-TFET with HTS and HS dielectric at $V_G = 1.5$ V. The effective channel length is 25 nm. The inset shows the calibration of our simulation result with [19]*

Table 1 Comparison of device parameter values for DU GAA-TFET with HTS and HS dielectric

Parameters	DU GAA-HTS	DU GAA-HS	[27]
I_{ON}, A/μm	2.10×10^{-6}	3.50×10^{-7}	0.3×10^{-6}
I_{OFF}, A/μm	2.51×10^{-17}	4.32×10^{-15}	0.30×10^{-13}
I_{ON}/I_{OFF}	0.83×10^{11}	0.81×10^{8}	107
SS, mV/dec	52.6	55.9	90
C_{gd}, F	1.75×10^{-15}	6.15×10^{-15}	—
C_{gs}, F	0.48×10^{-15}	0.09×10^{-15}	—

at the device surface, and consequently, it increases the I_{ON} that flows through the device.

At the same time, DU compromises the channel resistance to be divided into gate resistance ($R_{with\text{-}gate}$) and without gate resistance of the channel region ($R_{without\text{-}gate}$). Therefore, an extension of the drain–channel region without gate occurs, which causes increase in $R_{without\text{-}gate}$ of the drain–channel region with decrease in $R_{with\text{-}gate}$. Hence, it enhances the gate controllability over the source–channel and causes variation in electron current density across the drain–channel length and depth [17, 28]. Specifically, we found that electric field by the gate voltage over the drain–channel region is gradually weakened, which has no effect on I_{ON}. Accordingly, it is observed that pushing of the gate end away from the drain junction reduces the tunnelling at the drain–channel junction. Therefore, low I_{OFF} with suppressed ambipolar behaviour and low subthreshold swing was achieved as shown in

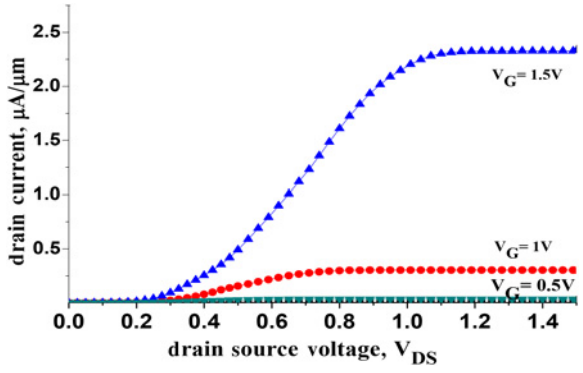

Fig. 4 *I_D–V_{DS} characteristic of DU GAA-TFET with HTS for different values of gate voltage while keeping source voltage (V_S) = 0*

doi: 10.1049/mnl.2017.0311

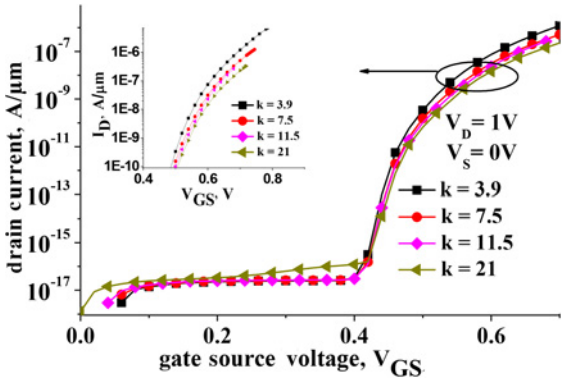

Fig. 5 *Transfer characteristic of DU GAA-nTFET for different values of the source–spacer dielectric on V_{GS} scale of 0.8 V. The inset shows the output characteristics in defined gate–source voltage of drain current for increase in value of source–spacer dielectric (k)*

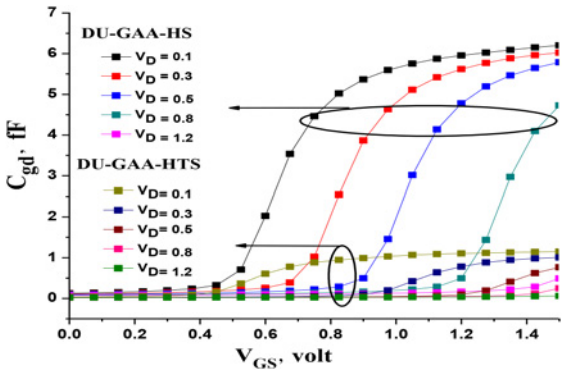

Fig. 6 *Comparison of gate-to-drain capacitance as a function of gate-to source voltage (V_{GS}) for different values of V_{DS} for both devices based on HTS and HS dielectrics*

Fig. 2. It may also be verified from the transfer characteristics in Fig. 4 that drain current (I_D) increases for a further increase in gate–source voltage (V_{GS}). Conclusively, it is observed that low source–spacer dielectric ($k = 3.9$) with DU causes less fringing field in the source near the gate edge. This is because of the non-depletion of the source toward gate side by low-k spacer as shown in Fig. 5. Significantly, it shows gradual fall in drain current (I_D) with increase in values of the source–spacer dielectric. Low-k spacer enhances the fringe field within the spacer as compared with that of high-k spacer dielectric placed across drain side. This phenomenon leads to carrier tunnelling at the surface only and not inside the body. As a consequence, it leads to high electric field occurring across source–channel junction with reduced ambipolar behaviour and gate–drain capacitance due to asymmetry in underlap-based structure.

Here, Figs. 6 and 7 analyse the gate–drain capacitance and gate–source capacitance, respectively, of both the devices for different values of drain voltage (V_D). C_{gd} is the Miller capacitance and in order to improve the TFET switching speed with low dynamic power, parasitic capacitances should be reduced. Now, $C_{gd} = C_{of} + C_{dif} + C_{dov} + C_{gd,inv}$ and $C_{gs} = C_{of} + C_{sif}$, where C_{of} is the outer fringing capacitance related to the fringing field effects between the gate electrode and the channel. C_{dov} is the drain overlap capacitance. C_{dif} and C_{sif} are the inner fringing capacitances at drain and source sides, respectively. Sometimes parasitic capacitances may vary due to charge variation in the channel close to source or drain. However, on varying the position of the drain body junction with respect to the gate edge, e.g. by controlling the drain dopant profile, C_{of} and C_{dov} can be adjusted [29]. It is observed that on

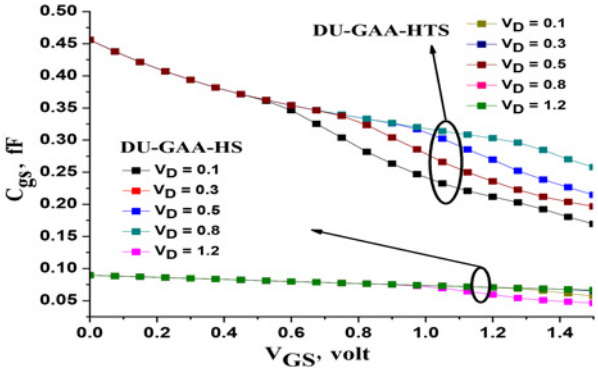

Fig. 7 *Comparison of gate-to source capacitance as a function of gate-to-source voltage (V_{GS}) for different values of V_{DS} on both the devices based on HTS and HS dielectrics*

increasing the value of gate-to-source voltage (V_{gs}). C_{gd} increases owing to the formation of inversion layer increases toward the source from drain below gate oxide for increasing value of drain voltage or in other terms due to reduction in channel to drain potential barrier, whereas C_{gs} in Fig. 7 drops slightly with increasing V_{gs}. The reason behind this being that the coupling reduces between the source and the gate due to the extension of the inversion layer and the presence of potential barrier. The forgoing observations are also in consistency with that reported in [30]. As a consequence, the proposed device consists of Si semiconductor produces low leakage current, low Miller capacitance (C_{gd}), which leads to abrupt control switching with concern of reliability and consistency. Thus, our device also satisfies the requirement of low-power applications with improved device reliability.

4. Conclusion: A systematic investigation of the impact of the underlap structure with HTS and HS dielectric on the device performance of a GAA-TFET has been made, whereas experimental non-idealities of real device fabrication have been analysed when included TAT model. Thus, it is found that the combination of DU with low-k spacer placed over source region reduces the fringing field within the spacer with increase in resistance of drain–channel junction produces the best device performance in terms of DC and AC characteristics with suppressed ambipolar behaviour, and abrupt ON–OFF transition. These performances are mainly achieved due to non-depletion of the source toward gate side and better gate controllability over the channel, which leads to source–channel tunnelling inside the surface instead of tunnelling toward the body influence by low spacer dielectric placed over source region. Hence, it can also be very attractive for low-power applications with reliability concern.

5. Acknowledgment: This work was supported by the Council of Scientific and Industrial Research (CSIR) funded Research Project, grant no. 22/0651/14/EMR-II, Government of India.

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