Deep insight into linearity and NQS parameters of tunnel FET with emphasis on lateral straggle

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Published in Micro & Nano Letters; Received on 19th May 2017; Revised on 14th July 2017; Accepted on 28th July 2017

Tunnel field-effect transistor (TFET) is considered to have superior device performance compared with DG-metal–oxide–semiconductor FET in terms of reduced off-state current and lower subthreshold swing. However, performance of a device solely depends on the accuracy in the fabrication process. This work presents a systematic methodology in small-signal-radio-frequency (RF) and linearity domain to analyse the effect of variation in lateral straggle caused by the variation tilt angle during ion implantation process. From previously published researches, it is intuitively established fact that the accurate evaluation of intrinsic components and estimation of linearity in short channel devices is crucial to access the range of application of the device. In this work, the authors have investigated the RF intrinsic parameter performances of a silicon double gate TFET having variation in lateral straggle from 1 to 5 nm. This study includes the analysis of non-quasi-static RF bias-dependent parameters such as intrinsic capacitances (C_{gs}, C_{gd}), gate-to-drain intrinsic resistance (R_{gd}) and intrinsic time delay (τ). Similarly, the device linearity and reliability are investigated here in terms of higher-order transconductances (g_{m2} and g_{m3}), VIP_2, VIP_3, IMD_3, IIP_3 and 1 dB *compression point.*

1. Introduction: For the advanced low-power electronics industry, silicon-based metal–oxide–semiconductor FET (MOSFET) has been proved to be a substantially successful technological driver. To accomplish low-power performance, modern complementary MOS (CMOS) devices must have substantially low semiconductor technology node. However, continuous physical scaling leads to increased levels of standby power via short channel effects etc [1–3]. In this scenario, innovative device architectures have paved the way for exploration of more advancement of low-power industry.

Recently, tunnel FETs (TFETs) have drawn significant interests due to its potentiality to have subthreshold slope below 60 mV/dec [4]. In addition, TFETs, driven by band-to-band tunnelling mechanism [5–7], turn out to offer significantly low off-currents compared with MOSFET [8]. Moreover, TFET exploring structural symmetry with MOSFET has established itself to be potentially sound for radio-frequency (RF) applications [2].

During fabrication process of MOS devices, ion implantation has become the dominating doping technique to implant dopant in source and drain regions [9]. A non-zero tilt avoids the channelling effects in crystalline silicon [10]. Conversely, tilt causes extension of source/drain region into the channel. This effect of tilt angle is realised using Gaussian profile at the channel–source/drain junction. Gaussian profile at source/drain region is realised with the expression $N_{sd}(x) = N_{peak}\exp(-x^2/\sigma^2)$ [11], where σ is the fluctuation of ion beam direction and N_{peak} is peak doping concentration at the source/drain to channel junction. Here, lateral straggle parameter σ along the channel (in the direction of x) is varied from 1 to 5 nm in order to investigate the effect in RF and linearity domain.

It is evident that gradual source/drain junction reduces the effective channel length [12] of the device. Thus, the improvement in device on current is obtained. However, increase in lateral straggle parameter would affect the off-state current and thereby subthreshold swing. Apart from this, increasing lateral straggle induces large gate-to-source/drain overlap region [12]. It is established fact that overlap region has strong implications on overlap capacitance which in turn responsible for the switching response of the device. Therefore, the study of the impact of lateral straggle on the RF performance plays a crucial role.

It is established earlier that lateral straggle affects severely on the device performance in analogue domain [13]. In this Letter, we have analysed for the first time the effect of lateral straggle on the bias-dependent capacitance and resistance terms from small-signal measurements of TFET in detail.

Moreover, non-linear behaviour of a device is becoming stringent for future RF applications [14–16]. Since, device analogue performance is observed to have immense sensitivity for the variation lateral straggle [13], linearity figure-of-merits (FOMs) need to be emphasised in light of lateral straggle parameter. In this work, the linearity and intermodulation distortion performance due to variation in lateral straggle in TFET is investigated in TFET in terms g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, IMD_3 and 1 dB compression point.

This work is organised in the following sections. The device structure and the simulation methodology for this work are explained in Section 2. In Section 3, the detailed analysis of non-quasi-static (NQS) RF parameters are described followed by thorough discussion of linearity related FOMs in Section 4. Finally, the conclusion of this Letter is presented in Section 5.

2. Device structure and simulation: The device structure of DG-TFET studied in this work is presented in Fig. 1. Moreover, the detail descriptions of the device structure are listed in Table 1.

The doping profile along the channel below the gate is plotted in Fig. 2. Fig. 2 shows the Gaussian doping profiles with a peak density of 10^{20} cm^{-3} at the source region and 5×10^{18} cm^{-3} at the drain region, with the doping gradients of 1, 3, 5 nm/dec.

All simulations have been performed in Sentaurus TCAD device simulator [17]. Prior to simulations, simulation model parameters are calibrated with experimental result [18]. A constant temperature of 300 K has been employed by default during simulations. In this work, doping-dependent Masetti mobility model is opted to incorporate the effect of impurity scattering. Along with concentration-dependent recombination model for carrier transport is also considered. Furthermore, field-dependent mobility is introduced for accuracy of the results. In addition, we have employed non-local tunnelling process accompanying with bandgap

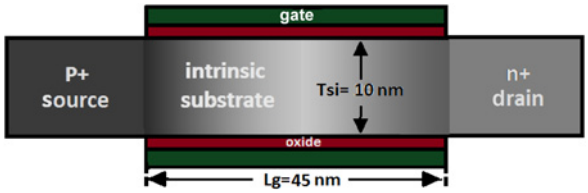

Fig. 1 *Cross-sectional view of DG-nTFET with lateral straggle at source/drain*

Table 1 Values for parameters

Parameters	Values
p^+ source doping, N_s	1×10^{20} cm^{-3}
N body doping, N_{ch}	1×10^{17} cm^{-3}
n^+ drain doping, N_d	5×10^{18} cm^{-3}
oxide thickness (t_{ox})	1.1 nm
gate material	molybdenum
gate length, L_g	45 nm
body thickness, T_{si}	10 nm

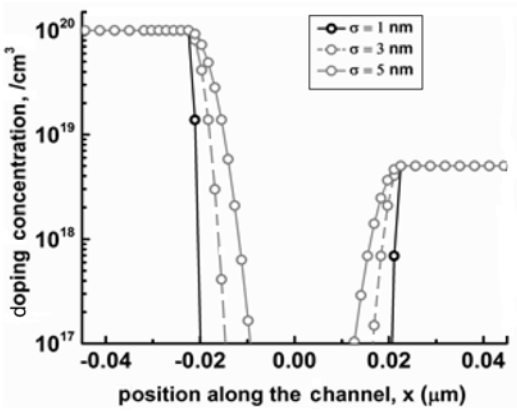

Fig. 2 *Doping concentration of DG-nTFET having increasing lateral straggle parameter values of 1, 3 and 5 nm*

narrowing model at the tunnelling junctions to capture the effects of spatial profile of the energy.

The supply voltage (V_{DD}) used for the work is 1.0 V. To compute the values of RF performance parameters, V_{ds} and V_{gs} are maintained to be fixed at values of 1 V and 1.4 V, respectively.

Usually, analytical modelling is used for linearity analysis**.** However, the use of physics-based device simulation provides an alternative approach of widespread comparative linearity analysis by analysing the trends of graphs and profiles etc., in much quicker and easier way compared with the analytical model.

For fair comparison among all the devices with various lateral straggle parameters, linearity FOMS are analysed as a function of gate overdrive voltage (V_{GT}). V_{GT} is expressed as ($V_{gs}-V_T$), where V_T is the threshold voltage, defined as voltage at $I_{ds}=10^{-7}$ A/μm and $V_{ds}=1$ V.

3. NQS performance discussion: NQS effect, a relaxation-time-dependent phenomenon in MOS devices is defined as the response of channel charges in the presence of a time-varying input signal. In this section, we have elaborately discussed the effect of lateral straggle on bias-dependent NQS-RF parameters in DG-TFET. In Fig. 3, the small-signal equivalent circuit of conventional TFET is shown. It contains the bias-independent extrinsic components and bias-dependent intrinsic components.

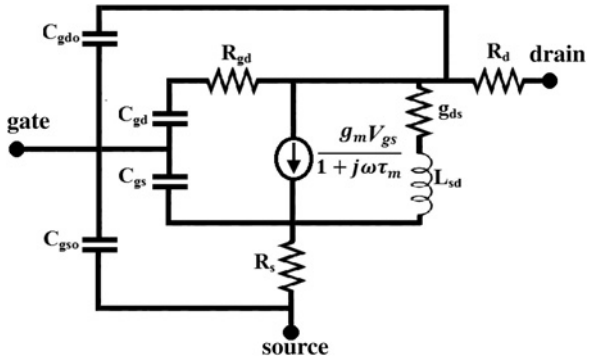

Fig. 3 *Small-signal equivalent circuit of conventional TFET*

The extrinsic part of a device is liable for parasitic effects which may affect the overall device performance. TFET contains extrinsic components such as gate-to-source capacitance (C_{gso}), gate-to-drain capacitance (C_{gdo}), source resistance (R_S) and drain resistance (R_D). The extrinsic capacitances constitute of three major components inner fringing capacitance, outer fringing capacitance and overlap capacitance. It is evident that with the increasing value of lateral straggle fringing capacitances remain constant. However, overlap capacitance increases consequently with the enhancement in lateral straggle parameter as gate-to-source/drain overlap increases. On the other hand, source and drain resistances solely depend on the material properties and area of source/drain region. Thus, with the increase in lateral straggle the values of R_S and R_D remain unaltered.

To obtain the bias-dependent intrinsic components, the extrinsic components need to be de-embedded from the small-signal equivalent circuit given in Fig. 3 following the process described in [19]. For that purpose, at first, the values of extrinsic components C_{gso}, C_{gdo}, R_S and R_D are extracted using the following expressions [20]. Y-parameter values in the expressions are obtained from ac simulation at zero bias condition

$$C_{gdo}=\frac{\mathrm{Im}(Y_{21})}{\omega} \tag{1}$$

$$C_{gso}=\frac{\mathrm{Im}(Y_{11})}{\omega}-C_{gdo} \tag{2}$$

$$R_S=\frac{\mathrm{Re}(Y_{11})+\mathrm{Re}(Y_{21})}{[\mathrm{Im}(Y_{11})+\mathrm{Im}(Y_{21})]^2} \tag{3}$$

$$R_d=-\frac{\mathrm{Re}(Y_{21})}{(\mathrm{Im}(Y_{21}))^2} \tag{4}$$

On the other hand, the bias-dependent intrinsic components are explained in terms of gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), gate-to-drain resistance (R_{gd}) and intrinsic time delay (τ). All the intrinsic parameters are also extracted by Y-parameter analysis. Thereafter, C_{gs}, C_{gd}, R_{gd} and τ are calculated with the expressions (5)–(8) from de-embedded Y parameters [21]

$$C_{gs}=\frac{\mathrm{Im}(Y_{11})+\mathrm{Im}(Y_{12})}{\omega} \tag{5}$$

$$C_{gd}=-\frac{\mathrm{Im}(Y_{12})}{\omega} \tag{6}$$

$$R_{gd}=-\frac{\mathrm{Re}(Y_{12})}{\omega^2 C_{gd}^2} \tag{7}$$

$$\tau=-\frac{1}{g_m}\left(\frac{\mathrm{Im}(Y_{21})}{\omega}+C_{gd}\right) \tag{8}$$

In the following discussion, for the variation in lateral straggle from 1 to 5 nm, the extracted C_{gs}, C_{gd}, R_{gd} and τ are analysed in detail.

doi: 10.1049/mnl.2017.0326

It is to be noted that the extraction of data are ranged up to 100 GHz as mentioned in [19].

Figs. 4 and 5 show the variations in C_{gs} and C_{gd}, respectively, as a function of frequency for the variation in lateral straggle. It is observed that with the increase in the value of lateral straggle, C_{gs} and C_{gd} increases. As with the increase in lateral straggle, the effective channel length of the device reduces; therefore, effective the lateral electric field (V/effective channel length) at $V_{ds} = 1.4$ V increases. Therefore, the number of carrier under gate increases readily. Thus, bias-dependent capacitances C_{gs} and C_{gd} enhance. Furthermore, as expected, the value of C_{gd} is higher than values of C_{gs} [22, 23].

Fig. 6 demonstrates the values of τ for TFET with different lateral straggles extracted at $V_{gs} = 1.4$ V and $V_{ds} = 1.0$ V. It is apparent from Fig. 6 that as lateral straggle increases from 1 to 5 nm the intrinsic time delay retards sequentially.

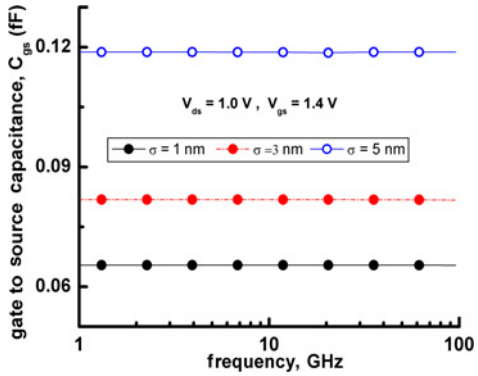

Fig. 4 *Variation of C_{gs} as a function of frequency for 45 nm TFET for various lateral straggles*

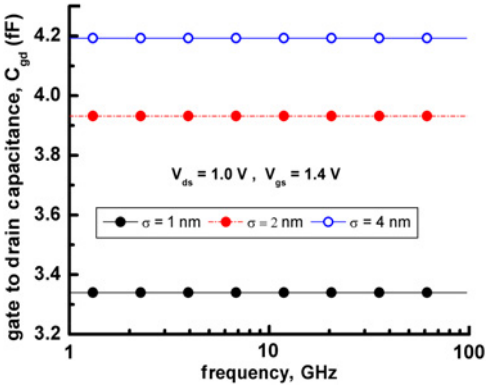

Fig. 5 *Variation of C_{gd} as a function of frequency for 45 nm TFET for various lateral straggles*

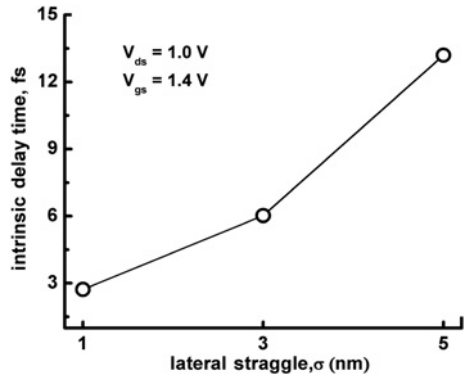

Fig. 6 *Variation in τ as a function of lateral straggle for 45 nm TFET at $V_{gs} = 1.4$ V and $V_{ds} = 1.0$ V*

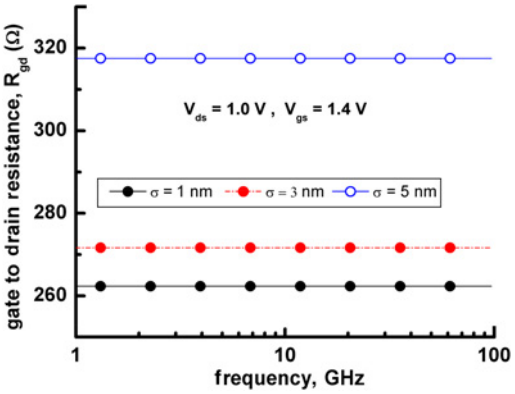

Fig. 7 *Variation of R_{gd} as a function of frequency for 45 nm TFET for various lateral straggles*

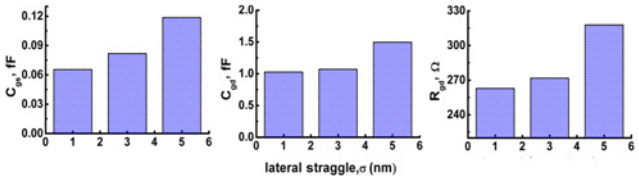

Fig. 8 *Bar graph of C_{gs}, C_{gd} and R_{gd} having increasing lateral straggle parameter. The values are extracted at bias condition of $V_{gs} = 1.4$ V, $V_{ds} = 1.0$ V and at frequency 11.8 GHz*

The sequential rise in τ can be explained in terms of device channel length and scattering. As explained earlier in Figs. 4 and 5, the number of carrier under gate increases with the increase in lateral straggle at constant bias condition; thus, the carrier scattering also increases and thereby, τ is degraded considerably at higher-lateral straggle.

In TFET, the distributed channel resistance is modelled by R_{gd}. With the increase in lateral straggles the transport delay of the channel increases. Thus, resistivity of the channel at drain end, defined by R_{gd} also shows increasing trend with increasing value of lateral straggle as shown in Fig. 7. As stated previously, the parameters of Figs. 4, 5 and 7 remain constant for the frequency range up to 100 GHz following the criteria of the model [19]. Thereby, the suitability of the device for RF application increases. In Fig. 8, bar graph of the parameters with respect to lateral straggle is also given for more clarity.

4. Linearity analysis: Linearity is the fundamental requirement for RF applications [14–16]. MOS devices with high linearity ensures distortion free output signal with minimal intermodulation and higher-order harmonics. Non-linearity is generally related to the higher-order transconductance, i.e. higher-order derivatives of the transfer characteristics (I–V) of a transistor. In this work, the metrics used to evaluate RF linearity are g_{m2}, g_{m3}, VIP_2, VIP_3, IMD_3, 1 dB compression point and IIP_3 [24, 25].

At first, we will discuss about the higher-order transconductance FOMs such as g_{m2}, g_{m3} which may interfere with fundamental frequency and results in non-linearity. To take into account such non-linearity, g_{m3} is considered to be dominant parameter compared with g_{m2}. Since, even-order harmonics in circuits can be eliminated with the help of balanced topologies, the impact ofg_{m2} is quite manageable to sustain high linearity. On the other hand, g_{m3} is highly uncontrollable, and hence determines the lower limits on distortion. Therefore, the amplitudes of g_{m2}, g_{m3} should be minimised as low as possible. g_{m2} and g_{m3} are given

by the following expressions [24]:

$$g_{m2} = \frac{\partial^2 I_{ds}}{\partial V_{gs}^2} \tag{9}$$

$$g_{m3} = \frac{\partial^3 I_{ds}}{\partial V_{gs}^3} \tag{10}$$

Figs. 9 and 10 show the variations in g_{m2} and g_{m3}, respectively, as a function of gate overdrive voltage, V_{GT} for various lateral straggles. It is observed from Figs. 9 and 10 that the amplitudes of g_{m2} and g_{m3} are higher for higher-lateral straggle parameter. Moreover, Fig. 10 shows that the value of V_{GT} at which g_{m3} crosses zero, denoted as zero-crossover point; increases with the increase in lateral straggle parameter. The shifting of zero-crossover point toward higher value of V_{GT} for higher-lateral straggle signifies that higher gate overdrive is required to maintain the linearity. The reason for degraded linearity at higher-lateral straggle is that the increasing lateral straggle generally decreases the effective channel length, which in turn reduces gate control of the device and deteriorates linearity performance.

VIP_2 and VIP_3 are further key metric associated with linearity and are given by [24–27]

$$V_{IP2} = 4 \times \frac{g_{m1}}{g_{m2}} \tag{11}$$

$$V_{IP3} = \sqrt{24 \times \frac{g_{m1}}{g_{m3}}} \tag{12}$$

Figs. 11 and 12 show the variations in VIP_2 andVIP_3 for various lateral straggles. It is evident from (11) and (12) that VIP_2 and VIP_3 are dependent on higher-order tranconductance parameters g_{m2} and g_{m3} which are dominant non-linear sources. Physically, VIP_2 signifies the point of extrapolated input voltage at which the values of first-order and second-order harmonic voltages are equal [24] and VIP_3 denotes the point of extrapolated input voltage at which the first-order harmonic voltage is equal to the third-order harmonic voltage [24]. It is discussed earlier in Figs. 9 and 10 that non-linearity of the higher-order transconductance FOMs should be minimised. Therefore, the values of VIP_2 and VIP_3 components need to be as high as possible to ensure distortion free output signal [28]. The peak point of VIP_3 curve implies the cancellation of third-order harmonics, and hence it should be high. It is evident from Fig. 12 that with decreasing lateral straggle, peak point positions of VIP_3 move from higher V_{GT} to lower, assuring more reliability via improved linearity at lower-lateral straggle.

Fig. 13 shows the variations of IMD_3, another FOM to determine the distortion performance of the device. IMD_3 is related to the non-linearity of static characteristics of device. IMD_3 is practically the extrapolated intermodulation current at which first-order harmonic power is equal to that of the third order [24]. To obtain better linearity IMD_3 must be as low as possible. IMD_3 is given by [28]

$$IMD_3 = \left(\frac{9}{2} \times (VIP_3)^3 \times g_{m3}\right)^2 \times R_S \tag{13}$$

where $R_s = 50\ \Omega$ is considered.

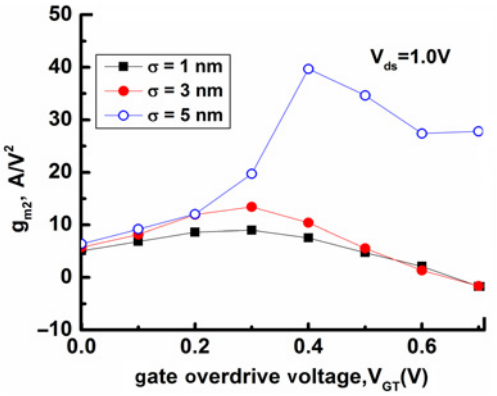

Fig. 9 *Variation in g_{m2} as a function of gate overdrive voltage for various lateral straggles for 45 nm TFET at $V_{ds} = 1.0$ V*

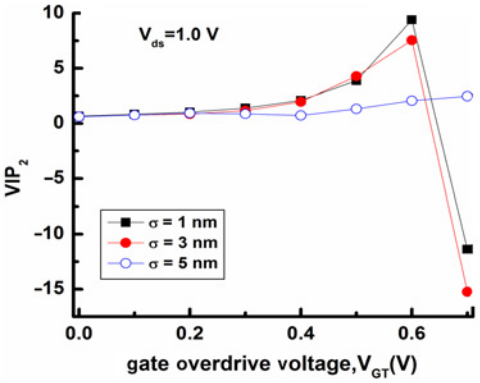

Fig. 11 *Variation in VIP_2 as a function of gate overdrive voltage for various lateral straggles for 45 nm TFET at $V_{ds} = 1.0$ V*

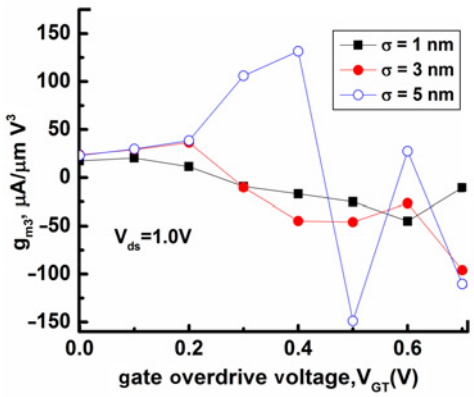

Fig. 10 *Variation in g_{m3} as a function of gate overdrive voltage for various lateral straggles for 45 nm TFET at $V_{ds} = 1.0$ V*

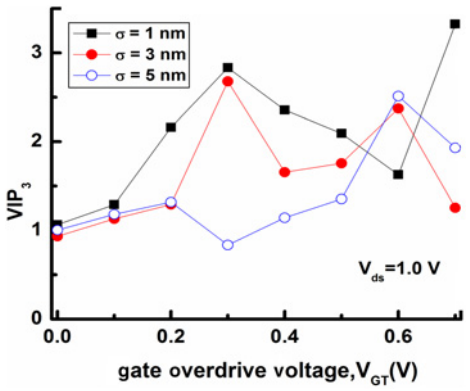

Fig. 12 *Variation in g_{m3} as a function of gate overdrive voltage for various lateral straggles for 45 nm TFET at $V_{ds} = 1.0$ V*

doi: 10.1049/mnl.2017.0326

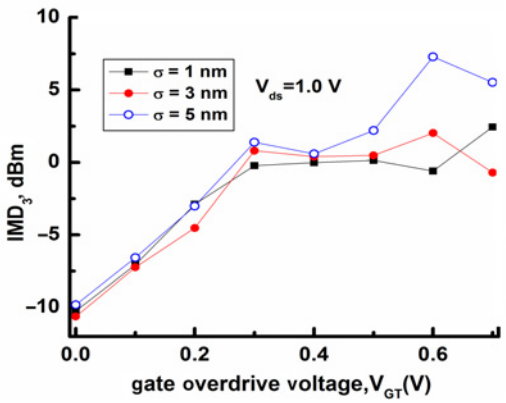

Fig. 13 *Variation in IMD_3 as a function of gate overdrive voltage for various lateral straggles for 45 nm TFET at $V_{ds} = 1.0$ V*

It is observed in Fig. 13 that a reduction in lateral straggle lowers the peak of IMD_3. The suppression of the harmonic distortion is due to the increase of the gate control over the channel via enhanced effective channel length at lower-lateral straggle.

In an amplifier, the plot of output power versus input power indicates the gain in terms of the slope of the curve. At some point of input power, the output power (i.e. gain) starts to decrease consistently and the amplifier goes into compression. The flatness of gain represents saturation condition of the device and its response becomes non-linear, produces signal distortion, harmonics etc. About 1 dB *compression point* of an amplifier is used to assess the device acceptability with respect to gain in the presence of distortion. It is defined as the point of input power at which the gain shifts from linearity by 1 dB. About 1 dB *compression point* is given by the following mathematical expression [24, 29]:

$$1\,\text{dB compression point} = 0.22 \times \sqrt{\frac{g_{m1}}{g_{m3}}} \tag{14}$$

Fig. 14 shows the variation in 1 dB *compression point* as a function of gate overdrive voltage for various lateral straggles at $V_{ds} = 1.0$ V. It is evident from Fig. 14 that 1 dB *compression point* decreases with the increase in lateral straggle. Results further reveal that reduced value of VIP_3 at higher-lateral straggle is mirrored in the degraded performance of 1 dB *compression point* at higher-lateral straggle.

IIP_3, another key parameter for linearity [16], is expressed in terms of the first- and third-order harmonics and is defined as

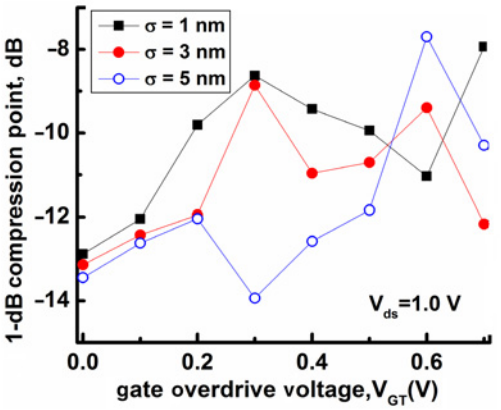

Fig. 14 *Variation in 1 dB compression point as a function of gate overdrive voltage for various lateral straggles for 45 nm TFET at $V_{ds} = 1.0$ V*

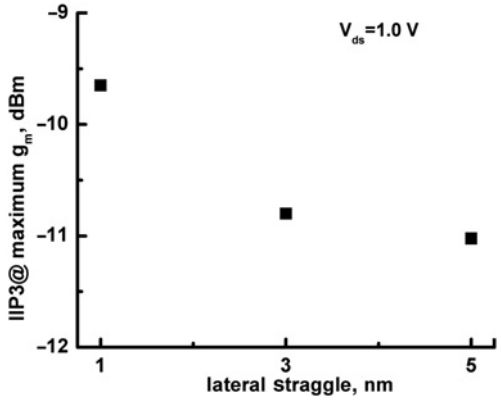

Fig. 15 *Variation in IIP_3 a function of gate overdrive voltage for various lateral straggles for 45 nm TFET at $V_{ds} = 1.0$ V*

[24, 30]

$$\text{IIP}_3 = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} R_s} \tag{15}$$

where $R_s = 50\ \Omega$.

Lower value of IIP_3 symbolises device non-linearity which is especially troublesome for RF systems. Fig. 15 presents the variation of IIP_3 with the variation of lateral straggle for TFET architecture. Furthermore, Fig. 15 clearly shows that IIP_3 is much lower for lateral straggle of 5 nm than for lateral straggle of 1 nm, pointing once again to the enhanced linearity characteristics of TFETs at lower-lateral straggle. Decreasing lateral straggle implies the enhanced gate control as explained previously in Fig. 13 and, thereby, an improved IIP_3 is obtained in TFET with low-lateral straggle parameter.

5. Conclusion: In this work, the effect of lateral straggle profile at the source/drain end of DG-TFET is presented in view of NQS-RF performance FOMs and linearity FOMs. It is observed that increasing lateral straggle degrades TFET performance in terms of C_{gs}, C_{gd} and R_{gd}. Furthermore, it turns out that the gradual variation in lateral straggle is also responsible for deteriorated intrinsic delay of a TFET structure. On the other hand, from linearity perspective, it is observed that all of the linearity FOMs including g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, IMD_3 and 1 dB compression point also get worsen at higher-lateral straggle. Therefore, it can be concluded from this Letter that the feasibility of higher-lateral straggle is not a way out at all to improve the RF FOMs and device reliability.

6. Acknowledgments: The authors thank the Council of Scientific and Industrial Research (CSIR), Government of India, Department of Science and Technology (DST), Government of India and All India Council for Technical Education (AICTE) for their financial assistance in carrying out research activities.

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doi: 10.1049/mnl.2017.0326