Junction-less charge plasma TFET with dual drain work functionality for suppressing ambipolar nature and improving radio-frequency performance

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This work deals with a distinct concept to realise the junction-less tunnel field effect transistor (JL TFET) by creating the plasma of charges. The crux of this study is to reduce ambipolar conduction and to improve high-frequency figure of merits. To construct a JL TFET, initially P^+ silicon film is considered and then metal electrodes are used to form drain and channel region. The drain electrode is separated into two sections and the work function of section adjacent to channel is selected higher than the other section. This provides a non-uniform doping profile in the drain region creating large barrier at the drain/channel junction to prevent the ambipolar conduction. Ambipolarity is reduced to 1×10^{-14} from 1×10^{-8} at $V_{gs} = -1.5$ V. The selection of work function and length of drain electrode adjunct to channel is crucial for optimising device performance. This optimisation provides information that work function >4.0 eV and length = 10 nm completely suppresses the ambipolarity which is around 1×10^{-21} with little degradation in ON-current. The high work function for the section of drain electrode adjunct to channel provides lower gate-to-drain capacitance (~2.67 fF) and superior high-frequency responses. Furthermore, performance assessment at circuit level is done by implementing primary digital circuits as inverter and NAND logic with lookup table based Verilog-A model.

1. Introduction: Tunnel field effect transistor (TFET) has shown its potentiality in semiconductor industry as an energy efficient device [1] due to its band-to-band tunnelling (BTBT) phenomenon, low operating voltage [2], low OFF-state current and subthreshold swing <60 mV/decade [3, 4]. However, TFET also suffers from lower ON-state current, ambipolar conduction (I_{ambi}) and poor radio-frequency (RF) performance which could be overcome by creating N^+ doped layer [5] at the source/channel junction and Gaussian drain doping profile [5]. The performance in terms of I_{ON} and RF parameters are enhanced with these methods at the cost of fabrication complexities and random dopant fluctuations. These methods are also not feasible for improving the performance of charge plasma (CP) and junction-less (JL) TFETs. Apart from this, the physical realisation of ultra-sharp doping profile in source/drain region in case of nanoscale devices is very complicated task and also expensive due to need of ion-implantation and thermal annealing techniques [6].

Pertinent to this, JL TFET where there is no doping concentration gradient and no junctions are studied widely in recent literatures [5, 6–11] to make the fabrication of device simpler while maintaining the advantages of TFET. In reported work [8], N^+ doped substrate is considered and later intrinsic channel region and P^+ source region are formed by creating plasma of charge carrier using appropriate work function metal contacts. This efficiently simplifies the fabrication process, but along with that, the formation of source region by work function engineering creates P^+ region near to surface and is not uniform throughout the source region which results in poor RF performance with parasitic conduction (ambipolar behaviour). For this purpose, we propose a device in which a new technique is adopted to form JL TFET from P^+ substrate instead of N^+ substrate which maintains uniform doping profile in the source region, provides abrupt source/channel interface and most importantly it follows the traditional P^+ substrate based complementary metal–oxide–semiconductor fabrication flow with their inherent advantages [12].

Practicing this technique for the formation of JL TFET from P^+ substrate provides opportunity to further use a distinct approach of dual drain work function engineering. Thus, the integrated effect produced by selection of P^+ substrate instead of N^+ substrate and dual work function at the drain electrode provides suppression in ambipolar nature and reduction in parasitic capacitance (C_{gd}). This results in overall performance improvement of the device in terms of creation of abrupt source/channel junction, better I_{ON} and improved RF figures of merit. It also resolves the issue related to presence of barrier between source and gate electrode in CP TFET (doping-less TFET) by its physically doped nature in source region which provides abrupt source/channel junction with enhanced ON-state current.

In this script, foremost focus is towards the suppression of ambipolarity and improvement in RF parameters to exercise the device in circuit level applications along with fabrication feasibility. Primary digital logic circuits such as inverter and NAND logics are implemented to assess the circuit-level performance by using lookup table based Verilog-A model of JL TFET. Comparison in terms of static noise margin (SNM) and noise margin high (NM_H), noise margin low (NM_L) propagation delay (τ_p), rise time (τ_r) and fall time (τ_f) are estimated in which all the results are better in case of dual drain work function JL TFET (DDW JL TFET) making it efficient for low-power circuit applications.

2. Device structure and simulation setup: Figs. 1*a* and *b* present the cross-sectional view of JL TFET with P^+ doped substrate and DDW JL TFET. The device in Fig. 1*b* differs from the device shown in Fig. 1*a* by the dual work functionality of drain metal contact. The parameters used in our simulation are: heavily doped P type silicon thin film with concentration 1×10^{19} cm^{-3}, body thickness (t_{Si}) 10 nm and HfO_2 is considered as gate dielectric material with 2 nm thickness (t_{OX}) [13, 14]. Length of drain (L_D), channel (L_{CH}) and source (L_S) regions are 55, 50 and 55 nm, respectively. The gate electrode is employed with work function (ϕ_{M1}) 4.5 eV [10] to create intrinsic region in channel, whereas drain electrode is employed with work function (ϕ_{M2}) 3.6 eV N^+ concentration in drain region. The spacing between the gate electrode ($M1$) and drain electrode ($M2/M3$) in JL TFET/DDW JL TFET is $L_{sp} = 5$ nm. However, the length (L_A) and

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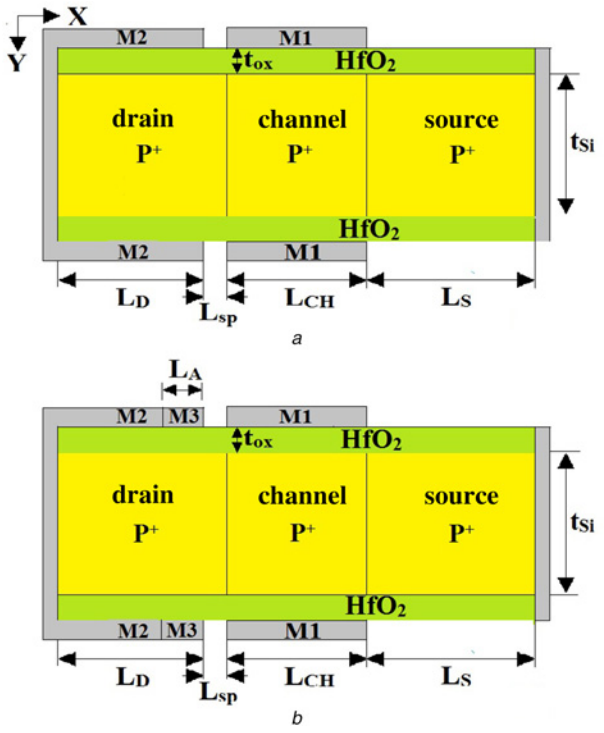

Fig. 1 *Cross-sectional view of*
a JL TFET
b DDW JL TFET

work function (ϕ_{M3}) of section $M3$ for creating non-uniform doping profile are taken as 10 nm and 4.0 eV, respectively.

As far as the practical realisation of the structure proposed, the fabrication of CP pn junction diode has been already demonstrated at the experimental level [15]. Hence, the proposed work may be considered as further extension of that fabricated CP pn junction diode. The following are the fabrication/design guidelines for the proposed device:

(i) First of all, the substrate is uniformly doped with acceptors (P+ dopants) as parent doping in the proposed device. Thereafter, N^+ and intrinsic regions are induced by the work-function difference between the metal gate used to form drain and channel regions, respectively.

(ii) Different metal electrodes are placed over the silicon (substrate) film to form the channel and the drain region. The metal electrodes and silicon film are separated by a dielectric layer of SiO_2 to avoid the silicide formation between silicon and metal [10, 16]. This also evades the fabrication complexity of the device.

(iii) The work function of metal electrode (cathode) to induce N^+ drain region should be kept less than that of intrinsic silicon ($\phi_{Md} < \chi_{Si} + E_g/2$) using CP concept [15] where χ_{Si} is electron affinity of bulk silicon and E_g is band gap of bulk silicon. However, the work function of gate electrode to form intrinsic region is kept 4.5 eV [10] and the source region is retained with its P^+ parent substrate. Thus, a typical TFET is formed by CP concept. Moreover, to fulfil the requirement of CP concept the thickness of silicon film must be less than Debye length, i.e. $L_D = \sqrt{(\chi_{Si}.u_T)/(q.N)}$, where χ_{Si} is the dielectric constant of silicon, u_T is the thermal voltage and N is the carrier concentration of the body [15].

(iv) This concept of creating plasma of charges beneath the respective metal electrodes does not need ion implantation and expensive thermal annealing technique which reduces the cost and provides practical feasibility in the device.

(v) Placing metal electrode over the drain also provides opportunity for formation of dual work functionality over the drain region for suppression of ambipolar behaviour of the device and improving RF performance. The advancement in nanolithography offers integration of dual work function on drain electrode using high-dose nitrogen implantation [17]. Dual work functions of the metal are adjusted by the use of high nitrogen implant and dose on molybdenum (Mo). For this, annealing at 700°C provides lowering of the work function and subsequent annealing at 900°C increases the work function [17]. Hence, the use of P+ dopants as parent substrate and dual work functionality over the drain region and formation of channel and drain region by CP concept in the case of proposed device will be useful for simpler fabrication, better electrical behaviour with less variability of the device [18]. The simulation-based results of our proposed structure with optimisation of device dimensions will provide platform for extension of this work at the experimental level.

The simulations are performed by using 2-D Silvaco ATLAS simulator version 5.20.2.R [19]. In this regard, Shockley–Read–Hall and Auger recombination models are employed due to presence of high impurity in the channel and minority recombination effects [20]. The bandgap narrowing model is employed for considering the bandgap shrinkage by high impurity doping. Further, the non-local BTBT model is used to account tunnelling generation rate of charge carriers at source/channel and drain/channel junctions. This non-local model uses the Wentzel–Kramer–Brillouin approximation to calculate the tunnelling probability and numerical solutions. In addition to these, quantum confinement model given by Hansch [21] and trap assisted tunnelling model given by Schenk are also employed [21].

3. Results and discussions

3.1. Performance comparison of DDW JL TFET with JL TFET: Analysis of variation occurring in DDW JL TFET in comparison to JL TFET with the influence of work function (ϕ_{M3}) is shown in Fig. 2 in terms of carrier concentration and energy band levels under equilibrium state. From Fig. 2, it can be observed that proposed modification in the device configuration results into asymmetric concentration of electrons and holes in the drain region under section $M2$ and $M3$. Relatively higher value of ϕ_{M3} with respect to ϕ_{M2} provides lower electron concentration and higher hole concentration in DDW JL TFET as compared to JL

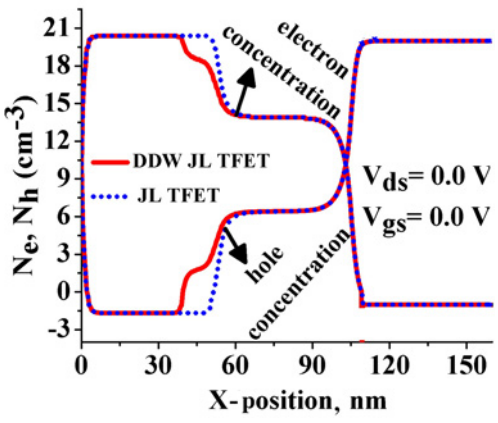

Fig. 2 *Comparison of JL TFET and proposed DDW JL TFET: carrier concentration under thermal equilibrium state*

TFET under section $M3$. Further, the clear understanding of tunnelling barrier can be visualised from Fig. 3. Since, the modification is made on the drain side, therefore no change is observed in the tunnelling distance at the source/channel interface (Fig. 3). Barrier at the drain/channel junction is modified as an upliftment of the bands under section $M3$ of drain electrode (Fig. 3). Thus, the increased tunnelling barrier can be seen at the drain/channel interface under thermal equilibrium, for DDW JL TFET. Henceforth, due to asymmetric concentration and varied band levels, there is variation in electric field at drain/channel junction along the lateral device dimensions as shown in Fig. 4*a* (equilibrium state), from where, we can infer out that the proposed device has reduced electric field under section $M3$ as compared to JL TEFT.

Whereas, the electric field in the other portion of proposed device is similar to JL TFET. Now comparing Fig. 3 (thermal equilibrium-state) and Fig. 4*b* (ambipolar state), as negative gate bias is applied keeping V_{ds} same (Fig. 4*b*), it is observed that conduction band and valence band of channel region gets aligned with conduction band and valence band of source region, respectively (Fig. 4*b*), which increases the barrier at source/channel interface and suppresses the flow of charge carriers. Whereas, at drain/channel interface conduction band of JL TFET gets aligned with valence band of DDW JL TFET (ambipolar state, Fig. 4*b*), but in case of DDW JL TFET barrier is larger in comparison to JL TFET. This higher barrier (for DDW JL TFET) at drain/channel junction limits the amount of holes to tunnel from drain to channel, in consequence of which, reduction in the drain current in ambipolar state can be noticed in Fig. 4*c* for the proposed device. Apart from this, a comparative analysis for tunnelling rate of holes is shown with negative gate bias in Fig. 4*d*, which illustrates that, JL TFET exhibits higher holes tunnelling rate due to less barrier height at the drain/channel junction leading to high ambipolar nature. Whereas, DDW JL TFET posses lesser holes tunnelling rate at the drain/channel junction due to the presence of dual drain work functionality which increases the barrier height at drain/channel junction as seen earlier in Fig. 4*b* leading to a huge reduction in ambipolar behaviour of the device.

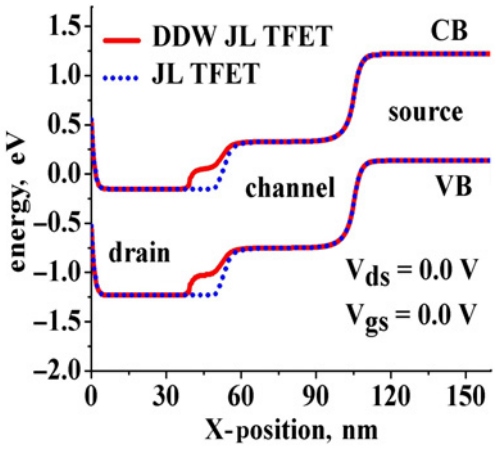

Fig. 3 *Comparison of JL TFET and proposed DDW JL TFET: energy band levels under thermal equilibrium state*

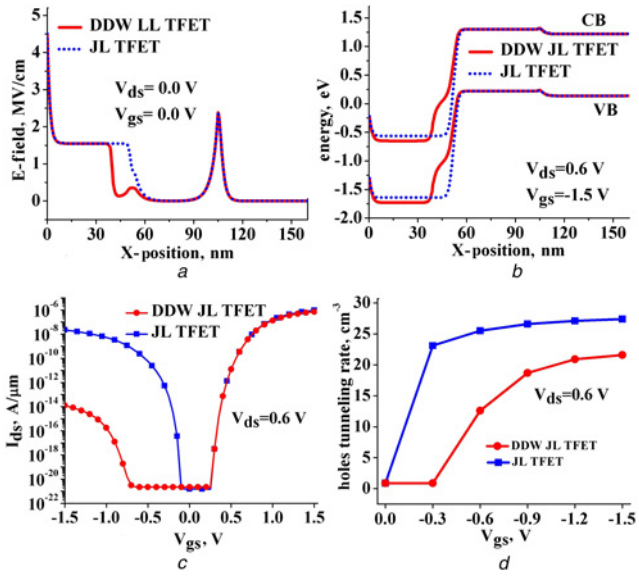

Fig. 4 *Comparison between JL TFET and DDW JL TFET*
a Electric field under thermal equilibrium state
b Energy band diagram under ambipolar state
c Transfer characteristics
d Holes tunnelling rate with negative gate bias

3.2. Optimisation of ϕ_{M3} and L_A of section $M3$ for DDW JL TFET: The use of dual drain work functionality in the proposed device suppresses the ambipolar current by a good amount as shown in Fig. 4*c*. Therefore, this section is fully dedicated to study the impact of variation in ϕ_{M3} and L_A on the band energies and transfer characteristics of the device. The increase in the value of ϕ_{M3} shifts the bands upwards as depicted in Fig. 5*a*. This increased energy of bands leads to misalignment of large discrete energy levels at the drain/channel interface, which increases the tunnelling barrier for the holes to tunnel from drain to channel, as a consequence, reduction of ambipolar behaviour takes place with the increment of work function (ϕ_{M3}) as pictured in Fig. 5*b*. However, this increment of energy level with ϕ_{M3} under section $M3$ also creates hurdle and acts as barrier in the path of charge carriers (electrons) to flow from channel to drain region under ON-state. Hence, ON-state current degrades for the larger values of ϕ_{M3} as depicted in Fig. 5*b*. Thus, from the aforementioned analysis, it can be concluded that, full suppression of ambipolar nature can be achieved by selecting higher values for ϕ_{M3} at the cost of degradation in ON-state current. Hence, a trade-off is required while selecting the value of ϕ_{M3} in terms of ON-state current and ambipolarity.

Further to this, the energy band diagram and transfer characteristics of the device are analysed at the constant value of ϕ_{M3} against the variation of L_A in Fig. 6. In this case, the increase in the value of L_A increases the length of shift in the energy levels as shown in Fig. 6*a*. Therefore, a higher lateral distance (Fig. 6*a*) is created for tunnelling of holes, as a result of that, reduction in the ambipolar current takes place (Fig. 6*b*). Apart from this, when we compare Fig. 5*b* with Fig. 6*b* it is observed that after some extent, the order of suppression of ambipolar current with the variation of L_A is lower (Fig. 6*b*) compared with variation in ϕ_{M3}

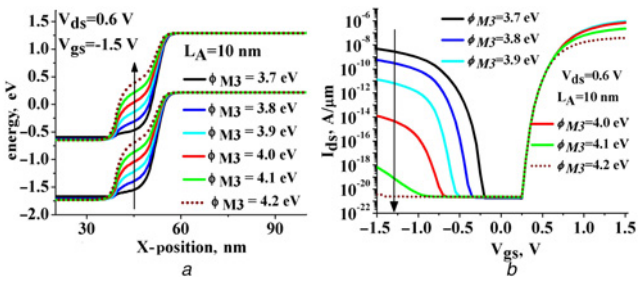

Fig. 5 *Energy band levels and transfer characteristics*
a Energy band levels
b Transfer characteristics of DDW JL TFET at various ϕ_{M3}

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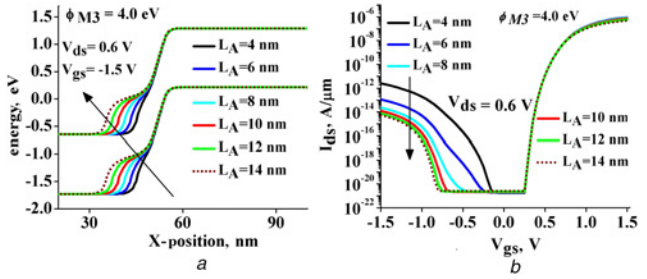

Fig. 6 *Energy band diagram and transfer characteristics of the device are analysed at the constant value of ϕ_{M3} against the variation of L_A*
a Energy band levels
b Transfer characteristics of DDW JL TFET at different L_A

(Fig. 5*b*) due to existence of some aligned bands. However, the ON-state current of device is not significantly degraded with variation in L_A (Fig. 6*b*). Finally, the combined effect of variation in ϕ_{M3} and L_A on ON-state current and ambipolar nature is shown in Figs. 7*a* and *b*. Here, we can observe that there is no noticeable change in I_{ON} for $\phi_{M3} < 4.0$ eV (Fig. 8*a*), but as the ϕ_{M3} exceeds 4.0 eV, I_{ON} starts degrading and becomes severe for $\phi_{M3} \geq 4.1$ eV. Therefore, it is suggested to use ϕ_{M3} below 4.1 eV. Similarly, Fig. 7*b* shows the sensitivity of ambipolar current with the variation in L_A and ϕ_{M3}, where it is observed that, there is no considerable degradation of ambipolar behaviour for $\phi_{M3} > 4.1$ eV and $L_A > 10$ nm, whereas degradation of I_{ON} occurs in Fig. 7*a* for $L_A > 10$ nm and $\phi_{M3} > 4.1$ eV. Hence, we can conclude that selecting $L_A = 10$ nm and $\phi_{M3} = 4.0$ eV provides decent amount of suppression in ambipolar nature without degrading the device current driving capability.

3.3. Parasitic capacitance and high-frequency performance: This section represents the potentiality of the proposed modification in the device for improving parasitic capacitance and RF parameters in terms of cut-off frequency (f_T) and gain band width product (GBP). Parasitic capacitance is a crucial parameter of the

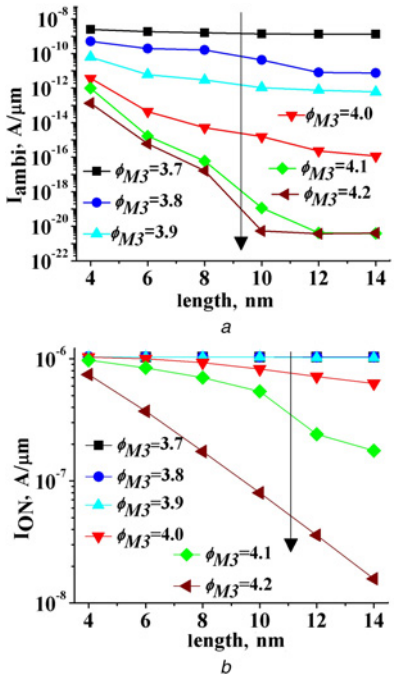

Fig. 7 *Sensitivity of ambipolar current with the variation in L_A and ϕ_{M3}*
a I_{ON}
b I_{ambi} w.r.t L_A at different values of ϕ_{M3}

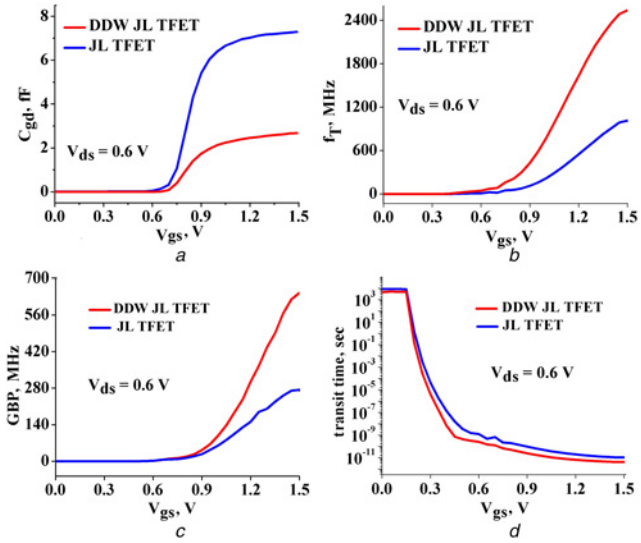

Fig. 8 *Comparison between JL TFET and DDW JL TFET*
a C_{gd}
b f_T
c GBP
d τ

device for the electrostatic control over the channel and obtaining high-frequency responses. Smaller value of C_{gd} provides better controlling of gate over the channel region in the case of proposed device. The parameter C_{gd} is lesser as compared to JL TFET as shown in Fig. 8*a*. The parameters f_T and GBP are computed using the formulae $f_T = g_m/(2\pi(C_{gs} + C_{gd}))$ and $\text{GBP} = g_m/20\pi C_{gd}$ with the help of TCAD simulations. The reduced value of the C_{gd} for proposed device reflects as increment in f_T and GBP which can be noticed in Figs. 8*b* and *c*. Apart from this, comparison of transit time (τ) is shown in Fig. 8*d*. τ decides the ability of a device to be operated in high-frequency microwave electronics. In this respect, Fig. 8*d* demonstrates that DDW JL TFET requires lesser time to tunnel from source to channel ensuring its high speed compared with JL TFET. It is computed using the relation $\tau = 1/(2\pi f_T)$. Thus, the proposed modification facilitates the device with better high-frequency performance and high operational speed.

3.4. Modelling of proposed DDW JL TFET circuit level performance comparison of JL TFET and DDW-JL TFET: Circuit level modelling and comparison of the conventional and proposed device are described in this section. For this, a lookup table based Verilog-A is developed for circuit implementation. This method is very accurate for estimating circuit level performance [22]. The capacitances C_{gs} and C_{gd} are incorporated including inner fringing and overlap capacitances between gate and source and between gate and drain, respectively [22]. Lookup table based approach is applied to compare the SNM of conventional and proposed inverter made by the device. For this, we have designed inverter of both the devices, considering its P-type and N-type configurations. I_{ON} and I_{OFF} of P-type are maintained same as that of N-type to make a fair comparison of circuit level parameters. An inverter is a basic block to implement a memory whose stability is related to SNM. SNM is defined as the highest dc noise voltage where the state of cell is not changed while it is accessed [23–25]. Basic inverter circuit is depicted in Fig. 9*a*. Lookup table model to compute *I–V* and *C–V* is built by TCAD data based on the device parameters.

Noise margin calculation is done by butterfly curves which is formed by superimposing voltage transfer characteristics (VTCs) and inverse VTC curves [23, 26, 27] as shown in Figs. 9*a* and *b*.

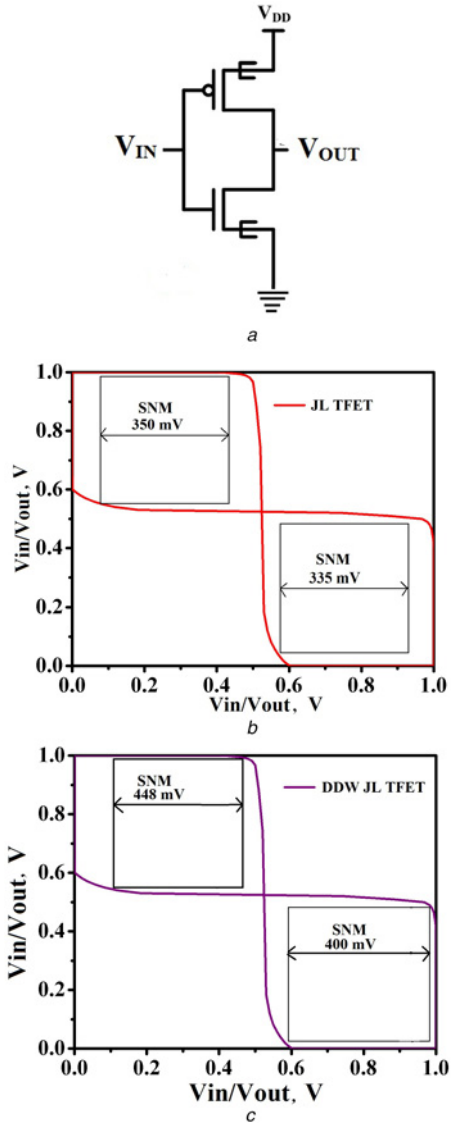

Fig. 9 *JL TFET based inverter circuit and butterfly curve*
a JL TFET based inverter circuit
b Butterfly curve of JL TFET to measure noise margin
c Butterfly curve of DDW JL TFET to measure noise margin

Extraction of SNM from both the VTCs is done by square fitting method (largest square is fitted in the overlapped plot of inverter [23]). Figs. 9*b* and *c* show the comparison of noise margin of JL TFET and DDW JL TFET, respectively, where it is clear that the noise margin is higher for the proposed device (DDW JL TFET). As the proposed device shows better SNM than JL TFET, therefore, optimisation of SNM at different voltages is evaluated for DDW JL TFET and obtained as follows: 198 mV for 0.5 V, 267 mV for 0.7 V and 352 mV for 0.9 V. Power dissipation for conventional device is obtained 63.44 and 61.12 pW for proposed device. Based on the transient response, inverter characteristics such as delay time τ_p, rise time τ_r, fall time τ_f, noise margin high NM_L and noise margin high NM_H are calculated and presented in Table 1 where it is clear that DDW JL TFET shows better results which implies that DDW JL TFET is applicable for low-power circuit applications. Further, NAND logic is implemented with Verilog-A model of JL TFET (Fig. 10*a*). Figs. 10*b* and *c* show the input (V_{in1}, V_{in2})/output (V_{out}) waveform of NAND logic for JL TFET and DDW JL TFET, respectively, where it is observed that (V_{out}) waveform of JL TFET is distorted whereas the (V_{out}) waveform of DDW JL TFET is smooth for entire range of (V_{in1}, V_{in2}). Apart from this, the switching time for JL TFET is delayed as compared to the DDW JL TEFT observed in the same figures. This shows that DDW JL TFET has better switching time

Table 1 Evaluation for transient analysis

Parameters	JL TFET	DDW JL TFET
τ_p, ns	8	3.44
τ_r, ns	3	0.2
τ_f, ns	3	0.2
NM_H, mV	420	440
NM_L, mV	395	400
p_d, pW	63.44	61.12

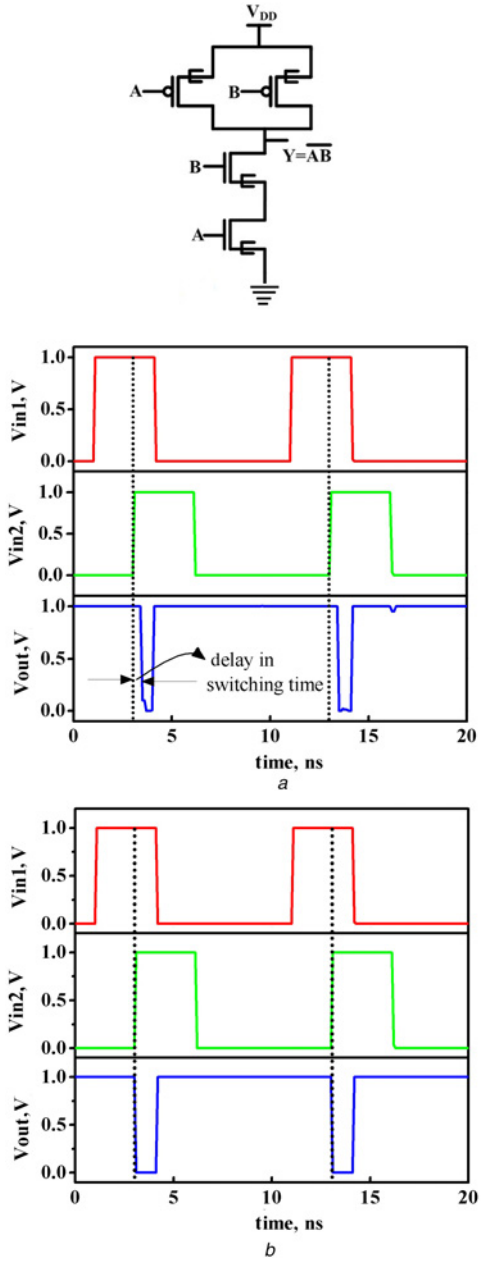

Fig. 10 *NAND logic and input (V_{in1}, V_{in2})/output (V_{out}) waveform*
a NAND logic
b Input (V_{in1}, V_{in2})/output (V_{out}) waveform of NAND logic for JL TFET
c Input (V_{in1}, V_{in2})/output (V_{out}) waveform of NAND logic for DDW JL TFET

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and less distortion (less noise) which is due to decreased junction capacitance (as shown previously in Fig. 8*a*).

4 Conclusion: In this Letter, we have presented a new approach to implement a JL TFET considering P^+ substrate as parent doping and then depositing metal electrode for the formation of N^+ drain region and intrinsic channel region. This brings abruptness at the source/channel junction and improves the device performance. Further, a novel concept of dual work functionality is used on the drain electrode to create a graded drain profile, which helps to achieve suppression in ambipolar nature of device. The importance of selecting work function (ϕ_{M3}) and length (L_A) of section *M*3 at drain electrode is also demonstrated to make a trade-off between ON-state current and ambipolar conduction of the device. Further, it is presented that DDW JL TFET offers superior device behaviour in terms of gate-to-drain capacitance and high-frequency response in comparison to JL TFET. Along with DC and analogue/RF parameters, circuit level performance is also evaluated by implementing the inverter and NAND logics of both the devices with the help of Verilog-A model. The circuit level performance parameters such as SNM, delay time τ_p, rise time τ_r, fall time τ_f, noise margin high NM_L and noise margin high NM_H were improved in case of DDW JL TFET which shows its potential for low-power circuit applications. NAND logic is implemented for both the devices and found that DDW JL TFET is less noisy and provides fast switching.

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