Complementary metal-SU8-graphene method for making integrated graphene nanocircuits

Haider Al-Mumen[1] ✉, *Wen Li*[2]

[1]*Department of Electrical Engineering, University of Babylon, Babylon, Iraq*
[2]*Department of Electrical and Computer Engineering, Michigan State University, East Lansing MI, USA*
✉ *E-mail: hayderalmumen@gmail.com*

Published in Micro & Nano Letters; Received on 6th July 2017; Revised on 4th December 2017; Accepted on 11th December 2017

This work reports a complementary metal-SU8-graphene (MSG) method for constructing integrated graphene nanocircuits with excellent air and temperature stability. In this approach, electron beam (e-beam) lithography was first used to selectively pattern micro/nanoscale meshes on pristine graphene to form p-type regions. Then SU-8 thin films were spun and e-beam patterned to convert the target region of p-type graphene into n-type. The SU-8 was utilised as a doping source and an encapsulating layer for n-type graphene. To demonstrate the proposed MSG method, a graphene-based voltage inverter is constructed by complementary doping p- and n-type field effect transistors on a single graphene sheet. The electronic and thermal characteristics of the fabricated device were also studied.

1. Introduction: Graphene has a unique combination of ultrahigh electron mobility and cutoff frequency [1, 2], which makes it an ideal candidate for the development of future integrated nanocircuits. Although several techniques have been proposed for the design of graphene radio-frequency circuits [3, 4], making digital circuits by graphene, still remain challenging due to the lack of reliable doping techniques for obtaining ambient stable n-type graphene [5–11]. Several techniques have been proposed for the design of graphene inverters but either only p-types field effect transistors (FETs) or p-type FET and unstable n-type FET have been used in those circuits [12, 13].

Another critical challenge in the design of graphene circuits is the selective n-doping of a graphene sheet within micro or nanoscale areas. The previously reported techniques usually doped the entire substrate surface, which is obviously unpractical for the constructing of integrated circuits. Recently, Aktary and co-workers have selectively n-doped graphene in millimetre scale [14]. Our previous work [15, 16] demonstrated that the SU-8 is an effective and reliable doping and encapsulation material for constructing nanometre-scale n-type graphene FETs with air stability. Based on such the SU-8 doping technique, the main contribution of this Letter is to demonstrate a complementary metal-SU8-graphene technique, which is capable of constructing both p- and n-type graphene FETs on a single substrate to achieve a monolithically integrated digital circuit. To demonstrate the feasibility of this method, we designed, constructed, and characterised an integrated graphene inverter circuit.

2. Methodology

2.1. E-beam lithography: Graphene integrated circuits require making both n-type and p-type transistors monolithically on a single substrate. Therefore, it is very important to develop a technique capable of selective doping and patterning n-type graphene using SU-8 that was demonstrated previously as an electron dopant. While photolithography of SU-8 has been widely used in microfabrication processes that required thick photoresist structures, the photolithographic method usually suffers from limited resolution and is not suitable for patterning submicron and nanoscale features. Aktary *et al.* [17] reported on electron beam lithography of SU-8 where a thin SU-8 film can be exposed using e-beam lithography to achieve small feature sizes down to 30 nm. Basically, the chemical reaction of SU-8 during e-beam exposure is similar to that during ultraviolet (UV) exposure. In both cases, SU-8 behaves as a negative resist. Upon irradiation, the photo-acid generator decomposes to hexaflouroantimonic acid that causes a highly cross-linked and insoluble polymer.

We carefully adjusted the parameters of the e-beam lithography to obtain sharp patterns at a particular location of the graphene sheet. For all experiments, we used the commercially available SU-8 2000.2 and SU-8 3005. The resist was spin-coated on the substrate with a spin speed of 6000 rpm to realise a thin layer of SU-8 of <1 μm. Different SU-8 thicknesses can be achieved by selecting different SU-8 models (2000 and 3000 series) and varying the spin speed. If a thinner SU-8 layer is desired, chemicals such as cyclopentanone can be added to any SU-8 models. Following spin coating, the SU-8 film was soft baked and hard baked at 65 and 95°C, respectively, for 2 min. The soft-baked SU-8 was patterned using JEOL 840 e-beam lithography instrument. The acceleration voltage and beam current were selected empirically to be 35 kV and 25 pA, respectively. After that, the exposed resist was developed for 1 min, followed by immersion in isopropanol alcohol and a rinse with deionised water.

The e-beam lithography parameters are kept constant except the beam dose, which was used to determine the width of the photoresist pattern. In order to study the resolution limit of e-beam exposed SU-8 patterns, the SU-8 resist was exposed using different areal doses between 3 and 300 μC/cm^2. Fig. 1 shows the optical microscope images of the resulting patterns, suggesting that the e-beam writing resolution was significantly affected by the beam dose. Large areas of undeveloped SU-8 residues were observed around the desired patterns at high e-beam doses of around 300 μC/cm^2 (Figs. 1*a* and *b*), which broadened randomly the desired patterns. Therefore, using the lowest effective dose is considered to be the best solution to reducing SU-8 residues and improving pattern resolution. Experiment results show that the optimal e-beam dose for full exposure of ~0.5 μm thick was ~4 μC/cm^2.

2.2. Fabrication of a graphene inverter circuit: One great benefit of using e-beam lithography to expose SU-8 is the ability to selectively pattern and n-dope a graphene sheet at the nanoscale. As a demonstration of the technique, we constructed a graphene inverter circuit (a logic NOT gate), by integrating both n- and p-type graphene FETs on a single substrate. In this case, the SU-8 coated graphene formed an n-type region and the uncoated graphene was a p-type region, as schematically shown in Fig. 2*a*.

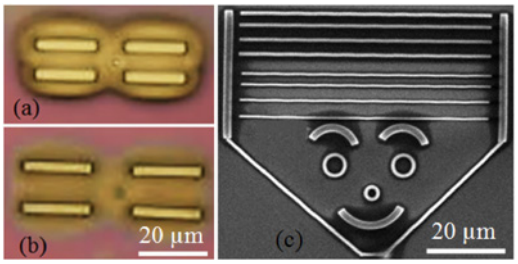

Fig. 1 *SU-8 patterns with various feature sizes (500 nm–3 μm), exposed using different areal doses*
a 300 μC/cm^2
b 15 μC/cm^2
c 4 μC/cm^2

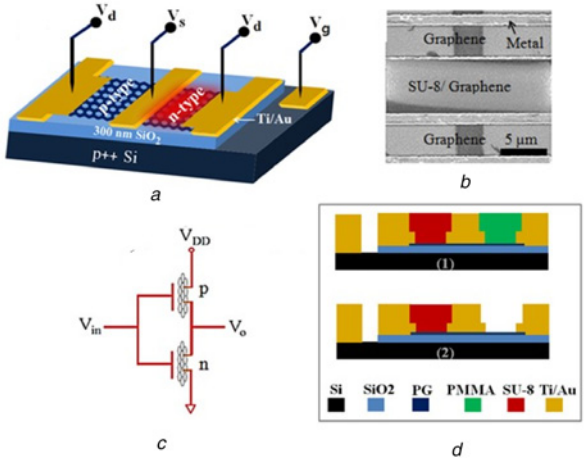

Fig. 2 *Integrated graphene inverter*
a Schematic of the circuit fabrication
b SEM image of the fabricated inverter
c Circuit layout
d Schematic of the fabrication technique to avoid impinging electrons

The SU-8 doping and patterning followed the aforementioned methods. Three metal electrodes (Au/Ti) were constructed on the graphene sheet to form two transistors. The two transistors shared a same back gate as an input voltage terminal (V_{in}). The source and drain of the two transistors are connected together as shown in Fig. 2*d* to form an inverter circuit. Moreover, to avoid impinging electrons during e-beam lithography, a sacrificial layer of PMMA or copper is required. After developing SU-8, the sacrificial layer can then be dissolved in acetone (for PMMA) or $FeCl_3$ (for copper).

3. Device characterisation and discussion

3.1. Characteristics of the as-fabricated graphene circuit: To verify the formation of the n-type and p-type transistors on the same graphene sheet, the transfer resistances R_p and R_n between the source and drain contacts of the individual FETs were measured as a function of the applied voltage V_{in} (Fig. 3). The measured Dirac points of both the n-type and p-type graphene sheets were at −27 and 17 V, respectively. By connecting p-type FETs to V_{DD} and n-type FET to the ground, a Dirac point splitting along the V_{in} axis and then the complementary configuration was achieved within the region of Dirac points.

The inverter function was demonstrated by connecting the source of the n-type FET to the ground, the source of the p-type FET to a supply voltage (V_{DD}), and the output (V_0) to the common drain of the FETs. The output voltage for this configuration was given by $V_0 = V_{DD}\ R_n/(R_p + R_n)$. The voltage transfer characteristic of the

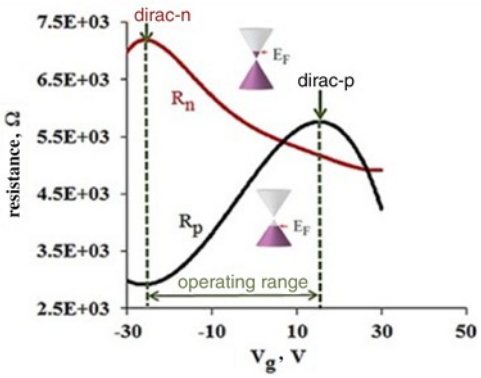

Fig. 3 *Resistance curve (R versus V_{in}) of graphene transistors schematically illustrated in Fig. 1, measured at room temperature*

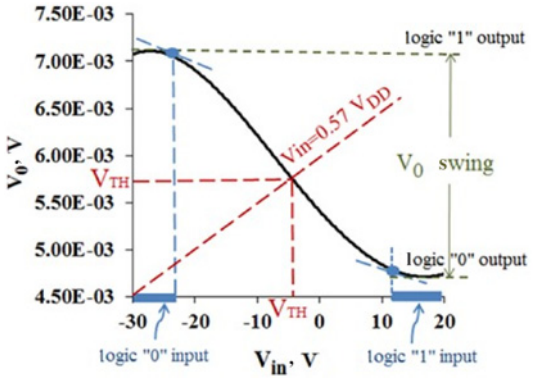

Fig. 4 *Voltage transfer characteristic, demonstrating a logic inverter function*

fabricated inverter is given Fig. 4. The two FETs operated in the range between the Dirac points, where the increase in V_{in} caused the increase of R_p and the decrease of R_n, thus the increase in the ratio of R_n/R_p. As a result, V_0 decreased with the increase in V_{in}, leading to the voltage inversion. Away from the Dirac points, the saturation of the output voltage V_0 resulted in the approximately constant ratio of R_n/R_p, when $V_{in} < -27$ V for the n-type FET and $V_{in} > 17$ V for the p-type FET. Due to the small bandgap of the doped graphene, the output voltage could not saturate to zero or V_{DD}, indicating that the as-fabricated graphene inverter could not be completely turned-off. The voltage gain of the inverter was much less than 1, as determined by $A = dV_0/dV_{in}$. The small voltage gain of the fabricated inverter could be mainly due to the very small change of the transistor resistances around the Dirac points. The voltage gain can be increased by decreasing the oxide thickness. The swing voltage of the inverter was 3 mV at $V_{DD} = 10$ mV. The threshold voltage (V_{TH}), which is the input voltage at the maximum voltage gain of the inverter, was ~5.6 mV ($V_{in} = V_{TH}$) and slightly greater than $V_{DD}/2$, which is the conventional CMOS inverter value.

3.2. Effect of the SU-8 thickness and soft-bake: The n-type semiconductor properties of graphene can be controlled by carefully selecting the soft-baking time and the thickness of the SU-8 layer, as appear in Fig. 5. We noticed the soft-baking time has a significant effect on the Dirac point and Fermi level. Specifically, longer baking time pushes the Dirac point more towards the left-hand side of I_{ds}–V_g characteristic curve, which means higher n-doing level of graphene. Maximum shifting in the Dirac point was from 50 to −75 V. This can be attributed to the increase of the concentration of the photo acid generator of the

doi: 10.1049/mnl.2017.0508

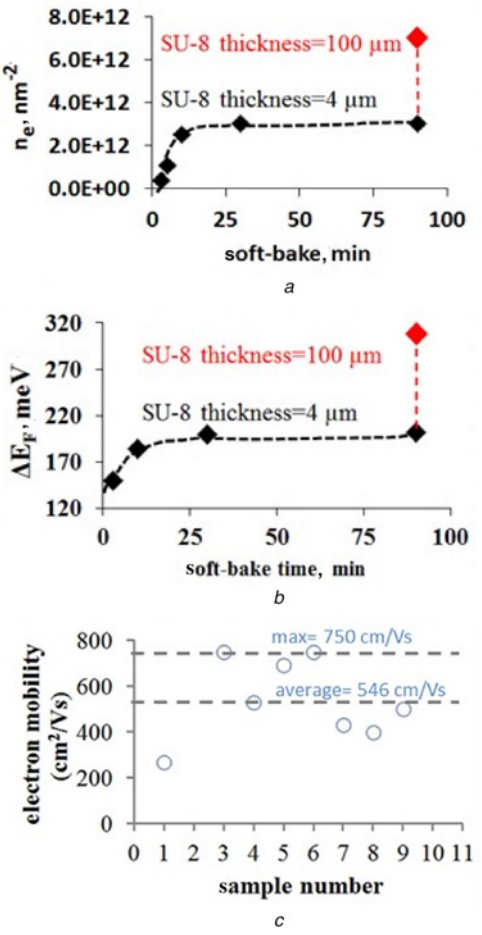

Fig. 5 *Electronic characteristic of the device*
a Electron concentrations (n_e) and Fermi level shift (ΔE_F) of graphene samples as a function of SU-8 thickness and soft-baking duration
b Fermi Level at various soft-bake times
c Electron mobility of eight samples

SU-8 compound due to evaporating of the solvent, the other compound of the SU-8, during baking. The electron areal concentrations (n_e) were estimated by $n_e = \eta(V_g - V_d)$ with $\eta = C_{ox}/e = (\varepsilon_0\varepsilon_r)/(te) = 7.2 \times 10^{10}$ cm^{-2} V^{-1}, where C_{ox} is the oxide capacitance, t is the SiO_2 thickness (300 nm), ε_0 is the permittivity of free space, ε_r is the relative permittivity of SiO_2, V_g is the gate voltage, V_d is the gate voltage at the Dirac point, and e is the electron charge. The location of the Fermi level with respect to Dirac point can be calculated using the equation: $\Delta E_F = \sqrt{\pi n_e (\hbar v_F)^2}$, where v_F is the Fermi velocity of electrons ($\simeq 10^8$ cm/s), and E_F and E_D are the energy positions of the Fermi level of the n-type graphene and the Dirac point, respectively [18]. As expected, the increased absorption of the donors (the photo-acid generator) can effectively enhance the electron doping concentration, resulting in the upward movement of the Fermi level and thus larger ΔE_F. The maximum achieved electron mobility was 750 cm^2/Vs and the average electron mobility ($n = 8$) was 546 cm^2/Vs, as shown in Fig. 5*b*.

3.3. Temperature stability of the SU-8 doped graphene FET: The temperature stability or operation temperature range of a graphene transistor is one of the significant factors that has to be taken into account. We studied the current transfer characteristics of graphene FETs doped with cross-linked SU-8, in a wide temperature range from RT to 100°C. Fig. 6 demonstrates the temperature stability of the n-type properties of a device within

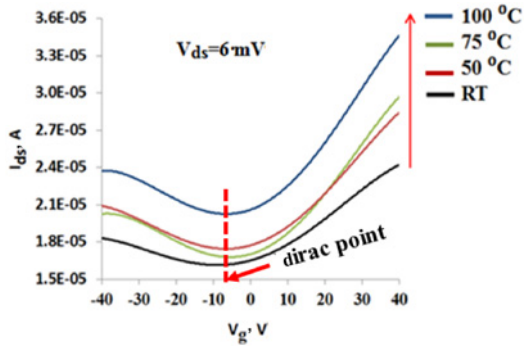

Fig. 6 *Temperature stability of n-type graphene FETS*

the testing temperature range, in which only a small shift in the Dirac point was observed. The V_g–I_{ds} slopes of the current transfer characteristic curves showed no significant changes in the electron mobility. Maximum achieved electron mobility for n-doped graphene was ~750 cm^2 V^{-1} s^{-1}. The slight shifting was observed, in the drain current (I_{ds}) which can be attributed to the negative resistance temperature coefficient behaviour of the graphene [19].

4. Conclusion: Graphene doping at a dedicated area within a microscale graphene sheet represents a practical method for the MSG technology. Our fabrication method is compatible with the conventional microfabrication technology, which makes it a candidate technique for graphene integrated circuits. A graphene-based inverter was fabricated and characterised as a case study, which exhibits a clear voltage inversion property. The n-doped integrated circuit was stable in air and in a wide temperature range.

Even though, it is difficult to completely turn off the inverter due to the small bandgap of the doped graphene, this technique is still promising for analogue integrated circuit design.

5 References

[1] Novoselov K.S., Geim A.K., Morozov S.V., *ET AL.*: 'Electric field effect in atomically thin carbon films', *Science*, 2004, **306**, pp. 666–669
[2] Bolotin K.I., Sikes K.J., Jiang Z., *ET AL.*: 'Ultrahigh electron mobility in suspended graphene', *Solid State Commun.*, 2008, **146**, pp. 351–355
[3] Lin Y.-M., Valdes-Garcia A., Han S.-J., *ET AL.*: 'Wafer-scale graphene integrated circuit', *Science*, 2011, **332**, pp. 1294–1297
[4] Wang H., Hsu A., Wu J., *ET AL.*: 'Graphene-based ambipolar RF mixers', *IEEE Electron Device Lett.*, 2010, **31**, pp. 906–908
[5] Lin Y.-C., Lin C.-Y., Chiu P.-W.: 'Controllable graphene N-doping with ammonia plasma', *Appl. Phys. Lett.*, 2010, **96**, p. 133110
[6] Wei D., Liu Y., Wang Y., *ET AL.*: 'Synthesis of N-doped graphene by chemical vapor deposition and its electrical properties', *Nano Lett.*, 2009, **9**, pp. 1752–1758
[7] Guo B., Liu Q., Chen E., *ET AL.*: 'Controllable N-doping of graphene', *Nano Lett.*, 2010, **10**, pp. 4975–4980
[8] Zhao L., He R., Rim K.T., *ET AL.*: 'Visualizing individual nitrogen dopants in monolayer graphene', *Science*, 2011, **333**, pp. 999–1003
[9] Wang X., Li X., Zhang L., *ET AL.*: 'N-doping of graphene through electrothermal reactions with ammonia', *Science*, 2009, **324**, pp. 768–771
[10] Englert J.M., Dotzer C., Yang G., *ET AL.*: 'Covalent bulk functionalization of graphene', *Nat. Chem.*, 2011, **3**, pp. 279–286
[11] Childres I., Jauregui L.A., Foxe M., *ET AL.*: 'Effect of electron-beam irradiation on graphene field effect devices', *Appl. Phys. Lett.*, 2010, **97**, p. 173109
[12] Rizzi L.G., Bianchi M., Behnam A., *ET AL.*: 'Cascading wafer-scale integrated graphene complementary inverters under ambient conditions', *Nano Lett.*, 2012, **12**, pp. 3948–3953
[13] Traversi F., Russo V., Sordan R.: 'Integrated complementary graphene inverter', *Appl. Phys. Lett.*, 2009, **94**, p. 150

[14] Chen H., Cao Y., Zhang J., *ET AL.*: 'Large-scale complementary macroelectronics using hybrid integration of carbon nanotubes and IGZO thin-film transistors', *Nat. Commun.*, 2014, **5**, pp. 1–9
[15] Al-Mumen H., Dong L., Li W.: 'SU-8 doped and encapsulated n-type graphene nanomesh with high air stability', *Appl. Phys. Lett.*, 2013, **103**, p. 232113
[16] Al-Mumen H.: 'Characterisation of SU-8 n-doping carbon nanotube-based electronic devices', *Micro Nano Lett.*, 2015, **10**, pp. 670–673
[17] Aktary M., Jensen M.O., Westra K.L., *ET AL.*: 'High-resolution pattern generation using the epoxy novolak SU-8 2000 resist by electron beam lithography', *J. Vac. Sci. Technol. B*, 2003, **21**, p. L500
[18] Al-Mumen H., Rao F., Dong L., *ET AL.*: 'Thermo-flow and temperature sensing behaviour of graphene based on surface heat convection', *Micro Nano Lett.*, 2013, **8**, pp. 681–685
[19] Al-Mumen H., Rao F., Dong L., *ET AL.*: 'Design fabrication and characterization of graphene thermistor'. 8th IEEE Int. Conf. Nano/Micro Engineered and Molecular Systems (NEMS), 2013

doi: 10.1049/mnl.2017.0508