Modified Schottky Barrier CNTFET with lightly doped drain

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For the first time, a modified Schottky barrier carbon nanotube field-effect transistor (SB-CNTFET) with lightly doped drain (LDD) has been proposed. The newly designed CNTFET benefits from the advantages of both SB in source and the lightly doped ohmic drain contact. Simulations are based on two-dimensional non-equilibrium Green's function solved self-consistently with Poisson's equation. To get to an improved electrical characteristic, comparisons have been made among four CNTFET structures which are conventional SB-CNTFETs, triple LDD-CNTFET (TLDD-CNTFET), double LDD-CNTFET and Schottky source and ohmic drain CNTFET. The results show that the TLDD-CNTFET design decreases the leakage current significantly and increases on–off-current ratio as well as the cut-off frequency. It is also demonstrated that TLDD-CNTFET structure possesses three perceivable steps in the potential profile of the channel, which leads to additional lateral electric field peaks inside the channel and thus improve the immunity against short-channel effects. The important parameters such as transconductance, on–off ratio, subthreshold swing, cut-off frequency, delay and drain-induced barrier lowering of the CNTFETs have been calculated and discussed. Results show that by using lightly doped regions in the drain of SB-CNTFETs, the dc and ac characteristics have been considerably improved compared with the conventional SB-CNTFET.

1. Introduction: Carbon nanotube field-effect transistor (CNTFET) is a type of molecular transistor that has already demonstrated high on-current [1–4]. As the gate dielectric thickness scales down to about 1 nm, the gate tunnelling leakage current increases drastically, leading to high-power consumption and reduced device reliability [5]. This problem can be solved by employing high k dielectric materials. Scaling down of the metal–oxide–semiconductor field-effect transistors (MOSFETs) results in degradation in their performance. Some important issues associated with short-channel effects (SCEs) which cause reliability problems in nanoscale MOSFETs are: drain-induced barrier lowering (DIBL), hot-carrier effect at large drain voltages, lack of pinch-off, shift in threshold voltage with changing channel length and degradation of the subthreshold slope [6]. Significant advances have been achieved in understanding device physics and improving device performance for CNTFETs [7, 8]. Replacing the silicon channel of MOSFETs with one-dimensional (1D) CNTs results in room-temperature ballistic transport over several hundred nanometres, larger current density and surpassing the SCEs which deteriorated the performance of the nanoscale silicon MOSFETs [9]. The larger carrier mobility in CNTs provides the possibility of larger current density and high-frequency operation of CNTFETs.

Performance optimisations of conventional CNTFETs and graphene nanoribbon FETs (GNRFETs) have been under study for some years [10–12]. As for source and drain contacts, underlaps with staircase doping, Schottky_Ohmic CNTFET, were introduced previously by Lin *et al.* [13]. The idea of changing the doping near the contacts directly changes the energy band diagram and the charge transport in the channel and this, in turn, would modify the device characteristics [1, 10, 11].

A tunnelling GNRFET has been proposed in [5] in which a conventional GNRFET has been modified, so that its heavily doped drain extension has been replaced by a linear doping profile while the source side has remained unchanged with a Schottky contact. The device is called Schottky–ohmic GNRFET. Also in a recent Letter, a GNRFET with locally embedded stone-wales (SW) defects near its drain contact has been investigated. Localised states induced by the SW defects are able to reduce ambipolar conduction and provide higher on–off ratio and attenuated kink effect [12].

In this Letter, we propose a Schottky barrier-CNTFET (SB-CNTFET) with a Schottky contact at the source and a lightly doped ohmic contact at the drain. A 2D numerical simulation, which is based on the self-consistent solution of the 2D Green's function and Poisson equation has been used [14–16]. The current–voltage characteristic of the proposed transistor is modified, so that instead of an ambipolar behaviour it is efficiently unipolar. The simulation results show that the off-state current of the Schottky_Ohmic CNTFET has a lower magnitude than SB_CNTFETs. The reason is that in the Schottky_Ohmic CNTFET contrary to the SB_CNTFET, in all of the gate voltages, the majority carriers are electrons and the current originates from the tunnelling of the electrons from the SB at the source [5, 13]. The important transistor parameters have been calculated such as on-current, off-current, on–off ratio, transconductance (g_m), subthreshold swing (SS), delay (τ), DIBL and cut-off frequency (f_T). The simulations show that by using the proposed design significant ac and dc performance improvements have been obtained.

New structures have been designed based on arranging lightly and heavily doped regions at the drain. Four different structures have been simulated and their characteristics have been compared with each other. Finally, based on the new designs and comparisons, the best structure with the ultimate performance has been obtained and introduced. It is clear from results that the new structure has a lower off-current and in turn a larger I_{on}/I_{off}. The cut-off frequency has been increased compared with conventional SB-CNTFETs.

The rest of this Letter is organised as follows: a brief review of SB-CNTFET and modified SB-CNTFET is discussed in Section 2. Simulation methodology of the modified SB-CNTFET is discussed in Section 3. In Section 4, two lightly doped drain (LDD) structures are presented. The discussion about the proposed transistors and the comparisons with other CNTFET structures have been presented in Section 5. This Letter is concluded in Section 6.

2. Modified SB-CNTFET: The schematics of the conventional SB_CNTFET and the Schottky source and ohmic drain CNTFET (SSOD-CNTFET) are shown in Fig. 1.

As shown in Fig. 1, the gate covers the entire channel and the intrinsic CNT at the source is contacted to a metal electrode. In Fig. 1*a* at both the source and the drain, the CNT–metal interface

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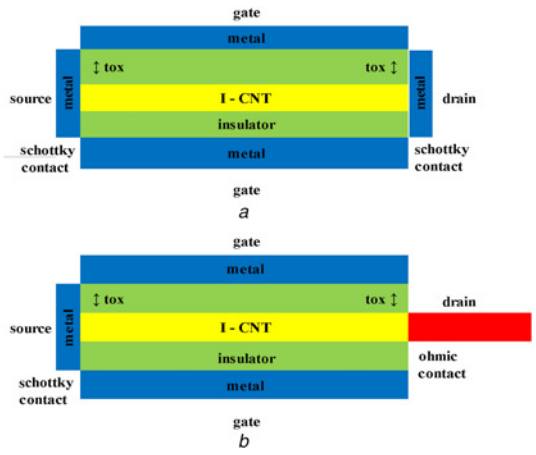

Fig. 1 *Side view of*
a SB_CNTFET
b SSOD-CNTFET, the drain region is heavily doped and an ohmic contact has been formed

forms a Schottky contact, whereas in Fig. 1*b*, at the drain, the CNT has been doped heavily (N-type) to form an ohmic drain contact. The oxide is 1.5 nm thick HfO_2 ($k = 16$), the CNT is a zigzag (13, 0) with a diameter of about 1 nm and a bandgap about 0.8 eV. The gate work function is assumed to be 4 eV and a zero SB height at the source has been assumed. The channel (gate) length (L_{ch}) is 30 nm. Fig. 2 shows the energy band diagram of the CNTFETs. In Fig. 2*a*, the SB-CNTFET SB at source has been shown. Since the drain voltage equals the gate voltage, the potential barrier at the drain has been diminished. In Fig. 2*b*, the CNT is contacted to a heavily doped region and an ohmic drain has been formed in SSOD-CNTFET. It is clear from the energy band diagram shown in Fig. 2 that there is a Schottky contact at the source side and an ohmic contact at the drain side of SSOD-CNTFET. The doping of the drain region for SSOD-CNTFET is 1.5 nm^{-1}. As illustrated in Fig. 2, the current

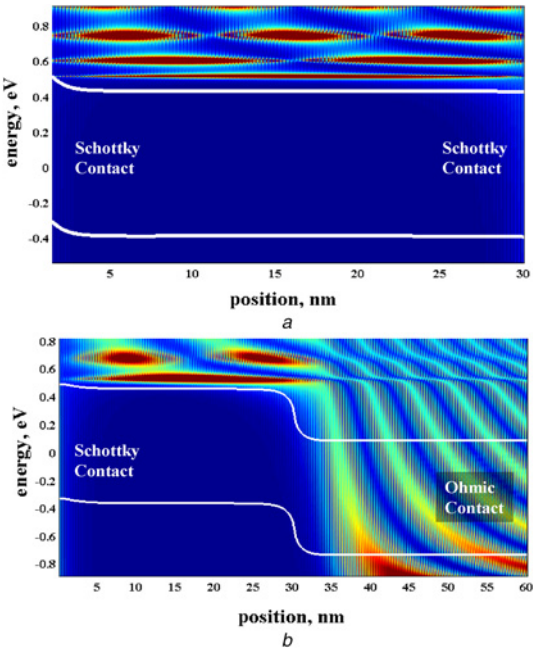

Fig. 2 *Energy diagram versus position of*
a SB-CNTFET
b SSOD-CNTFET at $V_D = V_G = 0.4$ V with a channel length of $L_{ch} = 30$ nm

of the SB-CNTFET is due to the transport of the electrons through the conduction band and holes through the valence band.

Application of a heavily doped region at the drain renders the current made up of majority carriers (electrons). The larger mobility of the electrons provides improvements in the device behaviour. Different colours represent the number of electrons per unit energy (dn/dE) along the CNT axis and the solid lines indicate the band diagram of the first subband.

The simulation results for these two CNTFETs will be compared with that of the proposed structures in the following sections.

3. Simulation methodology: Schrödinger and Poisson equations have been solved self-consistently. Finite difference scheme has been used to convert the Schrödinger and Poisson equations into matrices. The density of states and charge density have been calculated based on the non-equilibrium Green's function (NEGF) method. Our model, as well as the basic device effects, is capable of taking into account the band-to-band tunnelling (BTBT), potential barriers and fringing fields. Newton–Raphson method has been used to solve the Poisson equation.

The 2D cylindrical Poisson equation has been solved to obtain the electrostatic potential $V(r, z)$ [14, 15]

$$\frac{\partial^2 V}{\partial r^2} + \frac{1}{r}\frac{\partial V}{\partial r} + \frac{\partial^2 V}{\partial z^2} = -\frac{q}{\varepsilon}\frac{1}{2\pi R}\left(p(z) - n(z) - N_A + N_D\right) \quad (1)$$

where R is the diameter of CNT; $p(z)$ and $n(z)$ are the 1D hole and electron densities along the CNT; and N_A and N_D are the prescribed doping densities.

The Poisson equation reduces to the Laplace equation inside the CNT and the gate insulator (oxide) regions, except for the CNT/oxide interface because charges exist only at the CNT surface. The electrostatic potential has been obtained by solving 2D Poisson equation on the CNT/oxide interface and Laplace equation elsewhere in the cylindrical coordinate.

The boundary conditions used to solve the Poisson equation for SB_CNTFET are [15]

$$V(r = R_{gate},\ z) = V_{bi} + V_G \quad (2)$$

$$\frac{\partial V}{\partial r}(r = 0,\ z) = 0 \quad (3)$$

$$V(r,\ z = 0) = V_{bi} \quad (4)$$

$$V(r,\ z = L) = V_{bi} + V_D \quad (5)$$

where V_{bi} is the source built-in potential at the interface of the source and the channel (CNT) which is determined by the work function difference between the metallic contact and the semiconducting NT.

Since the potential and charge density are invariant around the NT, the Poisson equation is essentially a 2D problem along the tube (z) and the radial direction (r).

Across the NT surface, there is a discontinuity in ε which requires applying a matching condition as below [15]:

$$\varepsilon_{ins}\left.\frac{\partial V}{\partial r}\right|_{R^+} - \varepsilon_0\left.\frac{\partial V}{\partial r}\right|_{R^-} = -\frac{q(p - n)}{2\pi R\varepsilon_0} \quad (6)$$

Neumann boundary conditions are imposed at the drain of the SSOD-CNTFET. That is the normal component of the electric field at the channel–drain interface is zero. This boundary condition satisfies the charge neutrality at the contact regions. For other boundaries, without electrode contacts, the same zero electric field conditions have been assumed.

The Green function has been calculated from

$$G(E) = \left[(E + 0^{+})I - H - \Sigma_1 - \Sigma_2\right]^{-1} \tag{7}$$

where E is the energy; $\boldsymbol{H}$ is Hamiltonian matrix; and Σ_1 and Σ_2 are self-energies. More details of our simulation method have been described in [16].

We repeat the steps of solving the coupled 2D Poisson and NEGF equations until a self-consistent potential is obtained. Once self-consistency is achieved, the drain current for coherent transport under a bias voltage V can be calculated by means of the Landauer–Buttiker formula [16, 17]

$$I = \frac{4q}{h}\sum_{n}\int_{E} T(E)\left[f_{\mathrm{s}}(E) - f_{\mathrm{d}}\left(E,\ V_{\mathrm{DS}}\right)\right] \mathrm{d}E \tag{8}$$

where q is the electron charge, $f_{\mathrm{S}}(E)$ and f_{D} (E, V_{DS}) are the Fermi distribution functions at the source and drain sides and $T(E)$ is the source-to-drain transmission. The summation is over the subbands contributing to the current. The experience shows that if the integration interval would be from a limited value below the valence band to a limited value above the conduction band, it provides precise results. This value can be about 0.2–0.4 eV.

The intrinsic cut-off frequency of the transistor is computed by [18, 19]

$$f_{\mathrm{T}} = \frac{1}{2\pi}\frac{g_{\mathrm{m}}}{C_{\mathrm{g}}} \tag{9}$$

where the g_{m} is the transconductance

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{gs}}} \tag{10}$$

The intrinsic switching delay (τ) is given by [20]

$$\tau = C_{\mathrm{g}} \cdot V_{\mathrm{DD}}/I_{\mathrm{on}} \tag{11}$$

where C_{g} is

$$C_{\mathrm{g}} = \frac{\partial Q_{\mathrm{g}}}{\partial V_{\mathrm{gs}}} \tag{12}$$

4. LDD SB-CNTFET: Schematic diagram of the designed structures of LDD SB-CNTFETs is shown in Fig. 3. A(13, 0) CNT has been considered as the channel with a length of $L_{\mathrm{ch}} = 30$ nm and the length of the LDD region is $L_{\mathrm{d}} = 30$ nm. As shown in Fig. 3, the intrinsic CNT channel ends in N-type regions in the drain. DLDD-CNTFET has two doped regions in the drain, where the length and the impurity concentration of the regions are as follows: $N_{\mathrm{d1}} = 1.5\ \mathrm{nm}^{-1}$, $N_{\mathrm{d2}} = 0.15\ \mathrm{nm}^{-1}$ and $L_{\mathrm{d1}} = L_{\mathrm{d2}} = 15$ nm. The triple LDD-CNTFET (TLDD-CNTFET) has three-doped regions, where $N_{\mathrm{d3}} = 0.15\ \mathrm{nm}^{-1}$, $N_{\mathrm{d4}} = 0.3\ \mathrm{nm}^{-1}$, $N_{\mathrm{d5}} = 0.15\ \mathrm{nm}^{-1}$ and $L_{\mathrm{d3}} = L_{\mathrm{d4}} = L_{\mathrm{d5}} = 10$ nm.

Energy versus position of two LDD structures are shown in Fig. 4.

As shown in Fig. 4, the shape of the energy bands near the drain are severely dependent on the doping. The drain side in DLDD_CNTFET renders a severe variation in the energies, so that near the heavily doped region the valence band and the conduction band both exist at the same energies and this leads to the BTBT. We will discuss the BTBT in the next section and show that it is responsible for the leakage current of the device. On the other hand, the energies of TLDD-CNTFET changes slowly and conduction and valence band do not overlap at the same energies.

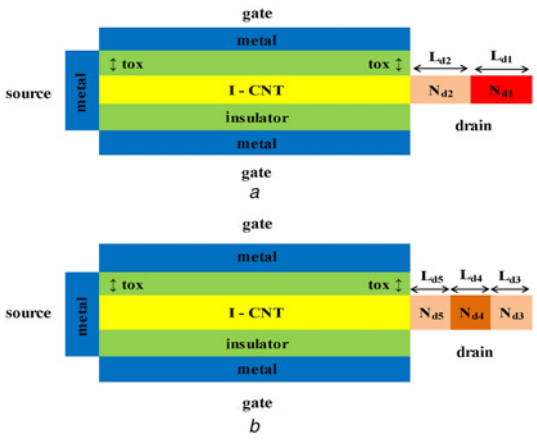

Fig. 3 *Side view of*
a DLDD-CNTFET with two drain regions
b TLDD-CNTFET with three drain regions

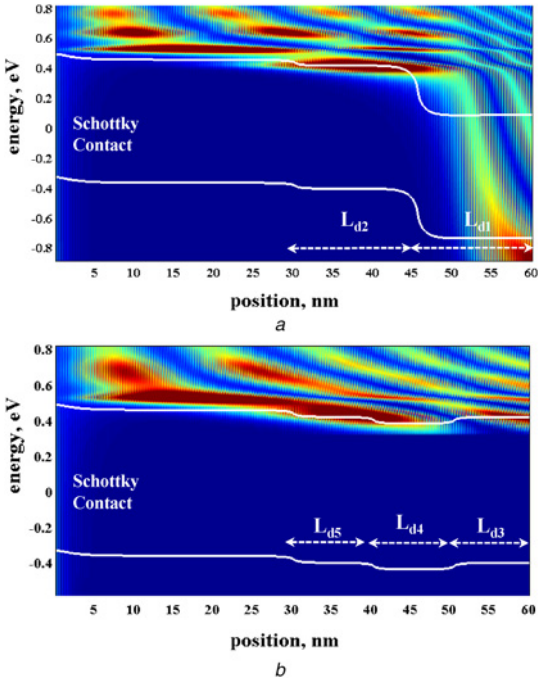

Fig. 4 *Energy bands versus position for*
a DLDD-CNTFET
b TLDD-CNTFET at $V_{\mathrm{D}} = V_{\mathrm{G}} = 0.4$ V and $L_{\mathrm{ch}} = L_{\mathrm{D}} = 30$ nm

5. Results and discussion: In this part of this Letter, the dc and ac performances of the CNTFETs have been compared and discussed. On-current, off-current, on–off ratio, g_{m}, SS, delay, DIBL and cut-off frequency. To show the efficiency of the proposed CNTFET design, comparisons have been made among four CNTFET structures at different channel lengths and gate voltage. The variations of off-state current, on-state current and on–off-current ratio versus the gate length have been plotted in Fig. 5.

In Fig. 5, it is observed that among the designed structures, the TLDD-CNTFET has the largest on-current and the lowest off-current. This is because the TLDD structure suppresses the ambipolar behaviour of the SB-CNTFET by eliminating the hole tunnelling current and the BTBT current and thus the off-current is reduced. Fig. 5*b* shows the on-state current. The TLDD-CNTFET produced the largest on-current. It is noted that the on-state current (I_{on}) of four structures do not have significant variations with the change in the channel length. The reason is that the transport of the

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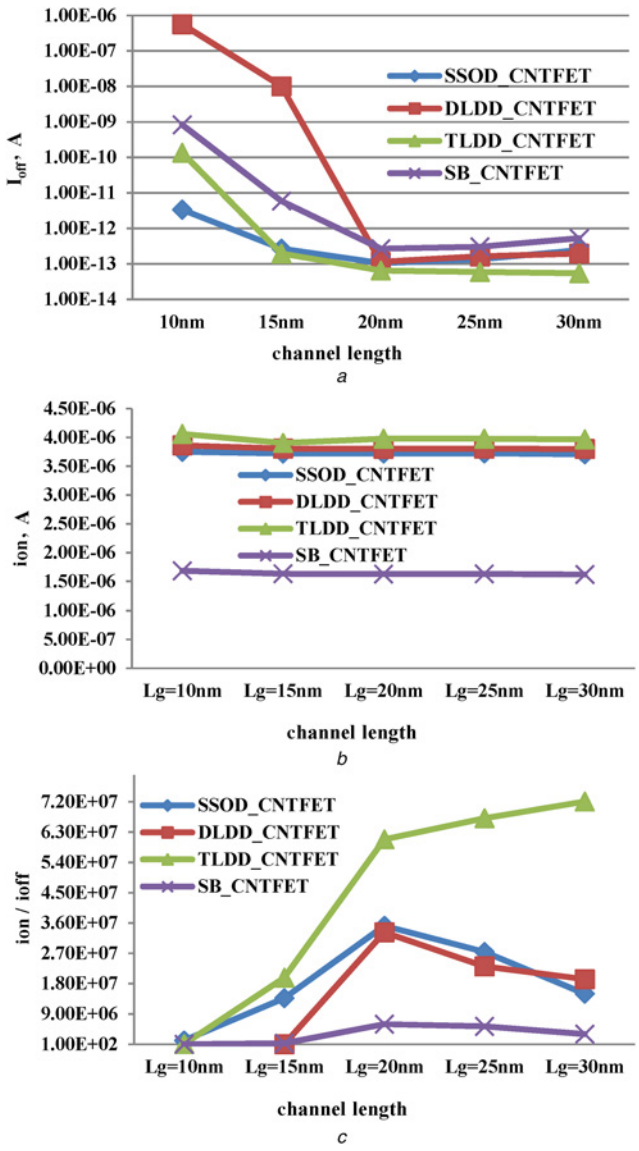


Fig. 5 *Variations of*
a I_{off}
b I_{on}
c I_{on}/I_{off} of four structures of CNTFETs with gate length at $V_D = 0.5$ V

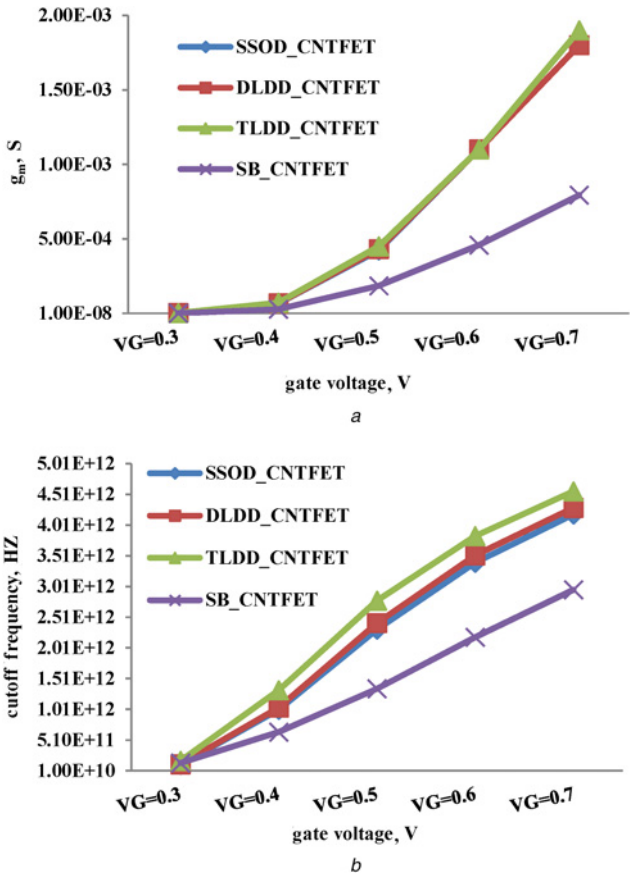


Fig. 6 *Variations of*
a g_m
b Cut-off frequency with gate voltage at $V_D = 0.5$ V for $L_{ch} = L_d = 30$ nm

electrons in the channel is ballistic and the main mechanism of the current flow is the tunnelling of the electrons through the SB at the CNT–metal interface at the source. The amount of the tunnelling current depends directly on the gate voltage, which can narrow the potential barrier width and increase the tunnelling current. The on–off-current ratios of the transistors have been compared in Fig. 5*c*. In Fig. 5*c*, the TLDD structure exhibits larger I_{on}/I_{off} ratio. This had been expected from Figs. 5*a* and *b* since TLDD has the largest on-current and the lowest off-current.

The improved on–off ratio of the TLDD-CNTFET is mostly due to its diminished off-current. This verifies that by controlling the energy bands variations near the drain using triple-doped regions, we succeeded in the elimination of the BTBT at the drain and thus reduction of the off-current. The transconductance and cut-off frequency of the devices versus the gate voltage is shown in Fig. 6. The calculations showed that the change in the drain current relative to the change in the gate voltage has been increased for larger gate voltages. This leads to the increase of the g_m with gate voltage for all devices. As shown in Fig. 6*a*, application of multiple-doped regions could increase the g_m, which means that the gate in the proposed designs has a stronger control over the channel. This has been accomplished by getting rid of the SB at the drain in the new structures. From Fig. 6*b*, we found out that the intrinsic cut-off frequency keeps increasing as the gate voltage increases and the f_T of TLDD-CNTFET is greater than those of other devices. The observed increase in the f_T of TLDD-CNTFET could be attributed to higher-average electron velocity, the improved g_m and the reduced gate capacitance. The added lightly doped regions modify the electric field lines between the gate and the drain contacts, so that the intrinsic gate capacitance and the fringing capacitances decline and this, in turn, leads to a larger f_T.

The simulated intrinsic cut-off frequencies of conventional SB-CNTFET, SSOD-CNTFET, DLDD-CNTFET and TLDD-CNTFET at $L_{ch} = L_d = 30$ nm and $V_G = 0.7$ V are about 0.84, 4.18, 4.29 and 4.56 THz, respectively.

The effects of the channel length on the transconductance and the cut-off frequency have been calculated at 0.5 V gate and drain voltages as shown in Fig. 7. It is observed that the longer the channel length, the lower the cut-off frequency. The g_m is an approximately constant for all structures relative to the channel length and exhibits almost the same manner as the on-current.

From the data in Fig. 7*a*, it is apparent that the transconductances of the LDD structures of TLDD are significantly larger than SB-CNTFET. Interestingly, the g_m for TLDD-CNTFET is better than DLDD-CNTFET and SSOD as well.

Fig. 7*b* illustrates that the intrinsic cut-off frequency keeps decreasing approximately as the channel length varies from 10 to 30 nm. Simulation results show that the TLDD-CNTFET has the best high-frequency performance among all the studied transistors. The simulated intrinsic cut-off frequencies of TLDD, DLDD, SSOD and SB_CNTFET at $L_{ch} = 30$ nm is about 1.91, 1.65, 1.58 and 0.9 THz, respectively.

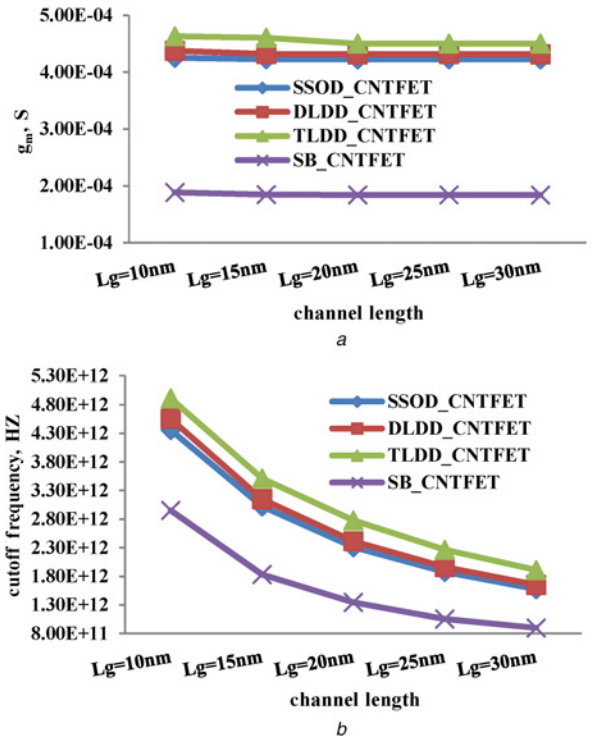


Fig. 7 *Variations of*
a g_m
b Cut-off frequency with channel length at $V_G = V_D = 0.5$ V

Fig. 8 shows the SS of the devices versus the drain current. The SS has been calculated based on the below equation at the subthreshold region of the $I_D - V_{GS}$ characteristic at $V_D = 0.5$ V:

$$SS = \frac{\Delta V_{gs}}{\Delta(\log I_d)} \text{ mV/dec} \tag{13}$$

As shown in Fig. 8, it is notable that the proposed designs for the drain region have been successful in improving the SS. It is because of the unipolar characteristics of the transistors which have been provided by eliminating the hole tunnelling current. The DLDD, TLDD and SSOD-CNTFETs have subthreshold swings much lower than that of the SB_CNTFET structure. The SS for the TLDD is near the optimum value for SS and is the lowest SS among all the devices.

Another important parameter of the transistor is the intrinsic switching time delay (τ) which is defined as

$$\tau = \frac{(Q_{on} - Q_{off})}{I_{on}} \tag{14}$$

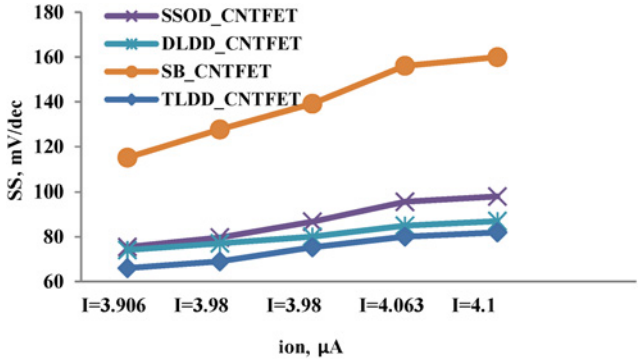


Fig. 8 *Variation of SS versus* I_{on} *at* $V_D = 0.5$ *V*

where the Q_{on} and Q_{off} are the CNT charges in the on- and off-state regimes. We evaluated this parameter versus channel length and gate voltage for the four device structures.

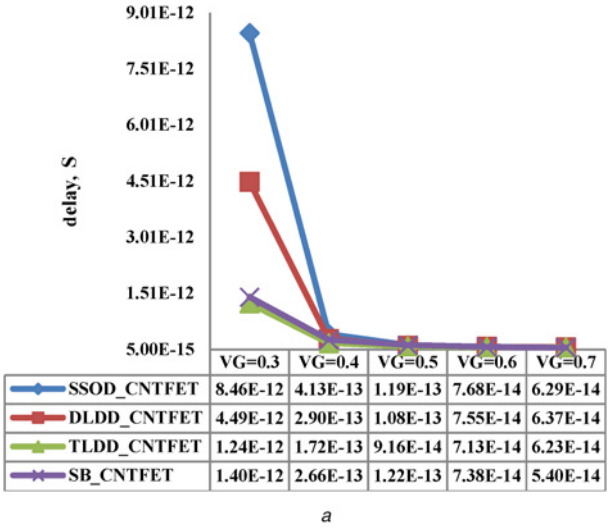
Fig. 9 illustrates and compares the variations of intrinsic switching time delay with gate voltage (at $L_{ch} = 30$ nm) and channel length (at $V_G = V_D = 0.5$ V for the on-state). As shown in Fig. 9 for the channel lengths between 15 and 30 nm, the TLDD-CNTFET has a lower switching time delay than other structures. The calculated intrinsic switching time delays of TLDD, DLDD, SSOD and SB_CNTFET at $V_G = 0.5$ V are about 91, 108, 119 and 122 fs, respectively, and at $V_G = 0.6$ V is about 71, 75, 77 and 74 fs, respectively.

According to the calculated switching time delay, the TLDD structure is a faster device and can be a good candidate for high-speed circuits.

In nanoscale transistors, the drain can interfere with controlling the channel charge, which would otherwise be controlled only by the gate. As the channel length scales down in short-channel transistors, the drain voltage can interact with the source/channel junction and lower the potential barrier. This means that the electrons are injected into the channel without the gate permission and the gate has no longer any control over the drain current. DIBL is the parameter that measures this problem as below:

$$\text{DIBL} = \frac{\Delta V_{th}}{\Delta V_d} \text{ mV/V} \tag{15}$$

which means that DIBL is defined as the variations of the threshold voltage in response to the variations of the drain voltage. Fig. 10



	VG=0.3	VG=0.4	VG=0.5	VG=0.6	VG=0.7
SSOD_CNTFET	8.46E-12	4.13E-13	1.19E-13	7.68E-14	6.29E-14
DLDD_CNTFET	4.49E-12	2.90E-13	1.08E-13	7.55E-14	6.37E-14
TLDD_CNTFET	1.24E-12	1.72E-13	9.16E-14	7.13E-14	6.23E-14
SB_CNTFET	1.40E-12	2.66E-13	1.22E-13	7.38E-14	5.40E-14

a

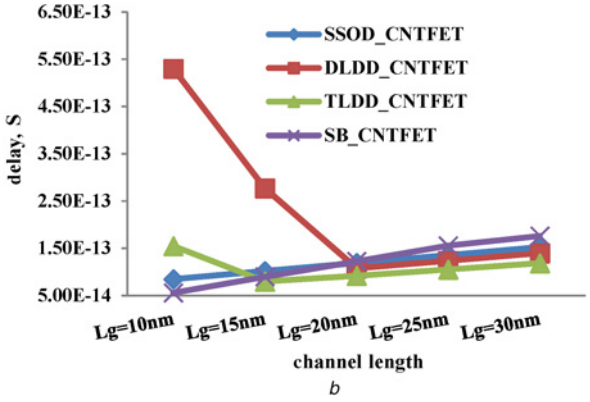


Fig. 9 *Variation of delay with the*
a Gate voltage at $V_D = 0.4$ V, $L_{ch} = 30$ nm
b Channel length at $V_D = V_G = 0.5$ V

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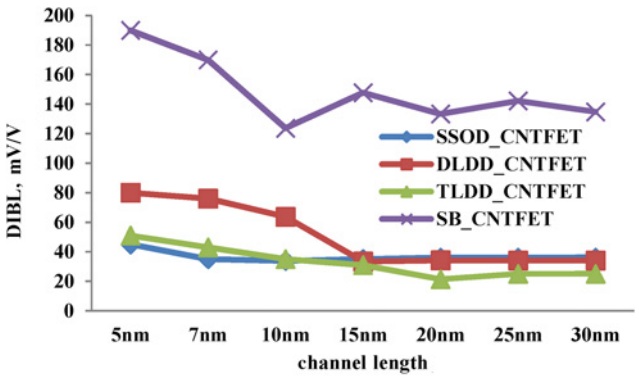

Fig. 10 *Variation of DIBL with channel length at $V_D = 0.5$ V*

illustrates and compares the DIBL (mV/V) versus channel length (at $V_D = 0.5$ V) for the CNTFETs.

As shown in Fig. 10, the proposed designs could suppress the SCEs considerably and the DIBL has become smaller than the SB-CNTFET. Again the TLDD-CNTFET has a lower DIBL than other structures. We shall here, therefore, introduce TLDD-CNTFET to the researchers note as a design with superior performance.

6. Conclusion: The behaviour of nanoscale SB-CNTFET with Schottky–Ohmic source–drain contacts was theoretically studied with a quantum kinetic model. The electrical characteristics of a novel nanoscale SB_CNTFET with Schottky contact at the source and triple lightly doped regions at the drain were investigated. The appropriate design for lightly doped regions could modify the energy bands and in turn the transistor characteristics. Results revealed that compared with the other structures, TLDD-CNTFET structure exhibited significant improved dc and ac performances. The advantages of the TLDD design is the diminished leakage current. A larger on–off-current ratio and transconductance, high-frequency performance and lower delay, SS and DIBL than other SB_CNTFET structures. The proposed CNTFET is a new structure satisfying a well-behaved nanotransistor requirements defined by device designers.

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