

Double trenches LDMOS with trapezoidal gate

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A novel double trenches lateral double diffused metal oxide semiconductor with trapezoidal gate (TGDT LDMOS) is proposed. One feature of the device is that two dielectric trenches which are equivalent to two field plates are introduced in the drift region. The two dielectric trenches not only modulate the body electric field to improve the breakdown voltage (BV) of the device but also assist to deplete the drift region to reduce the specific on-resistance ($R_{on,sp}$). The other feature is the presence of the trapezoidal gate which increases the gate oxide thickness to reduce the capacitance of gate and drain (C_{GD}). Thereby the charge between the gate and drain (Q_{GD}) is reduced, so that the conduction loss of the device is decreased. Compared with the conventional LDMOS with trapezoidal gate and the single trench LDMOS with trapezoidal gate, the figure of merit ($FOM = BV^2/R_{on,sp}$) of the TGDT LDMOS is increased by 112.5 and 54.5%, respectively. Compared with the conventional double trenches LDMOS with rectangle gate, the FOM is similar, but the Q_{GD} is reduced by 45.7%. Simultaneously, the feasible process steps of the TGDT LDMOS are given in this work.

1. Introduction: The power semiconductor device is a kind of microelectronic device which can be used to deal with the voltage and current. There are two developing directions of the power semiconductor device. The first direction is a large power device which means that it requires a large breakdown voltage (BV) and a lower specific on-resistance ($R_{on,sp}$) [1–4]. Due to the presence of a ‘silicon limit’ problem, which exists between the $R_{on,sp}$ and BV, the development of the power device is limited [5, 6]. Many device structures [7–10] have been improved by the researchers to alleviate the ‘silicon limit’. The second direction is lower on-resistance and faster switching speed (smaller gate capacitance C_g or gate charge Q_g) [11, 12], which requires smaller $R_{on,sp} \times Q_{GD,sp}$ [13, 14]. When we research the switching speed of device, we will consider the rates of the charge accumulation and depletion of the gate oxide layer. The charge of drain and gate (Q_{GD}) is the main part of the gate conduction charge. It is used to measure the speed of gate drive and the size of power loss of different devices. As the Q_{GD} and C_{GD} of [15]

$$Q_{GD} = \int_{V_{ON}}^{V_{DS}} C_{GD}(V_D) dV_D, \quad (1)$$

$$C_{GD} = \frac{\epsilon S}{d}, \quad (2)$$

we can reduce the C_{GD} to Q_{GD} . Also, we can increase the thickness of d of the gate oxide layer and reduce the dielectric coefficient ϵ of the gate oxide layer and the contact area S between the gate and the drain to reduce the C_{GD} .

According to these two development directions, a double trenches lateral double diffused metal oxide semiconductor with trapezoidal gate (TGDT LDMOS) is proposed in this Letter. Confirmed by MEDICI simulation and some physical models, such as AUGER, CONMOB, FLDMOB, CONSRH etc. One feature of the TGDT LDMOS is to using two dielectric trenches to assist depleting the drift region. The BV is improved. So that the device obtains a high figure of merit ($FOM = BV^2/R_{on,sp}$). The other feature is that the thickness of the gate oxide layer (d) of the trapezoidal gate of the TGDF LDMOS is thicker than that of the rectangular gate of the RGDF LDMOS. Therefore, the capacitance between the drain and gate (C_{GD}) of the trapezoidal gate

is less than that of the rectangular gate. Thereby the Q_{GD} is reduced to cut down the conduction loss.

2. Structure and mechanism: Compared with the conventional lateral double diffused metal oxide semiconductor with trapezoidal gate (TG LDMOS) in Fig. 1a, the conventional single trench lateral double diffused metal oxide semiconductor with trapezoidal gate (TGST LDMOS) in Fig. 1b adds a dielectric trench in the upper part of the drift region like trench1. The dielectric trench1 works as a field plate to modulate the body electric field and assist to deplete the drift region. So the BV is increased and $R_{on,sp}$ is reduced. At the bottom of the TGDT LDMOS drift region in Fig. 1d, the other dielectric trench2 is introduced to modulate body electric field and introduce the electric field spike at the left side dielectric trench (point A). The electric field spikes can improve the BV of the device. Compared with the conventional double trenches lateral double diffused metal oxide semiconductor with rectangle gate (RGDT LDMOS) in Fig. 1c, the trapezoidal gate is used in the TGDT LDMOS. It increases the thickness of the gate oxide layer, so the C_{GD} is reduced and the Q_{GD} is lowered.

3. Results and discussion: Compare the basic device parameters (BV, $R_{on,sp}$, FOM and Q_{GD}) of the TGDT LDMOS, TGST LDMOS and TG LDMOS with TGDT LDMOS. From the simulation results, we can see the performance of TGDT LDMOS is better than the other structures’. The device simulation parameters of the TGDT LDMOS are shown in Table 1.

Fig. 2 shows the equipotential distributions of the four devices. Compared with the conventional TG LDMOS, a dielectric trench is added into the upper part of the TGST LDMOS drift region to modulate the body electric field and assist to deplete the drift region. The concentration of the drift region is increased from 7×10^{15} to $11 \times 10^{15} \text{ cm}^{-3}$. The $R_{on,sp}$ is decreased from 0.9 to 0.78 mΩ cm². The FOM is enhanced by 33.3%. Compared with the conventional TGST LDMOS, the other dielectric trench is introduced at the bottom of the TGDT LDMOS drift region to assist depleting the drift region further. From the red rectangle in Fig. 2, we can see that the equipotential contours of the RGDT LDMOS and TGDT LDMOS near the drain are more intensive and uniform than the TG LDMOS and TGST LDMOS. The BV of TGDT LDMOS is 119.3 V. Compared with the TGST

LDMOS and TG LDMOS, the BV of TGDT LDMOS enhances by 54.9 and 65.5%, respectively. Compared with the RGDT LDMOS, the BV is similar.

Fig. 3 shows the distributions of the surface electric field of the four devices at $y = 0.01 \mu\text{m}$ or the lines MM' in Fig. 2. The dielectric trench is added into the drift region to assist depleting the drift region and increase the electrical field spikes at the drain of the

device. So the surface electric field distributions of the TGDT LDMOS and RGDT LDMOS are more uniform. Thereby the lateral BV of the device is increased. Fig. 4 shows the distributions of the body electric field of the four devices at $y = 2.09 \mu\text{m}$ or the lines NN' in Fig. 2. From the point A of Figs. 2c and d, we can see that electric field spikes are introduced at the left edge of the dielectric trench2. The electric field at the surface of trench2 of the TGDT LDMOS increases from $16.4 \text{ V}/\mu\text{m}$ of TG LDMOS to $55.7 \text{ V}/\mu\text{m}$.

BV, $R_{\text{on,sp}}$ and FOM of TGDT LDMOS versus the N_d is shown in Fig. 5. With the increasing of drift concentration N_d , the BV is increased firstly and then decreased, $R_{\text{on,sp}}$ is reduced continuously. The biggest FOM is 11.9 MW cm^{-2} , when the N_d is $8 \times 10^{15} \text{ cm}^{-3}$. The BV and $R_{\text{on,sp}}$ and FOM of TGDT LDMOS versus the depth t_1 are shown in Fig. 6a. When N_d is $8 \times 10^{15} \text{ cm}^{-3}$ and L_1 is $1.6 \mu\text{m}$, as the depth t_1 increases, the $R_{\text{on,sp}}$ of the device is increasing. That is because with the depth t_1 increases, the drift region is narrowed, the $R_{\text{on,sp}}$ of the device increases. When the t_1 is $0.9 \mu\text{m}$, the values of the BV and FOM of the TGDT LDMOS are better, $R_{\text{on,sp}}$ is smaller. Fig. 6b shows the BV, $R_{\text{on,sp}}$ and FOM of the TGDT LDMOS versus L_1 . As the width L_1 increases, the region on the left side of the trench2 is decreasing, so the R_{on} of that region is increasing. The $R_{\text{on,sp}}$ is increasing. When L_1 is $1.6 \mu\text{m}$, the compromise of the BV and $R_{\text{on,sp}}$ is the best.

Compared with the rectangular gate of the RGDF LDMOS, the trapezoidal gate of the TGDF LDMOS is introduced to increase the thickness of the gate oxide layer (d). The capacitance between the drain and gate (C_{GD}) of the trapezoidal gate is less than that of the rectangular gate. The Q_{GD} of TGDF LDMOS is smaller than the Q_{GD} of the RGDF LDMOS. We can obtain the gate charge curves and the Q_{GD} of different devices by the simulated test circuit (shown in the inset figure of Fig. 7) with Medici software [16]. The Q_{GD} of TGDT LDMOS and TG LDMOS is least. Compared with the RGDT LDMOS, the Q_{GD} of TGDT LDMOS is reduced by 45.7%. The drain voltage diversifications of the four devices versus time are shown in Fig. 8, and C_{DG} and Q_{GD} are shown in the inset figure of Fig. 8. From the charge of the drain and gate (Q_{GD}) calculation formula (1) and capacitance formula (2), we can know that the Q_{GD} of TGDF LDMOS is smaller than the Q_{GD} of the RGDF LDMOS. The time of Q_{GD} is corresponded to the time of the drain voltage reducing to the turn-on voltage. The time of the drain voltage drops to the open voltage of TGDT LDMOS is 65.8 ns , and the time of RGDT LDMOS is 121.1 ns . So the Q_{GD} of the TGDT LDMOS is least.

Fig. 9 shows the feasible main process steps to fabricate TGDT LDMOS: etch the silicon drift region and deposit SiO_2 to form the trench2 in Fig. 9a; bond the p-substrate with a thermally

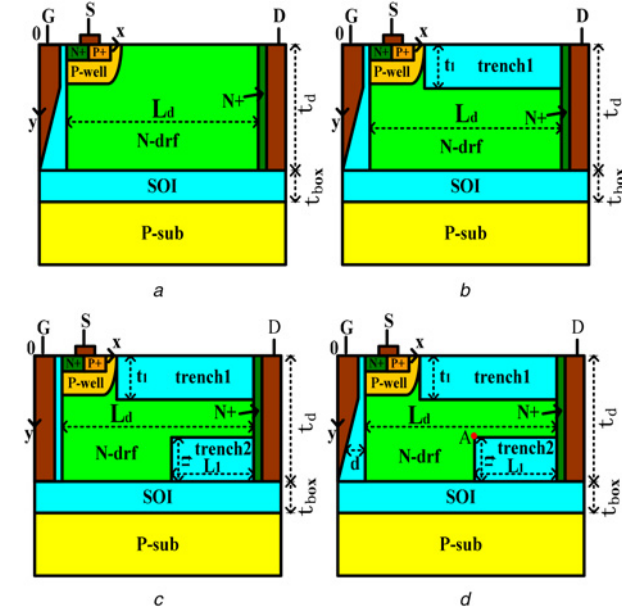


Fig. 1 Structures of
a TG LDMOS
b TGST LDMOS
c RGDT LDMOS
d TGDT LDMOS

Table 1 Device parameters of the TGDT LDMOS

Device parameters	Value	Unit
length of drift region, L_d	6	μm
thickness of drift region, t_d	3	μm
thickness of buried oxide layer, t_{box}	0.5	μm
substrate concentration, $N_{\text{sub}} (\times 10^{14})$	5	cm^{-3}
N-drift region concentration, $N_d (\times 10^{15})$	6–10	cm^{-3}
thickness of trench1 and trench2, t_1	0.7–1.1	μm
length of trench2, L_1	1.2–2.2	μm

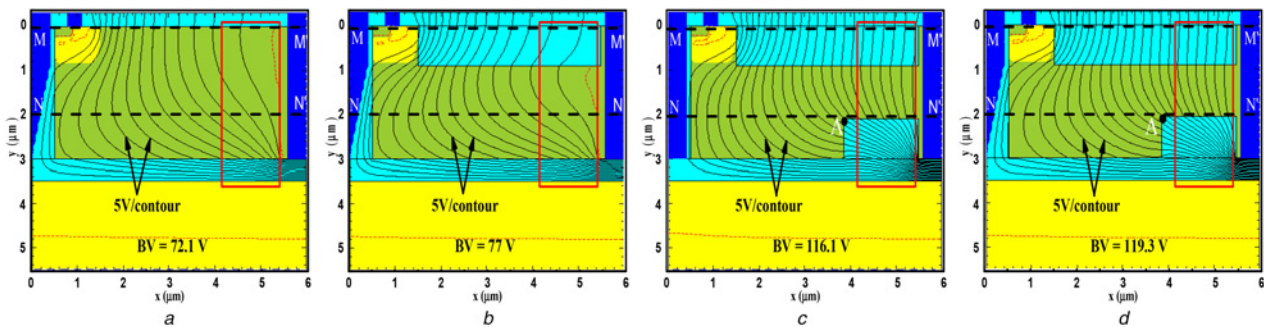


Fig. 2 Equipotential distributions of
a TG LDMOS
b TGST LDMOS
c RGDT LDMOS
d TGDT LDMOS

grown SiO₂ layer and the drift region in Fig. 9b; etch the silicon drift region to form the rectangular gate oxide trench, drain trench and trench1 in Fig. 9c; implant phosphor by inclination θ to form N⁺ active region at the drain in Fig. 9d; deposit oxide to form gate oxide trench and trench1 in Fig. 9e; implant boron to form the regions of p-body and P⁺ and phosphor to form the region of N⁺ in Fig. 9f, they are consistent with the conventional processes. Etch the oxide to form the trapezoidal gate trench in Fig. 9g; deposit metal to form the electrodes of source, gate and

drain in Fig. 9h. Therefore, the production processes of TGDT LDMOS are similar to the conventional processes, without adding additional process costs.

The device parameters of the four devices are shown in Table 2. TGDT LDMOS not only has a large BV and FOM, but also obtains the minimum Q_{GD} . Considering the comprehensive performance parameters of the power devices, the performance of the new structure TGDT LDMOS is better than the conventional structures.

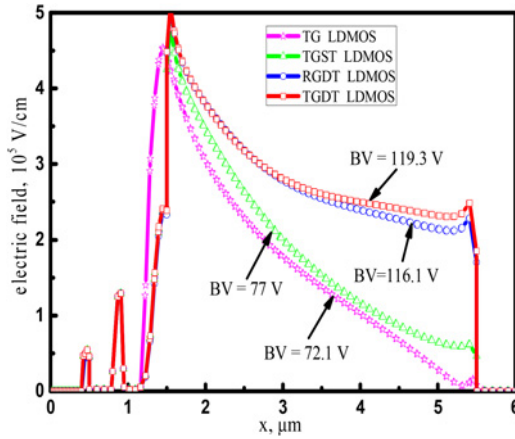


Fig. 3 Surface electric field distributions of four devices at $y = 0.01 \mu\text{m}$

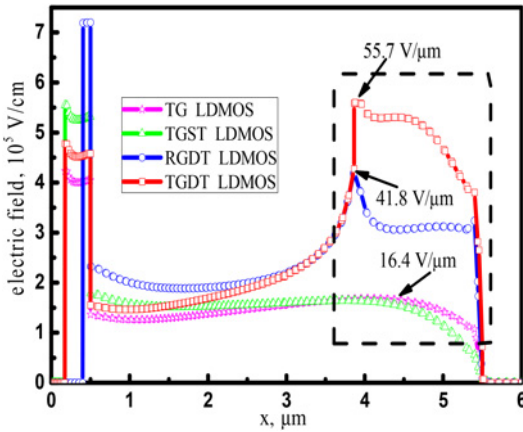


Fig. 4 Body electric field distributions of four devices at $y = 2.09 \mu\text{m}$

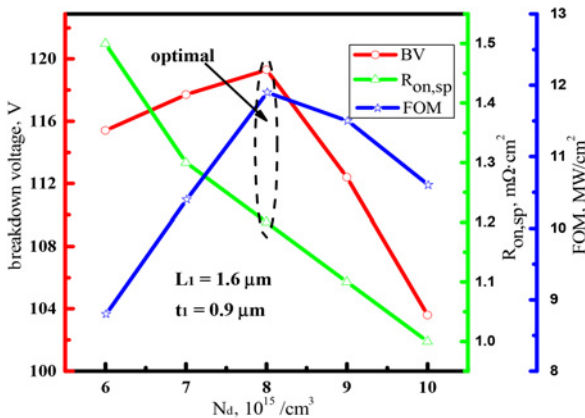


Fig. 5 BV , $R_{on,sp}$ and FOM of TGDT LDMOS versus the N_d when $L_1 = 1.6 \mu\text{m}$ and $t_1 = 0.9 \mu\text{m}$

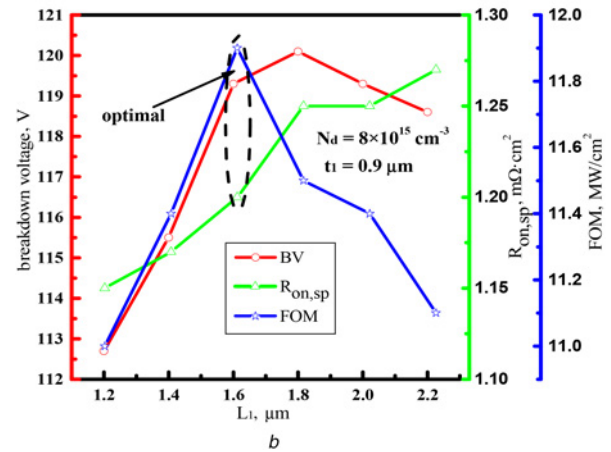
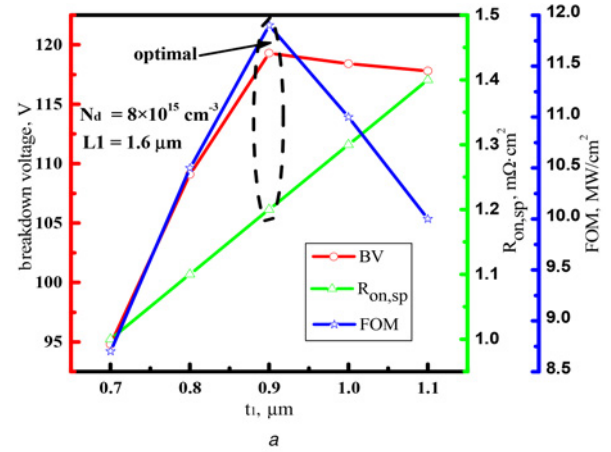


Fig. 6 BV , $R_{on,sp}$ and FOM of TGDT LDMOS versus t_1 and L_1
a When $N_d = 8 \times 10^{15} \text{ cm}^{-3}$ and $L_1 = 1.6 \mu\text{m}$
b When $N_d = 8 \times 10^{15} \text{ cm}^{-3}$ and $t_1 = 0.9 \mu\text{m}$

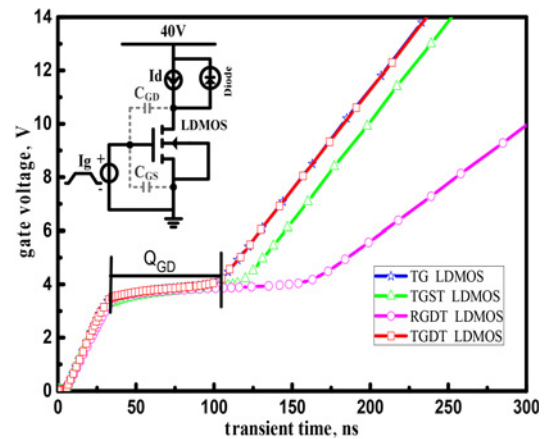


Fig. 7 Simulation of gate charge results of four devices and the simulated test circuit is shown as an inset

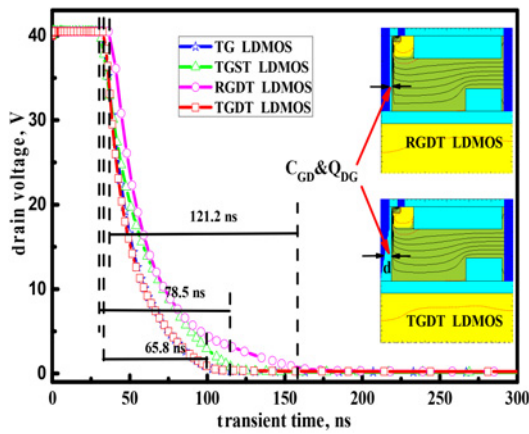


Fig. 8 Drain voltage diversifications of the four devices versus time

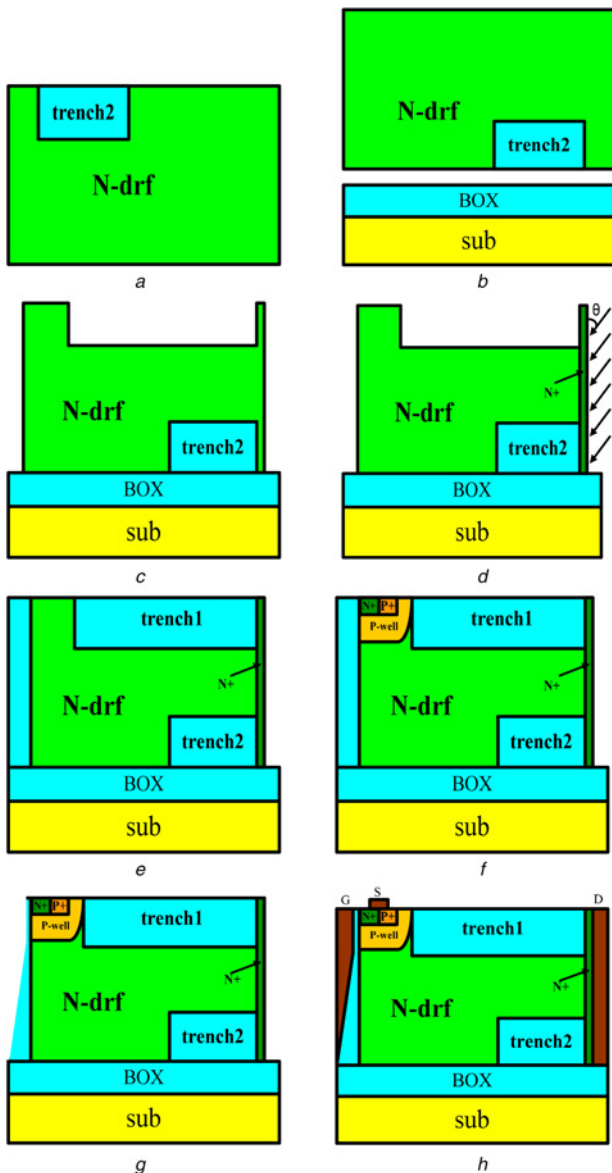


Fig. 9 Feasible main process steps to fabricate a TGD LDMOS

4. Conclusion: We study the parameters (BV, $R_{on,sp}$, FOM and Q_{GD}) of TGD LDMOS by Medici. The BV of TGD LDMOS is 119.3 V, $R_{on,sp}$ is 1.2 m Ω ·cm² and Q_{GD} is 65.8 nC·cm⁻².

Table 2 Device parameters of the four devices

	BV, V	$R_{on,sp}$, m Ω cm ²	FOM, MW cm ⁻²	Q_{GD} , nC cm ⁻²
TG LDMOS	72.1	0.9	5.7	65.8
TGST LDMOS	77	0.78	7.6	78.5
RGDT LDMOS	116.1	1.05	12.8	121.2
TGD LDMOS	119.3	1.2	11.9	65.8

Compared with the conventional TG LDMOS and TGST LDMOS, the FOM enhances by 112.5 and 54.5%, respectively. Compared with the conventional RGDT LDMOS, Q_{GD} reduces by 45.7%. So the performance of TGD LDMOS is better than others' and the process steps are simple.

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