Effect of varying Indium concentration of InGaAs channel on device and circuit performance of nanoscale double gate heterostructure MOSFET

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The detailed numerical analysis is performed to study and evaluate the impact of Indium (In) concentrations of the Indium gallium arsenide (InGaAs) channel on different device performances of InGaAs/In phosphide double gate metal–oxide–semiconductor field-effect transistor using TCAD software. The RF/analogue figures of merits under investigation are transconductance (g_m), transconductance-to-current ratio (g_m/I_d), cut-off frequency (f_T), maximum frequency of oscillations (f_{max}) etc. A cascode amplifier is then designed using the device under study and its voltage transfer characteristics and differential gain are plotted to estimate the device performance in circuits. It is seen that with higher Indium content, the analogue/RF performance of the device significantly improves.

1. Introduction: The continuous requirement of complex integrated and highly dense circuits has led to the aggressive downscaling of the metal–oxide–semiconductor field-effect transistor (MOSFET). However, downscaling (nanoscale) leads to short channel effects which adversely affects the radio-frequency (RF)/analogue performance of the device. To overcome this problem, the new device architecture and material compositions became essential. Double gate MOSFETs have emerged as one of the most promising devices to investigate [1–4]. At the same time, the III–V compound semiconductor materials promised significant improvements over silicon (Si), germanium, and other elemental semiconductors because of their electronic band structure and material properties such as higher electron mobility [5]. The property of indium gallium arsenide (InGaAs) is intermediate between GaAs and InAs depending on the proportion of Ga to In. Researchers already studied that III–V heterostructures are most important materials for n-channel FETs because of its higher mobility [6–11]. Many are working on the implementation of InGaAs and other III–V compound semiconductors as high-mobility channel materials in FETs on Si, so that it can be used for mainstream complementary MOS technology. Recently, it has been demonstrated that higher In mole fraction(x) in $In_xGa_{1-x}As$ influence the performance of the devices and the device performance can be improved by increasing the mole fraction [12–14]. However, to the best of our knowledge, no such work is available in the literature which addressed the circuit application of such devices and analogue/RF performance dependence on its channel composition. Hence, there is a scope of investigation of channel composition of the devices to optimise its performances to use it in analogue circuits for low-power applications.

In this Letter, a simulation study of analogue/RF performance of the device with varying In concentration in channel material is presented. The device architectures and simulation methodology are discussed in Section 2. The detailed results are explained in Section 3. Section 4 summarises the conclusions of the Letter.

2. Device structure and simulation approach: The device under study, i.e. InGaAs/In phosphide (InP) nanoscale heterostructure double gate MOSFET is shown in Fig. 1. The channel of the heterostructure MOSFET is $In_xGa_{1-x}As$ material, where the effect of mole fraction is studied by varying the value of x which indicates the In mole fraction. The InGaAs channel material is considered because of its low electron effective mass and high saturation velocities. On both sides of the channel, two InP barrier layers are used. Length of the channel is 12 nm and the length of the source/drain extension is 2 nm. The InGaAs layer is sandwiched between two InP layers. The InGaAs channel thickness (t_{ch}) is 2 nm and the InP barrier thickness (t_b) is 2 nm. To minimise leakage currents, an oxide with a high-k dielectric Hafnium Dioxide (HfO_2) is used. The device has source/drain doping concentration of 10^{20} cm^{-3}. The channel region is considered as undoped.

The device under study is simulated using a two-dimensional (2D) structure in device simulator SILVACO ATLAS [15]. A 2D numerical simulation using drift-diffusion phenomenon has been performed. Newton numerical method has been used for calculation. The Shockley–Read–Hall carrier generation–recombination model is used in this analysis. Field-dependent mobility model has been considered to model the velocity saturation effect. For carrier statistics, Fermi–Dirac model is chosen. Newton method is used for this analysis. The device model is calibrated with the experimental data available in the literature for accurate analysis [16, 17].

3. Simulation results: Different RF and analogue performance parameters in the form of transconductance (g_m), transconductance-generation factor (g_m/I_d), cut-off frequency (f_T), and maximum oscillation frequency (f_{max}) are studied in this section. Initially, the effect of varying In content in the InGaAs channel is studied by calculating different analogue parameters by varying the composition of the channel material. The mole fractions of In considered for performance analysis are 0.53, 0.58, 0.63, and 0.7 along with InAs and GaAs as the channel material, which represents two extreme conditions. In Fig. 2, the surface potential is plotted as a function of horizontal distance in the channel of the double gate heterostructure MOSFET. It is observed from Fig. 2 that as the In concentration increases, the peak of potential minimum shifts upward with lowering the boundary values.

Fig. 3 shows the plot of conduction current density perpendicular to the channel for different In concentrations. With the increase in In concentration, conduction current density in the channel region increases. A sudden change in conduction current density at the

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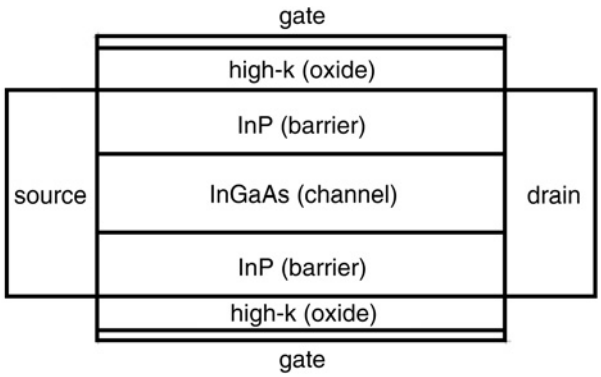

Fig. 1 *Structure of the InGaAs/InP heterostructure DG MOSFET*

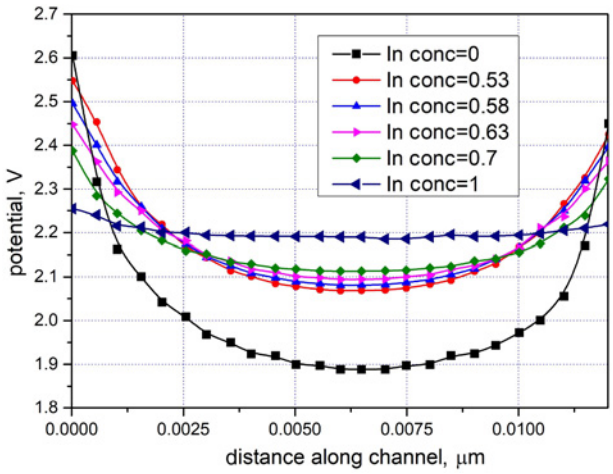

Fig. 2 *Potential profiles along the channel of the DG heterostructure MOSFET at $V_{gs} = 1$ V and $V_{ds} = 1$ V*

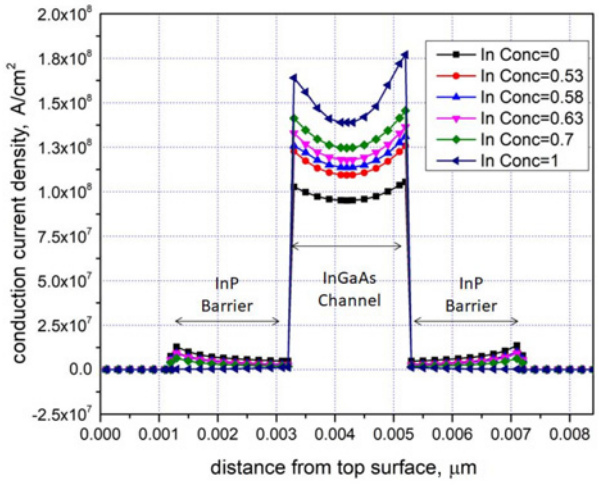

Fig. 3 *Conduction current density perpendicular to the channel at $V_{gs} = 1$ V*

channel and barrier layer interface is also observed. Owing to differences in electron affinity between the barrier and the channel material, a quantum well is formed allowing mobile electrons to migrate into the channel. The band discontinuities of the heterostructure create the rectangular shaped quantum well having confined high-mobility electrons in the channel [18]. As a result of electron confinement, there they reside as a thin, high density sheet of electrons known as a 2D electron gas (2DEG). Owing to these 2DEG, the concentration of free electrons occurs over a very narrow region close to the hetero-interface [19]. The 2DEG stays in InGaAs channel and higher conduction current density occurs in the channel. Moreover, an increase in In content in the $In_xGa_{1-x}As$ channel increases the conduction band offset between the channel and barrier layer, resulting in improved carrier confinement in the channel [20]. The formation of a 2DEG causes the channel to experience an overall increase in electron mobility. Electron mobility characterises how fast an electron is allowed to drift through the InGaAs lattice under the influence of an electric field. Thus, when an electric field, in other words a drain voltage, is applied across source and drain, electrons are driven through the channel.

3.1. Analogue performance: To compare the device performance for varying In mole fraction in InGaAs channel, analogue performance data is calculated and compared with different In concentrations in $In_xGa_{1-x}As$ channel. The mole fractions of In considered for analogue performance analysis are 0, 0.53, 0.58, 0.63, 0.7, and 1 with $V_{ds} = 1$ V and V_{gs} varying from −1 to 2 V. Fig. 4 shows the drain current (I_d) as a function of gate-to-source voltage (V_{gs}) for different mole fractions of In in the channel. It is seen that the drain current increases as the mole fraction of In in the channel increases.

The transconductance of a transistor is the ratio the drain current changes when the gate voltage is changed, using a constant drain voltage. Fig. 5 compares values of transconductance (g_m) as a function of V_{gs} for different mole fractions of In in the channel. This figure reveals that with the increase in mole fraction of the In, transconductance increases considerably. We have observed that both the maximum drain current (I_d) and transconductance (g_m) of the device increase with an increase in the In mole fraction x. This finding matches well with the findings reported by Thathachary *et al.* [21]. The main reason is that with increasing In mole fraction, both the low-field electron mobility and saturation velocity increase because of the decreasing electron effective mass [22]. It is known that effective mass m^* of the electron is inversely proportional to the In content in $In_xGa_{1-x}As$, channel; its mobility increases with increase in In concentrations. Also, the bandgap energy is proportional to the In mole fraction, which means the InGaAs channel with higher In mole fraction requires smaller surface potential (band bending or the Fermi-level movement) to reach the same density of inversion charges. InGaAs is a ternary compound between InAs and GaAs and in order to achieve successful crystal growth without major lattice defects, the channel material should ideally be lattice matched to the underlying InP substrate. Dislocations caused by lattice mismatch adversely affect the electrical characteristics of a device by creating localised states which act as traps for the charge

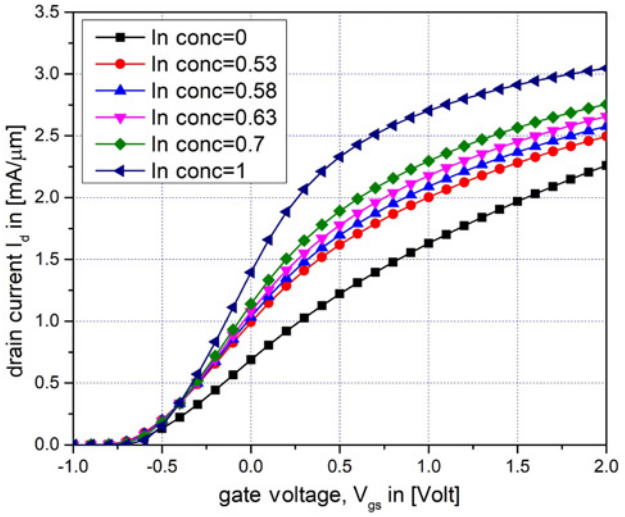

Fig. 4 *Variation of I_d in linear scale as a function of V_{gs} for different In concentrations at $V_{ds} = 1$ V*

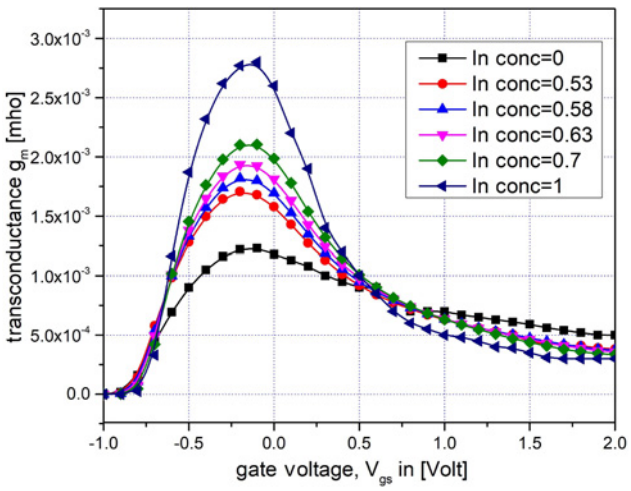

Fig. 5 *Variation of g_m as a function of V_{gs} for different In concentrations at $V_{ds} = 1$ V*

carriers. $In_{0.53}Ga_{0.47}As$ is the alloy whose lattice parameter matches that of InP at 295 K, whereas the $In_{0.75}Ga_{0.25}As$ layer is at the limit of pseudomorphic growth. The lattice constant of $In_xGa_{1-x}As$ becomes smaller than InP for mole fraction lower than 0.53 resulting a tensile strain in the channel. In contrast, the lattice constant of the InGaAs layer becomes larger than InP for an In molar fraction more than 0.53, and the channel is under a compressive strain [23]. This is due to the fact that in the channel under compressive strain, alloy scattering decreases which in turn increases the electron mobility. Therefore, increase in In mole fraction of the channel improves the ON current of the device. Unfortunately, increasing the In concentration in $In_xGa_{1-x}As$ also increases the lattice constant which increases the lattice mismatch with InP layer. Using a buffer layer, crystal growth defects may be reduced, but that degrades the performance of the 2DEG channel. Even though using high In mole fraction in InGaAs channel material is desired for high electron velocity [24], a trade-off in epilayer composition must be made to compromise between high-speed performance and device reliability.

As the transconductance (g_m) of the device expresses the gain given by the device, whereas the drain current (I_d) specifies the power dissipation to achieve the gain, the ratio is regarded as the available gain per unit power dissipation. So, it is targeted in design to have higher g_m/I_d ratio for better analogue performance of the device. Fig. 6 displays a comparison of g_m/I_d as a function

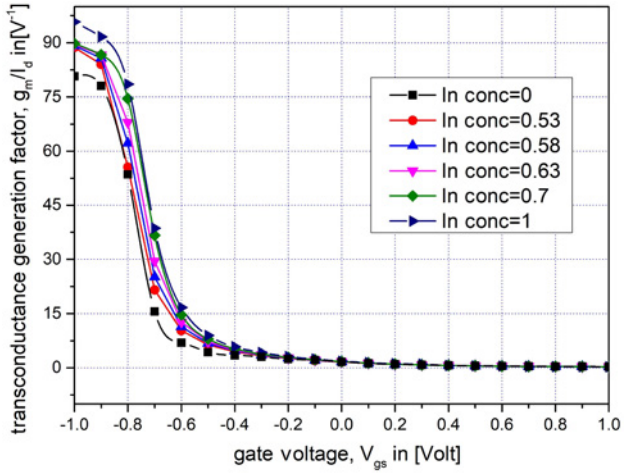

Fig. 6 *Variation of g_m/I_{ds} as a function of V_{gs} for different In concentrations at $V_{ds} = 1$ V*

of V_{gs} for different In contents in the channel. From this figure, it is observed that g_m/I_d does not vary too much with the increase in In content in the channel.

3.2. RF performance: For RF performance analysis, the unity current gain frequency (f_T) and the maximum frequency of oscillation (f_{max}) are considered. The cut-off frequency is defined as the frequency, where the current gain is unity. f_{max} is the frequency at which the maximum power gain = 1. It is defined with its input and output ports conjugate-matched for maximum power transfer. Approximately f_T can be defined as [25]

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \tag{1}$$

where the terms g_m, C_{gs}, and C_{gd} represent the transconductance, the gate-to-source capacitance, and gate-to-drain capacitance, respectively. f_{max} is taken [19] as

$$f_{max} = \frac{g_m}{2\pi C_{gs}\sqrt{4 \times (R_s + R_i + R_g) \times (g_{ds} + g_m(C_{gd}/C_{gs}))}} \tag{2}$$

where R_s, R_g, and R_i are the source, gate, and intrinsic channel resistances, respectively. g_{ds} is the output conductance.

As f_T and f_{max} are related to the gate capacitances of the device, C_{gs} and C_{gd} are extracted from the simulation. Fig. 7 plots the gate capacitance (C_{gs} and C_{gd}) as a function of gate voltage (V_{gs}) for different In concentrations of the channel.

Fig. 8 shows the difference of cut-off frequency (f_T) of the device for different In concentrations in the channel. From Fig. 8, it is observed that the cut-off frequency is increasing with the increase in the percentage of In in the channel. This is due to the improvement in g_m for increasing In mole fraction, as observed in Fig. 5. Fig. 9 plots the maximum oscillation frequency (f_{max}) variation with gate voltage (V_{gs}) for different In concentrations in the channel. From Fig. 9, it is understood that maximum oscillation frequency (f_{max}) of the device increases with an increase in the percentage of In in the channel material.

3.3. Circuit performance: Circuit performance was estimated by using the device in a cascode amplifier. The cascode amplifier is a two-stage circuit constructed using two transistors. The schematic circuit diagram of a two-stage cascode amplifier is shown in Fig. 10, where MOSFET M2 is biased by the biasing voltage, and in the gate terminal of MOSFET M1 the input is applied. In the circuit, one transistor operates as a common source and the other as a common gate configuration. This combination has advantages in

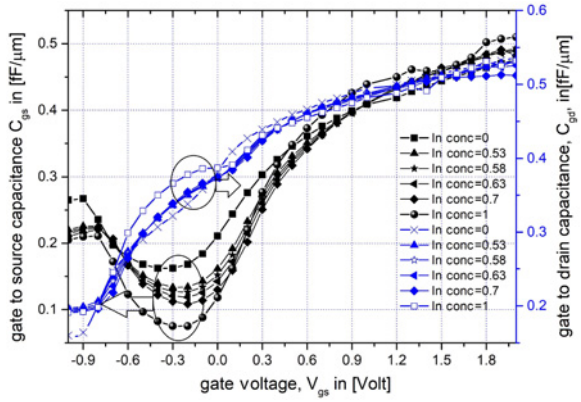

Fig. 7 *Variation of gate capacitances (C_{gs} and C_{gd}) as a function of V_{gs} for different In concentrations at $V_{ds} = 1$ V*

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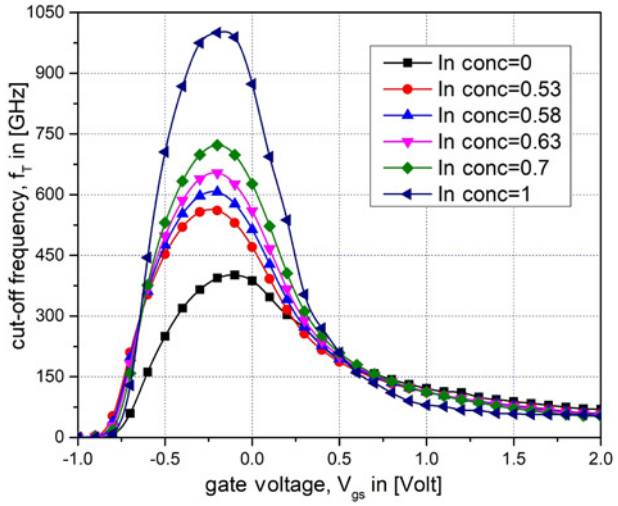

Fig. 8 *Variation of f_T as a function of (V_{gs}) for different In concentrations at $V_{ds} = 1$ V*

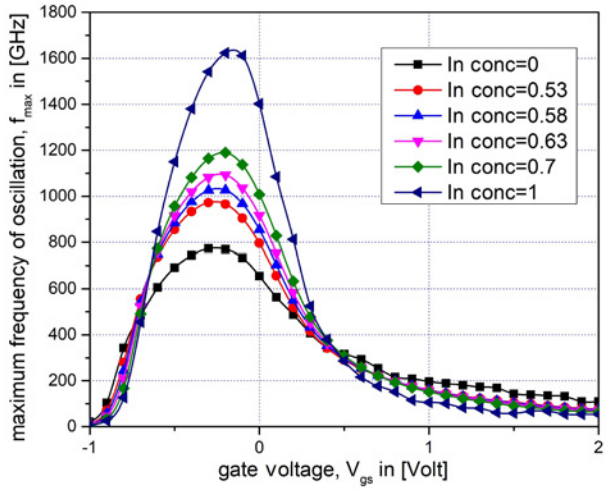

Fig. 9 *Variation of f_{max} as a function of (V_{gs}) for different In concentrations at $V_{ds} = 1$ V*

terms of higher input–output isolation, higher gain or higher bandwidth, better stability, higher slew rate etc.

The output characteristic of the simulated two MOSFET cascode amplifier constructed using the device under study is shown in Fig. 11. The variation of the characteristics with different In concentration is understood from this figure. The devices are specified by the width of 1 μm and the reference voltage of 0.6 V is used. Fig. 12 shows the variation of the differential gain as a function of input voltage for different In percentage. From this figure, it is clear that the maximum differential gain of the device with lower mole fraction is greater than the devices with higher In content.

4. Conclusion: Various device parameters related to analogue circuit performance for InGaAs/InP heterostructure MOSFETs have been studied in this work. The impact of In content of the channel on RF/analogue performance of the device is investigated. Higher ON current and g_m with increasing In percentage has been observed in this Letter. It is concluded that the analogue performance parameters such as transconductance (g_m), transconductance–-generation factor (g_m/I_d), cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) increase with increase in mole fraction of In in the channel. The device with

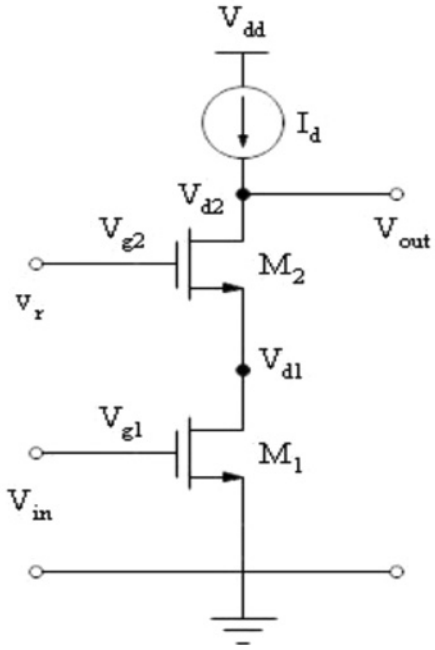

Fig. 10 *Schematic representation of a cascode amplifier*

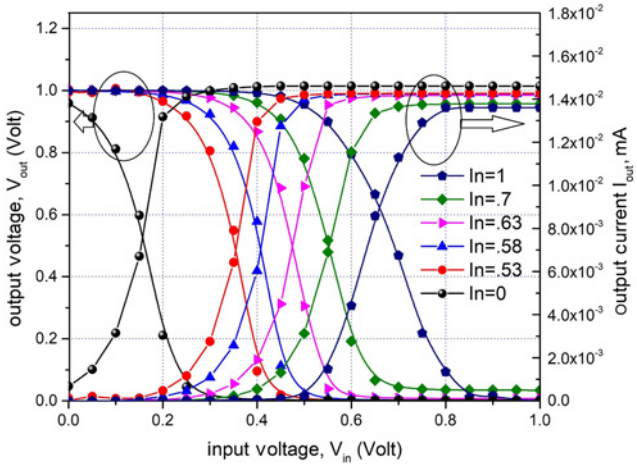

Fig. 11 *Output characteristics of the cascode amplifier for different In concentrations*

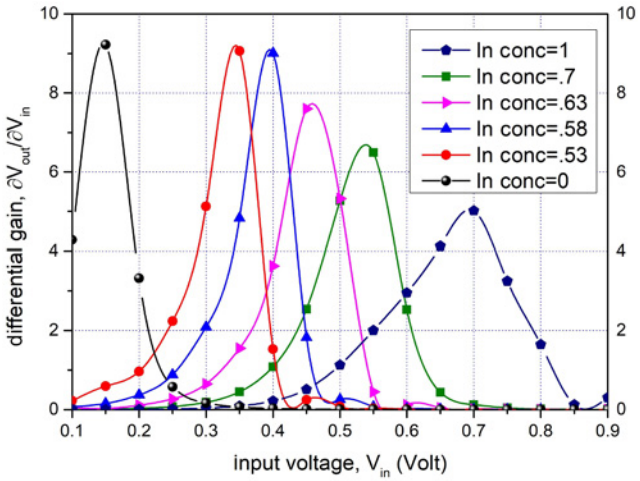

Fig. 12 *Variation of the differential gain as a function of input voltage*

higher In content shows improved f_T and f_{max}. However, if we use a single stage to multiple stage circuit design such as a cascode amplifier, the differential gain decreases with increase in In content. The increase of the In concentration in $In_xGa_{1-x}As$ also increases the lattice constant which in turn increases the lattice mismatch with InP layer. Thus, a trade-off in channel composition must be made to optimise the device performance and device reliability. These findings form the design guidelines to optimise the performance of the device with InGaAs channel.

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