Effect of gate dielectric on electrical parameters due to metal gate WFV in n-channel Si step FinFET

Rajesh Saha ✉, *Brinda Bhowmick, Srimanta Baishya*

Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Silchar 788010, India
✉ *E-mail: rajeshsaha93@gmail.com*

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This work reports the statistical impact of dielectric constant (k) of gate dielectric materials on various electrical parameters in step-FinFET (fin field-effect transistor) and conventional FinFET (C-FinFET) due to the gate metal work function variability (WFV). 3D technology computer-aided design simulations showed that several performance parameters are more affected by the WFV in C-FinFET than in step-FinFET. It was observed that the fluctuation of parameters like subthreshold swing (σSS), on current (σI_{on}), and off current (σI_{off}) are noticeably affected by dielectric materials. However, for both the structures, there is no significant variation in the threshold voltage (σV_T) with variation in k values for varying grain size.

1. Introduction: Aggressive downscaling of the device dimensions puts severe limitations on a metal oxide semiconductor transistor due to unbearable short channel effects [1]. However, the fin field-effect transistors (FinFETs), which can control the channel from all the three sides of the channel, have been perceived as a suitable alternative [2]. The scaling of device dimensions demands a proportionate scaling down of the oxide thickness which, in turn, results in an increased gate leakage. To overcome this problem, high-k gate dielectrics such as crystallised HfO_2 [3], ZrO_2 [4], and doped dielectric [5] have been found to be more suitable. However, the high-k gate oxides are not compatible with a polysilicon gate due to the two key technical difficulties: Fermi-level pinning [6] and phonon scattering [7]. It has been shown that these problems can be resolved by replacing a polysilicon gate by a metal gate. On the other hand, the work function (WF) value of the metal gate depends upon the crystal orientation of the metal, which leads to the undesirable variation in threshold voltage [8]. The shape of the distribution due to WF variability (WFV) is close to normal if the number of grains covering the gate area is large [8]. The impact of the WFV of the metal gate on threshold voltage reduces with increase in the aspect ratio and/or decrease in grain size [9]. In this regard, the Ti metal gate is less prone to threshold voltage variation than other metal gates like Ta, W, and Mo [10]. The statistical variation in threshold voltage due to the WFV of the metal gate also decreases with the increase in device dimensions of metal oxide semiconductor field effect transistors and the shape of the distribution of the threshold voltage is normal for small grain size [11, 12]. It has been reported that the conventional FinFET (C-FinFET) shows lesser variation in threshold voltage than junctionless FinFET in the presence of the WFV of the metal gate [13]. The influences of the WFV on threshold voltage and subthreshold swing are lower and higher, respectively, in Ge p-channel FinFET than in Si p-channel FinFET [14]. In [15], we have reported the variation in various electrical parameters of Si step-FinFET is less affected by the WFV of the metal gate at different channel length, fin width, and grain sizes. Likewise, Gate All Around Nanowire Field Effect Transistor (GAA NW FET) is also less prone to threshold voltage variation due to WFV than C-FinFET [16]. However, the influence of the WFV for different dielectric materials on other electrical parameters like threshold voltage, drain current, and subthreshold swing (SS) in the non-C-FinFET structure should be an interesting one.

In this Letter, we studied the effect of the WFV of the Ti metal gate on threshold voltage (σV_T), on current (σI_{on}), subthreshold swing (σSS), and off current (σI_{off}) for different dielectric constants in Si step-FinFET. Our study is a simulation using a 3D technology computer-aided design (TCAD) simulator. A comparative investigation of the WFV induced on electrical parameters between the step-FinFET and C-FinFET with various gate dielectric constants is presented.

2. Device descriptions and TCAD calibration: The 3D and 2D views of the proposed Si step-FinFET are shown in Figs. 1*a* and *b*, respectively. Fig. 1*c* shows the 2D view of C-FinFET. We have designed the step-FinFET from C-FinFET by reducing a fraction of the fin width in the upper section as shown. As a result, the step-FinFET has two different fin widths, and consequently, two different gate oxide thicknesses. However, the total fin height for both the devices is the same.

All simulations were carried out using a 3D TCAD device simulator [17]. The calibration of the TCAD model was done by matching the direct current characteristic of the simulated results with the fabricated results reported in [18]. Due to the presence of high doping sources and drain regions, the Fermi Dirac statistics, the bandgap narrowing, the Shockley Read Hall for recombination and generation, and doping dependent Masetti models were activated in simulation [17]. Furthermore, some of the mobility parameters were tuned to the experimental results. The adjusted values of mobility parameters were: $\text{mumin1} = 180\ \text{cm}^2/\text{Vs}$, $\text{mumin}^2 = 29\ \text{cm}^2/\text{Vs}$, $\text{mu1} = 39\ \text{cm}^2/\text{Vs}$, $C_r = 25.7 \times 10^8$, and $\beta = 3$ [17], where mumin1, mumin2, mu1 are the reference mobility parameters, C_r is the reference concentration parameter, and β is a fitting parameter. To take care of the high-field effect, the corresponding high field saturation model was activated. With a very small gate length and fin width, a significant amount of the quantum confinement effect is expected to be present. As the device has very small device dimensions, the quantum confinement effect cannot be ignored, and to account for the same, the TCAD has the necessary quantum density gradient model which was also activated. Parameters and their default values for the same are $\gamma = 3.6$ is the weighting factor quantum potential, $\theta = 0.5$ is the weight for the quadratic term, $\xi = 1$ is the weight for quasi-Fermi potential, and $\eta = 1$ is the weight for electrostatic potential. The good agreement of the simulated and experimental results [18] for both the transfer and output characteristics as shown in Figs. 2*a* and *b*, respectively, indicates that the simulator is accurately calibrated. In this Letter, the calibrated TCAD model parameters are used for all simulations.

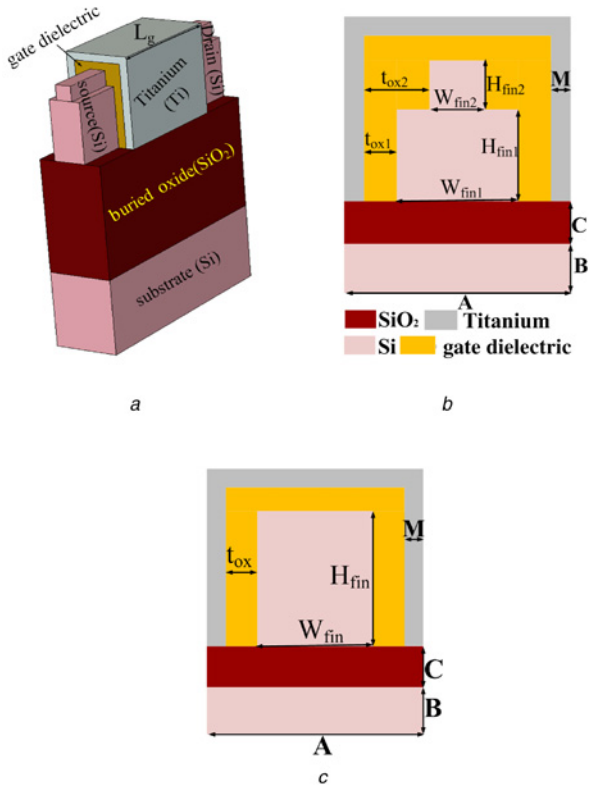

Fig. 1 *Schematic of the structures*
a 3D view of the proposed Si-step–FinFET
b 2D view of the Si-step–FinFET
c 2D view of C-FinFET

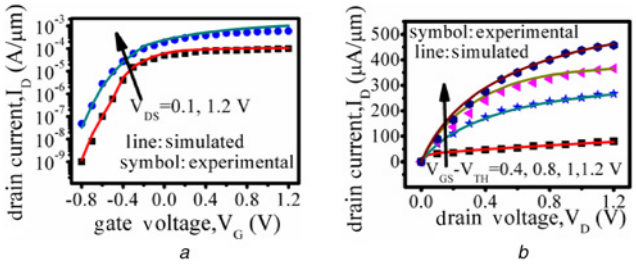

Fig. 2 *Calibration TCAD model with experimental results [18] for*
a Transfer characteristics
b Output characteristics

A comparison between the conventional and step-FinFET shows that in a 10 nm technology node the Step-FinFET is capable of meeting the targeted ITRS requirements of on and off currents [15]. The major advantage of such a device is that a very low value of off current can be achieved without any significant degradation of the on current. Due to the lesser fin width, the source/drain resistances are increased, leading to a decrease in the drain current [19]. However, increase in the on state saturation resistance is less affected by the decreased fin width and the on current is not affected significantly. Furthermore, the step device has lower horizontal electric field and gate capacitance [15].

If we reduce the entire fin width of a C-FinFET to get the benefits of reduced fin width, a uniform larger oxide thickness will be formed over the whole fin. On the other hand, only a part of the cross-section of the step device has a larger oxide thickness, which helps in reducing the gate leakage current. The reduction of the entire fin width results in decrease of both the on and off currents by almost equal order [19]. As such, in the step structure, the off current is reduced considerably, with negligible degradation in the on current.

The different gate dielectric materials with their dielectric constants (k) used in this work are SiO_2 ($k=3.9$), Al_2O_3 ($k=10$), HfO_2 ($k=22$), and La_2O_3 ($k=27$). The device parameters used for C-FinFET and step-FinFET are gate length ($L_g=12$ nm), fin height at lower section ($H_{fin1}=8$ nm), fin height at upper section ($H_{fin2}=2$ nm), fin width at lower section ($W_{fin1}=4$ nm), fin width at upper section ($W_{fin2}=2$ nm), oxide thickness at lower section ($t_{ox1}=1$ nm), oxide thickness at upper section ($t_{ox2}=2$ nm), fin height of C-FinFET ($H_{fin}=8$ nm), fin width of C-FinFET ($W_{fin}=4$ nm), oxide thickness of C-FinFET ($t_{ox}=1$ nm), height of buried oxide (C = 15 nm), source/drain doping ($N_S/N_D=10^{19}$ cm^{-3}), and channel doping ($N_A=10^{16}$ cm^{-3}).

To analyse the impact of WFV, Ti is used as the gate material as it exhibits lower deviation in WF [6]. It has WF values of 4.6 and 4.4 eV in orientations ⟨200⟩ and ⟨111⟩ with probabilities 60 and 40%, respectively [6]. A dedicated random algorithm is inbuilt in the TCAD simulator, which assumes non-uniform distribution with an average grain size ($\bar{\varphi}$) of 5 and 7 nm, is used to study the distribution of WF within the gate area. The metal grains are randomly distributed with their WFs and probability of occurrence in the gate area having a unique grain pattern. Each of the structural combination is simulated 200 different times to find the variation in electrical parameters.

3. Results and discussion: To study the significance of WFV of the Ti metal gate, step-FinFET and C-FinFET are simulated 200 times each having a randomly different grain pattern. The numerical values of σV_T, σSS, σI_{on}, and σI_{off} are extracted at drain to source voltage (V_{DS}) of 0.5 V. The threshold voltage is extracted by using a constant current (10^{-7} A) method.

With two different values of grain size, σV_T of both step-FinFET and C-FinFET is portrayed in Fig. 3*a* for various values of k. It is observed that σV_T in the proposed device is less than the same in C-FinFET due to more controllability over the channel in the proposed FinFET. Due to the lower fin width in the upper part of the fin, V_t roll off is less [20], which makes it less sensitive to σV_T. Moreover, the value of σV_T does not change significantly with increase in k at various $\bar{\varphi}$ for both the structures at $V_{GS}=V_T$. This is due to the lower sensitivity to potential variation at larger k values (Fig. 3*b*) [16].

The variation of surface potential in the step-FinFET at off state ($V_G=0$ V) and on state ($V_G=1.5$ V) is shown in Figs. 4*a* and *b*, respectively. It is seen that the surface potential decreases with increase in k value at the off condition (Fig. 4*a*), while the opposite behaviour is observed at the on state (Fig. 4*b*). This behaviour leads to decrease and increase of the drain current at linear and saturation regions, respectively, with increasing k value as shown in Fig. 4*c*. This trend of drain current is due to increase in gate control over the channel with an increase in k value. For better visualisation of drain current at lower gate voltage, an inset is added in Fig. 4*c*.

A better gate control enables our device to have a lesser subthreshold swing (σSS) than C-FinFET for both values of $\bar{\varphi}$ as shown in

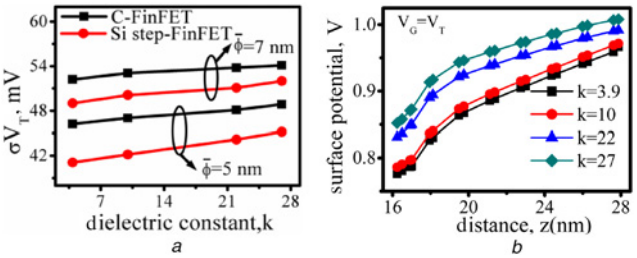

Fig. 3 *Variation in threshold voltage and its physics*
a σV_T for both Si-step–FinFET and C-FinFET
b Surface potential of Si-step–FinFET for various values of k at $V_{GS}=V_T$ and $V_{DS}=0.5$ V

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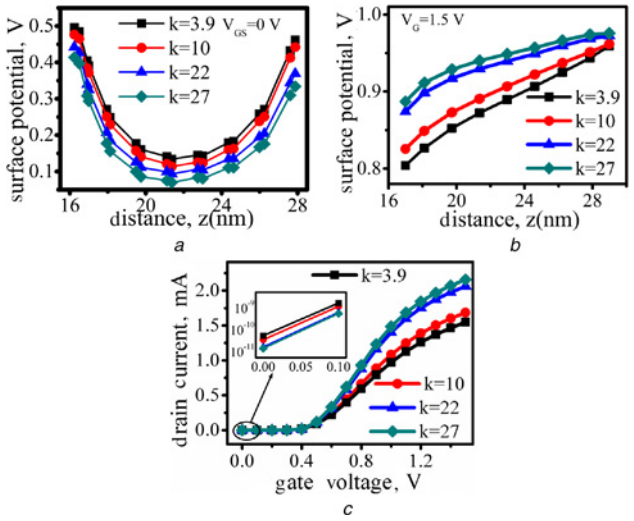

Fig. 4 *Surface potentials and drain current for various k*
a Surface potential of Si-step–FinFET at $V_{GS} = 0$ V and $V_{DS} = 0.5$ V
b Surface potential of Si-step–FinFET at $V_{GS} = 1.5$ V and $V_{DS} = 0.5$ V
c I_D–V_G plot of Si-step–FinFET for various values of *k*

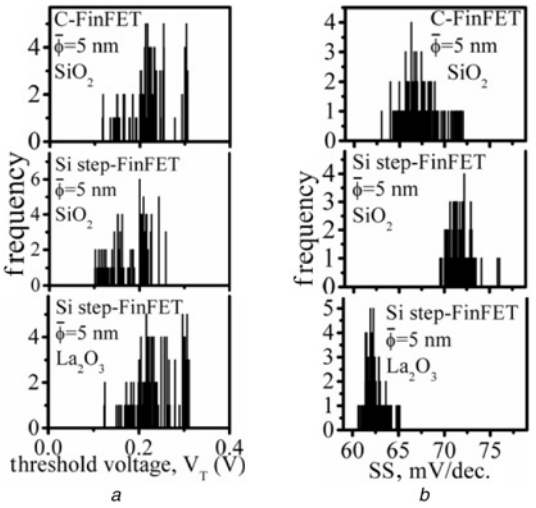

Fig. 6 *Histogram of a comparative study between S-step–FinFET and C-FinFET, and to analyse the effect of k in Si step-FinFET for*
a V_T variation
b SS variation

Fig. 5*a*. The SS value is inversely proportional to *k* [21] and, therefore, σSS decreases with increase in *k* for both the devices. Values of σI_{on} and σI_{off} are found to be higher in C-FinFET than in step-FinFET. A lower fin width gives rise to a higher source/drain resistance [19], which is responsible for a reduction of the drain current in both the linear and saturation regions. This leads to a reduced value of σI_{on} and σI_{off} as plotted in Figs. 5*b* and *c*, respectively. A larger *k* improves the drain current in the saturation and linear regions as shown in Fig. 4*c*. As expected, σI_{on} increases and σI_{off} decreases with increase in *k* values. For better visualisation of σI_{off} at $\bar{\varphi} = 5$ and 7 nm in the step-FinFET, an inset is added in Fig. 5*c*. The variation of σI_{off} with a large scale is not apparent. To show that in the expanded scale, the vertical axis is expanded, while the horizontal axis is compressed to accommodate as an inset.

As is observed from the histogram for V_T variation (Fig. 6*a*), we found the spreading in V_T is more in C-FinFET than in step-FinFET. Furthermore, the said spreading is not very significant for higher values of dielectric constant (Fig. 6*a*). As already established [8], the distribution of V_T is neither Gaussian nor symmetric.

Histograms for SS variation are shown in Fig. 6*b* and it was observed that spreading in SS is more in C-FinFET due to stronger gate control as already pointed out, which leads to more variation in SS. The inverse relationship between SS and *k* is established from the plots in Fig. 6*b*. It also demonstrates a reduction in the impact of WFV of the metal gate on SS with increased *k* values.

The histograms for I_{on} and I_{off} variations are shown in Figs. 7*a* and *b*, respectively. Likewise, we observed a lesser spread in I_{on} (Fig. 7*a*) and I_{off} (Fig. 7*b*) in our device. Thus, the proposed device is more immune to WFV. We also found that with an increase in *k*, the spreading of I_{on} increases and I_{off} decreases as portrayed in Figs. 7*a* and *b*, respectively. From this observation, we can conclude that with increasing *k*, σI_{on} is increased while σI_{off} is decreased.

In [13, 14], the impact of WFV on the threshold voltage for 5 nm grain size using Ti/high-*k* interface is reported in C-FinFET

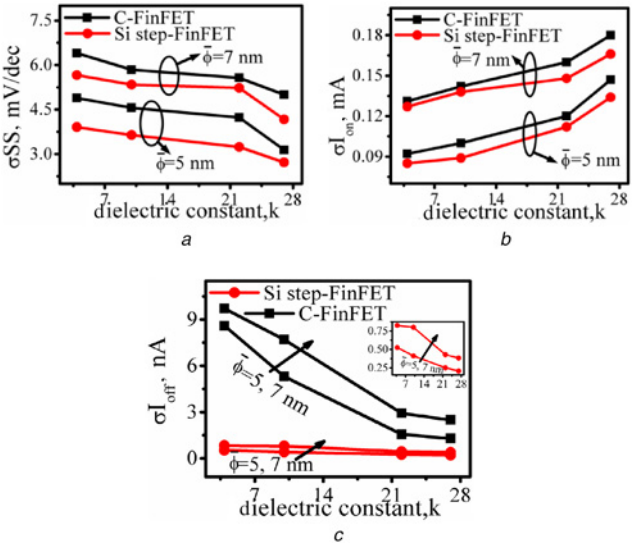

Fig. 5 *Variation in SS, I_{on}, and I_{off}*
a σSS for both Si-step–FinFET and C-FinFET
b σI_{on} for both Si-step–FinFET and C-FinFET
c σI_{off} for both Si-step–FinFET and C-FinFET

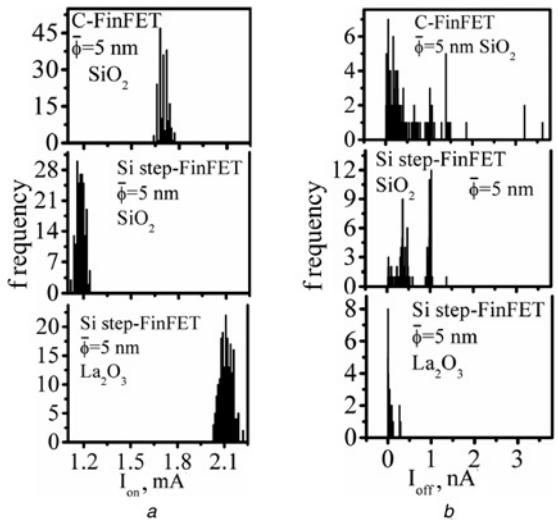

Fig. 7 *Histogram of a comparative study between S-step–FinFET and C-FinFET, and to analyse the effect of k in Si step-FinFET for*
a I_{on} variation
b I_{off} variation

structures and such devices have more fluctuation in electrical parameters than the proposed step-FinFET.

4. Conclusion: We have reported the impact of gate dielectric constant on electrical parameters in the presence of WFV of a metal gate. It has been observed that the increase in σV_T is insignificant with increase in k for both the step-FinFET and C-FinFET. However, the value of σSS decreases, σI_{on} increases, and σI_{off} decreases with increase in k for both the devices. We have demonstrated a comparative study on variability issues showed that the step-FinFET is more immune to WFV induced on σV_T, σSS, σI_{on}, and σI_{off}. As such, the proposed device can be used in low-power applications.

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