Examination of the impingement of interface trap charges on heterogeneous gate dielectric dual material control gate tunnel field effect transistor for the refinement of device reliability

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In this work, the authors have reported the reliability issues of dual material control gate tunnel field effect transistor (DMCG-TFET) and proposed heterogeneous gate dielectric dual metal control gate tunnel field effect transistors (HD DMCG-TFETs) in terms of interface trap charges (ITCs). The positive and negative types of localised charges at the semiconductor/insulator interface cause degradation in the device performance (DC/RF). In this regard, the proposed structure which includes combination of low-K and high-K dielectric improves the immunity towards the ITCs at the interface of semiconductor/insulator with better performance. In this concern, the study has analysed the impact of ITCs on DC and analogue/RF performances of the DMCG-TFET and HD DMCG-TFET in terms of various parameters like electric field, energy band diagram, carrier concentration, transfer characteristics, transconductance (g_m), cutoff frequency (f_T) and gain bandwidth product. Further to this, impact on device linearity parameters is also analysed through higher order of transconductance coefficients (g_{m3}), VIP2, VIP3 and IIP3.

1. Introduction: With the downsizing of device dimensions, metal–oxide–semiconductor field-effect transistor (MOSFET) manifests compactness, cost effectiveness and improved high-frequency performance [1, 2]. However, MOSFET faces some fundamental problems associated to device performance with downscaling like high leakage current, short-channel effects, drain induced barrier lowering and sub-threshold slope limited to 60 mV/decade, which severely degrades the performance of the device [2–4]. Tunnel field effect transistor (TFET) has a potential to overcome the above-mentioned problems due to its different working principle (band-to-band tunnelling mechanism) unlike MOSFET [4–6]. Regardless of these advantages, TFET suffers from various problems related to low drain current, conduction in ambipolar state and poor high-frequency performance [7–11].

For this, various structural modifications like bandgap variation by using different doping profile in source/drain region, hetero-material at drain/source region and pocket doping had been considered earlier for the improvement of DC/RF performance with suppressed ambipolar behaviour [12–18]. Although, the above-mentioned techniques improve DC/RF performance with suppressed ambipolar current, they create lattice mismatch, higher cost as well as fabrication complexity [19–22]. Hence, the improvement in drain current and suppression in ambipolar behaviour of the device are major concern of investigation. Therefore, to overcome these difficulties, the dual material control gate TFET (DMCG-TFET) with asymmetric doping in source and drain regions is presented [23]. In this, the different values of workfunction for tri-segmented DMCG-TFET are considered to maintain dual work functionality of the device for suppression of ambipolar behaviour, and to enhance the ON-state current. The presence of lower workfunction at auxiliary gate relative to control gate reduces the band bending and lateral electric field at the drain/channel junction which suppresses the ambipolar behaviour. However, the presence of lower workfunction at the tunnel gate relative to control gate increases the band bending and tunnelling probability at the source/channel junction in the ON-state, which results in an enhanced value of ON current (I_{ON}).

The tunnelling rate at the junctions (source/channel) is very sensitive towards electric field. However, the manifestation of interface trap charges (ITCs, positive/negative) at the silicon/insulator interface reduces the electric field at the tunnelling junction. Therefore, it shows the lower tunnelling probability and poor analogue/RF performance of the device. In this concern, we have proposed a hetero-gate-dielectric DMCG-TFET which is named as HD DMCG-TFET. HD DMCG-TFET improves the DC/RF performance as well as device reliability by reducing the effect of ITCs.

The remaining part of the Letter is organised as follows. Section 2 explains the architecture of device and simulation setup. Section 3 describes the results and discussion. Sections 4 finally summarises the conclusion.

2. Device structure and simulation setup: Fig. 1 shows the cross-sectional view of conventional DMCG-TFET (Fig. 1*a*) and HD DMCG-TFET (Fig. 1*b*). For both the devices, the design parameters considered are shown in Table 1. Simulation has been performed using Silvaco Atlas simulator in which a non-local band-to-band tunnelling model is used to compute the tunnelling

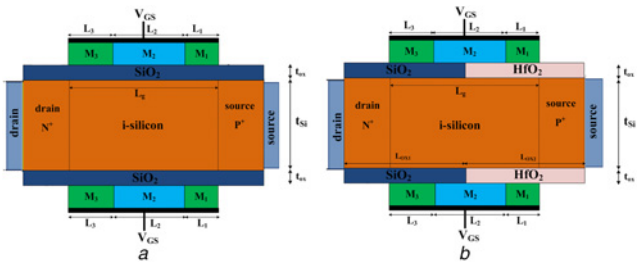

Fig. 1 *Cross-sectional view of*
a Conventional DMCG-TFET [4]
b Proposed HD DMCG-TFET

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Table 1 Device structure and simulation setup

Parameters	Conventional DMCG-TFET [5]	HD DMCG-TFET
drain length (L_D)	25 nm	25 nm
source length (L_S)	25 nm	25 nm
channel length (L_C)	50 nm	50 nm
source doping (*p-type*) (N_s)	1.0×10^{20} cm^{-3}	1.0×10^{20} cm^{-3}
channel doping (N_{ch})	1.0×10^{17} cm^{-3}	1.0×10^{17} cm^{-3}
drain doping (*n-type*) (N_d)	5.0×10^{18} cm^{-3}	5.0×10^{18} cm^{-3}
oxide thickness (t_{ox})	0.8 nm	0.8 nm
oxide length (L_{OX1}/L_{OX2})	100 nm (SiO_2)	50 nm(SiO_2)/ 50 nm (HfO_2)
silicon thickness (t_{si})	10 nm	10 nm
source voltage (V_S)	0 V	0 V
tunnelling gate length (L_1)	10 nm	10 nm
control gate length (L_2)	25 nm	25 nm
auxiliary gate length (L_3)	15 nm	15 nm
tunnel gate workfunction (ϕ_1)	4.0 eV	4.0 eV
control gate workfunction (ϕ_2)	4.6 eV	4.6 eV
auxiliary gate workfunction (ϕ_3)	4.0 eV	4.0 eV
interfacial charge density (q_f)	1.0×10^{12} cm^{-2}	1.0×10^{12} cm^{-2}

probability [24]. Shockley–Read–Hall recombination, bandgap narrowing model, trap-assisted tunnelling model and Auger recombination models are employed. Along with this, the Wentzel–Kramer–Brillouin approximation is used to calculate the tunnelling probability.

3. Results and discussion: In this section, DC characteristics of both the devices are compared in terms of ITCs. The use of hetero-dielectric (HD) increases the electric field at source/channel junction as shown in Fig. 2*b*. Fig. 2*b* shows almost overlapped lines to each other in comparison to Fig. 2*a*; it represents more immunity of the proposed structure towards ITCs. Figs. 3*a* and *b* describe the surface potential of both the devices at different (positive, neutral and negative) ITCs. HD does not cause significant improvement in surface potential for the proposed structure, but in the channel region, we can see less variation of surface potential due to the use of HD from the same figure. Similarly, Figs. 3*c*–*e* depict the energy band distribution along the length of devices for negative, neutral and positive ITCs, respectively. The use of HD reduces the tunnelling width at source/channel junction in case of the proposed device as shown in Fig. 3*d*.

3.1. Effect of ITC over the DC performance: In addition, Figs. 3*c* and *e* indicate less variation in energy band diagram (EBD) for negative and positive ITCs as compared to conventional device. Thin tunnelling width provides higher carrier transportation from the valence band of source to the conduction band of channel. It results in higher ON-state current for the proposed HD

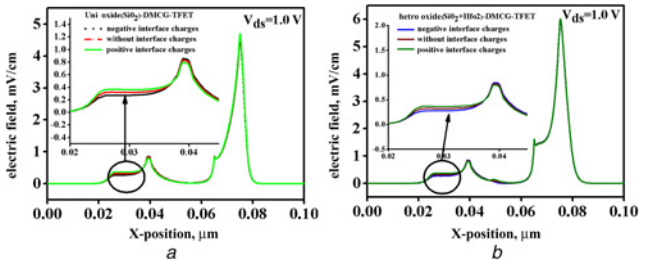

Fig. 2 *Effect of ITCs on the conventional DMCG-TFET and the proposed HD DMCG-TFET in terms of electric field*

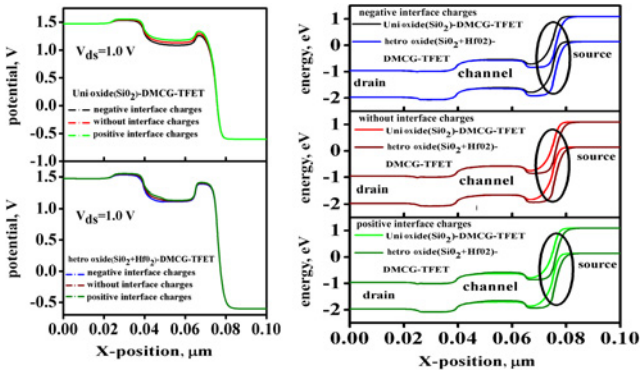

Fig. 3 *Effect of ITCs on*
a Surface potential for DMCG-TFET
b Surface potential for HD DMCG-TFET
c Variation in EBD for negative ITCs on both structures
d Variation in EBD without ITCs on both structures
e Variation in EBD for positive ITCs on both structures

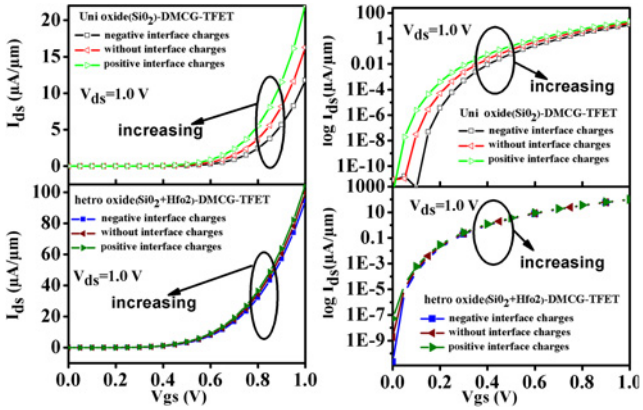

Fig. 4 *Input characteristics in linear scale and logarithmic scale*
a Input characteristics in linear scale for DMCG-TFET
b Input characteristics in linear scale for HD DMCG-TFET
c Input characteristics in logarithmic scale for DMCG-TFET
d Input characteristics in logarithmic scale for HD DMCG-TFET

DMCG-TFET as compared to conventional structure, which can be compared from Figs. 4*a* and *b*. Both the figures illustrate the comparison in terms of ITCs; HD DMCG-TFET has higher drain current due to the use of HD [25]. Simultaneously, Figs. 4*c* and *d* show drain current in log scale with V_{gs}. So, overall from Fig. 4, we can estimate that proposed device shows higher immunity for ITCs, and can be seen its effect on drain current and other sub-threshold characteristics [26]. Further Figs. 5*a* and *b* indicate variation in drain current with V_{ds}, where the effect of ITCs is higher on conventional device as compared to HD DMCG-TFET.

3.2. Effect of ITC over the analogue/RF performance: Further, we have analysed the impact of ITCs for RF figures of merit (FOMs). In this concern, transconductance (g_m) is defined as the efficiency of the device to convert gate supply voltage (V_{gs}) into the drain current. Fig. 6*b* indicates that the proposed device has higher g_m and better ITCs performance as compared to conventional DMCG-TFET (Fig. 6*a*). Transconductance generation factor is the device efficiency which converts the DC parameters (I_{ds}) into AC parameters (g_m). HD increases the g_m, which makes it more robust against ITCs as shown in Figs. 6*c* and *d*. In case of output conductance (g_{ds}), drain current starts dominating beyond sub-threshold region in case of the proposed device compared to DMCG-TFET, which is reflected

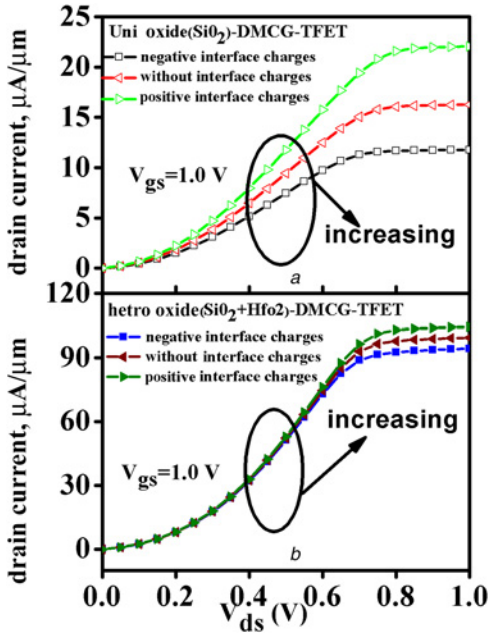

Fig. 5 *Variation in drain current with V_{ds} as function of ITCs*
a DMCG-TFET
b HM-DMCG-TFET

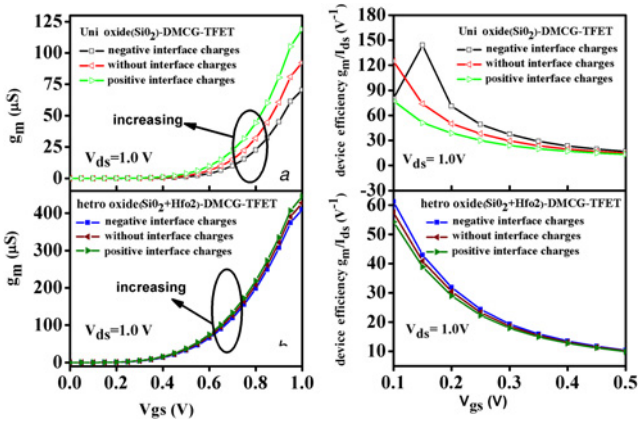

Fig. 6 *Variation in g_m and device efficiency as a function of ITCs*
a Variation in g_m as a function of ITCs for DMCG-TFET
b Variation in g_m as a function of ITCs for HD DMCG-TFET
c Variation in device efficiency as a function of ITCs for DMCG-TFET
d Variation in device efficiency as a function of ITCs for HD DMCG-TFET

in Fig. 7*a*. Moreover, from the same figure, we can see that HD DMCG-TFET is unaffected from ITCs. Similarly, output resistance also shows robust behaviour towards ITCs as shown in Fig. 7*b*. Fig. 8 shows variation in C_{gs} and C_{gd} with V_{gs} for both the devices. C_{gs} decreases with V_{gs} due to the increase in potential difference between gate and source terminals (Figs. 8*a* and *b*) and ITCs causes no effect on C_{gs}. Further, Figs. 8*c* and *d* present almost same magnitude of gate to drain capacitances for both the devices. In TFET, the total capacitance is combination of parasitic as well as inversion capacitances [27]. The ITCs have almost same consequences for DMCG-TFET and HD DMCG-TFET as shown in the same figure. Another significant high-frequency FOM is cut-off frequency (f_t), and can be defined as the operating frequency of device for which short-circuit current gain decreases up to unit value and can be formulated as: $f_t = g_m/2\pi(C_{GS} + C_{GD})$. Higher g_m with moderate C_{gd} are the reason for improved f_t of the proposed device as illustrated in Figs. 9*a* and *b*. Same figure shows the immune behaviour of HD

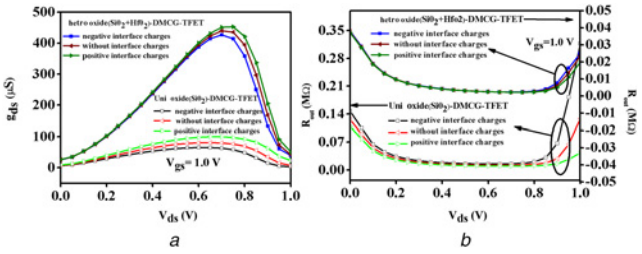

Fig. 7 *Variation in g_{ds} and output resistance as a function of ITCs*
a Variation in g_{ds} and output resistance as a function of ITCs, variation in g_{ds} as a function of ITCs for DMCG-TFET and variation in g_{ds} as a function of ITCs for HD DMCG-TFET
b Variation in output resistance as a function of ITCs for DMCG-TFET and HD DMCG-TFET

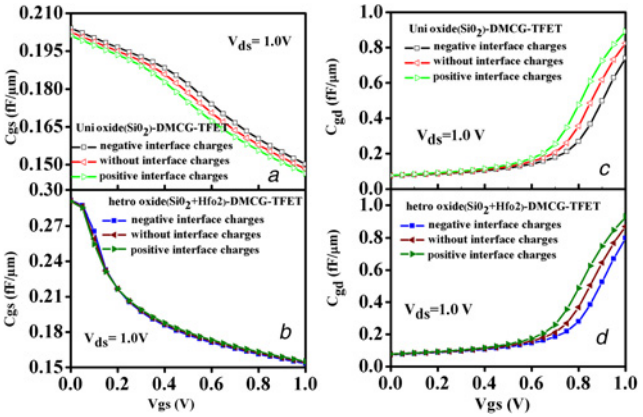

Fig. 8 *Variation in C_{gs} and C_{gd} as a function of ITCs*
a Variation in C_{gs} as a function of ITCs for DMCG-TFET
b Variation in C_{gs} as a function of ITCs for HD DMCG-TFET
c Variation in C_{gd} as a function of ITCs for DMCG-TFET
d Variation in C_{gd} as a function of ITCs for HD DMCG-TFET

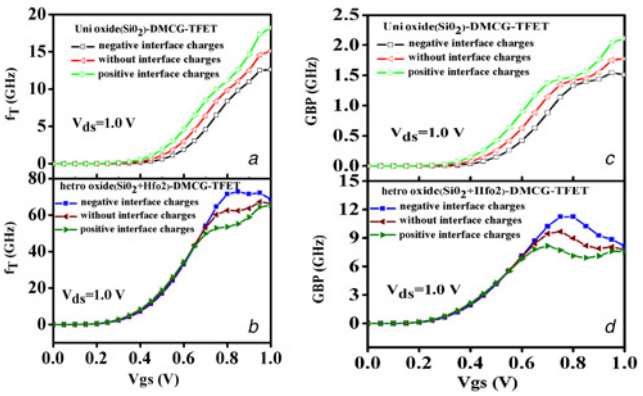

Fig. 9 *Variation in f_t and GBP as a function of ITCs*
a Variation in f_t as a function of ITCs for DMCG-TFET
b Variation in f_t as a function of ITCs for HD DMCG-TFET
c Variation in GBP as a function of ITCs for DMCG-TFET
d Variation in GBP as a function of ITCs for HD DMCG-TFET

DMCG-TFET towards ITCs as compared to conventional structure. Another high-frequency parameter is gain bandwidth product (GBP), which defines the operating bandwidth of an amplifier. Mathematical expression of GBP is approximately same as f_t. Consequently, it follows similar behaviour as f_t, which is shown in Figs. 9*c* and *d*.

3.3. Impact of ITCs on linearity and distortion performance: Advanced communication high-frequency devices need less

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distortion in their operating regions. Drain current saturation, and other sub-threshold parameters are not sufficient to analyse the device linearity. Since g_m is variable with V_{gs} so, third-order derivatives are used to examine the linearity of devices. The linearity can be analysed in terms of third-order harmonic distortion (gm3), second-order voltage intercept point (VIP2), third-order voltage intercept point (VIP3) and third-order intercept point (IIP3). We have considered $R_s = 50\,\Omega$ due to its practical demand in RF systems. In this section, we have given a detailed review of ITCs over linearity parameters. Here, Figs. 10*a* and *b* present variation in g_{m3} in the influence of ITCs for DMCG-TFET and HD DMCG-TFET, respectively. The peak of g_{m3} indicates lower limit of nonlinearity. The use of HD does not cause significant improvement in linearity but it reduces the effect of ITCs as we can see from the same figure. VIP2 is extrapolated input voltage at which first- and second-order harmonics are equal and it should be high enough. Figs. 10*c* and *d* give idea about the ITC resistant behaviour of the proposed device in comparison to conventional structure. In addition to these, the peak of VIP3 indicates the cancellation of third-order nonlinearity; HD DMCG-TFET having higher peak and little variation for positive and negative ITCs in comparison to DMCG-TFET as presented in Figs. 11*a* and *b*. Similarly, the

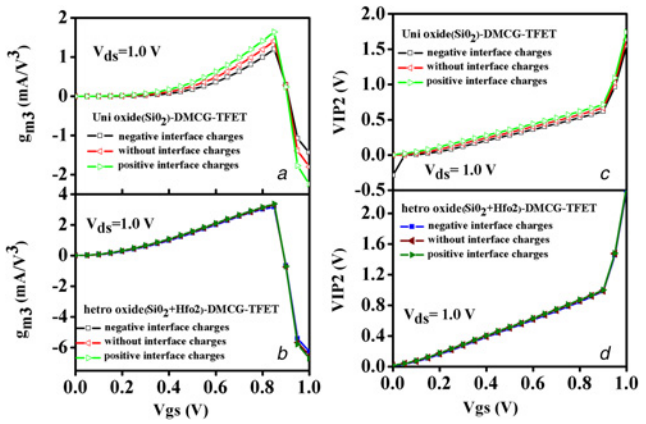

Fig. 10 *Variation in g_{m3} and VIP2 as a function of ITCs*
a Variation in g_{m3} as a function of ITCs for DMCG-TFET
b Variation in g_{m3} as a function of ITCs for HD DMCG-TFET
c Variation in VIP2 as a function of ITCs for DMCG-TFET
d Variation in VIP2 as a function of ITCs for HD DMCG-TFET

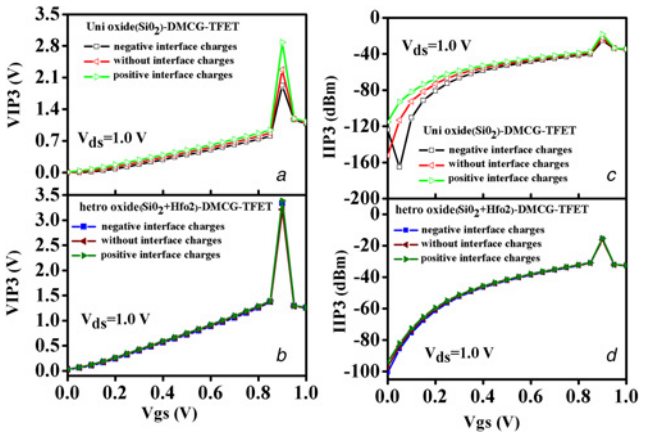

Fig. 11 *Variation in VIP3 and IIP3 as a function of ITCs*
a Variation in VIP3 as a function of ITCs for DMCG-TFET
b Variation in VIP3 as a function of ITCs for HD DMCG-TFET
c Variation in IIP3 as a function of ITCs for DMCG-TFET
d Variation in IIP3 as a function of ITCs for HD DMCG-TFET

Table 2 Impact of ITCs on DC/RF performance

Parameters at $V_{gs} = 0.5$ V	Conventional DMCG-TFET	HD DMCG-TFET
ITCs	positive (negative)	positive (negative)
input characteristics	1.96%↑(0.47%↓)	1.11%↑(0.896%↓)
output characteristics	1.24%↑(0.79%↓)	1.017%↑ (0.983%↓)
output conductance	1.196%↑(0.823%↓)	1.01%↑(0.986%↓)
gate to source capacitance	0.98%↑(0.95%↓)	1.01%↑(0.997%↓)
gate to drain capacitance	1.08%↑(0.935%↓)	1.07%↑(0.992%↓)
transconductance	1.74%↑(0.54%↓)	1.1%↑(0.93%↓)

HD in the proposed device improves the IIP3, which provides higher carrier transport and better controlling over the channel region as shown in Figs. 11*c* and *d*. Further, the same figure shows that HD DMCG-TFET has better performance than DMCG-TFET in terms of trap charge behaviour. Table 2 shows the impact of ITCs for device characteristics for conventional and proposed device.

4. Conclusion: In all the Nanoscale devices, generally the ITCs play an important role in deteriorating the performance of the device in terms of DC, analogue/RF, as well as linearity/distortion. In this manuscript, we have reported the effect of positive/negative ITCs for both the devices. For this, we have carried out and compared these effects in terms of DC/RF and linearity parameters through ATLAS simulator. From the outcome it is observed that HD DMCG-TFET shows less variation against the ITCs and shows better immunity towards ITCs. The HD engineering provides improved transconductance for HD DMCG-TFET which results in better DC/RF performance as compared to DMCG-TFET.

5 References

[1] Koswatta S.O., Lundstrom M.S., Nikonov D.E.: 'Performance comparison between p-i-n tunneling transistors and conventional MOSFETs', *IEEE Trans. Electron Devices*, 2007, **56**, (3), pp. 456–465
[2] Colinge J.-P.: 'FinFETs and other multi-gate transistors' (Springer, New York, NY, USA, 2008)
[3] Wang P.F., Hilsenbeck K., Nirschl T., *ET AL.*: 'Complementary tunneling transistor for low power application', *Sold-State Electron.*, 2004, **48**, (12), pp. 2281–2286
[4] Ionescu A.M., Riel H.: 'Tunnel field-effect transistors as energy efficient electronic switches', *Nature*, 2011, **479**, (7373), pp. 329–337
[5] Boucart K., Ionescu A.M.: 'Silicon nanowire tunnelling field-effect transistors', *IEEE Trans. Electron Devices*, 2007, **54**, (7), pp. 1725–1733
[6] Agarwal S., Klimeck G., Luisier M.: 'Leakage-reduction design concepts for low-power vertical tunneling field-effect transistors', *IEEE Electron Device Lett..*, 2010, **31**, (6), pp. 621–623
[7] Saurabh S., Kumar M.J.: 'Novel attributes of a dual material gate nanoscale tunnel field-effect transistor', *IEEE Trans. Electron Devices.*, 2010, **58**, (2), pp. 404–410
[8] Hraziia A., Andrei C., Vladimirescu A., *ET AL.*: 'An analysis on the ambipolar current in Si double-gate tunnel FETs', *SolidState Electron.*, 2012, **70**, pp. 67–72
[9] Abdi D.B., Kumar M.J.: 'Controlling ambipolar current in tunneling FETs using overlapping gate-on-drain', *IEEE J. Electron Devices Soc.*, 2014, **2**, (6), pp. 187–190
[10] Rawat B., Paily R.: 'Analysis of graphene tunnel field-effect transistors for analog/RF applications', *IEEE Trans. Electron Devices*, 2015, **62**, (8), pp. 2663–2669
[11] Ghosh S., Koley K., Sarkar C.K.: 'Impact of the lateral straggle on the analog and RF perforamcne of TFET', *Microelectron. Reliab..*, 2015, **55**, (2), pp. 326–331

[12] Banerjee S., Richardson W., Coleman J., *ET AL.*: 'A new threeterminal tunnel device', *IEEE Electron Devices Lett.*, 1987, **8**, (8), pp. 347–349
[13] Baba T.: 'Proposal for surface tunnel transistors', *Japanese Journal of Applied Physics*, 1992, **31**, (4B), pp. 455–457
[14] Vijayvargiya V., Vishvakarma S.K.: 'Effect of drain doping profile on double-gate tunnel field-effect transistor and its influence on device RF performance', *IEEE Trans. Nanotechnol.*, 2014, **13**, (5), pp. 974–981
[15] Lee M.J., Choi W.Y.: 'Effects of device geometry on hetero-gatedielectric tunneling field-effect transistors', *IEEE Electron Device Lett.*, 2012, **33**, (10), pp. 1459–1461
[16] Sahay S., Kumar M.J.: 'Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using heterodielectric BOX', *IEEE Trans. Electrons Devices*, 2015, **62**, (11), pp. 3882–3885
[17] Raad B., Nigam K., Sharma D., *ET AL.*: 'Dielectric and work function engineered TFET for ambipolar suppression and RF performance enhancement', *Electron. Lett.*, 2016, **52**, (9), pp. 770–772
[18] Soni D., Sharma D., Yadav S., *ET AL.*: 'Performance improvement of doped TFET by using plasma formation concept', *Superlattices and Microstructures*, 2018, **113**, (2018), pp. 97–109, doi: 10.1016/j.spmi.2017.10.012
[19] Ahish S., Sharma D., Nithin Kumar Y.B., *ET AL.*: 'Performance enhancement of novel InAs/Si hetero double-gate tunnel FET using Gaussian doping', *IEEE Trans. Electron Devices*, 2016, **63**, (1), pp. 288–295
[20] Hanna A.N., Hossain H.M., Hussain M.M.: 'Inas/Si heterojunction nanotube tunnel transistors', *Sci. Rep.*, 2015, **5**, pp. 1–7
[21] Kim S.H., Kam H., Hu C., *ET AL.*: 'Germanium-source tunnel field effect transistors with record high ION/IOFF'. 2009 Symp. on VLSI Technology, Honolulu, HI, 2009, pp. 178–179
[22] Raad B., Sharma D., Nigam K., *ET AL.*: 'Physics-based simulation study of high-performance gallium arsenide phosphide-indium gallium arsenide tunnel field-effect transistor', *Micro Nano Lett.*, 2016, **11**, (7), pp. 366–368
[23] Nigam K., Kondekar P., Sharma D.: 'Approach for ambipolar behaviour suppression in tunnel FET by workfunction engineering', *Micro Nano Lett.*, 2016, **11**, (8), pp. 460–464
[24] 'ATLAS device simulation soft' (Silvaco, Santa Clara, CA, USA, 2012)
[25] Gupta S., Nigam K., Pandey S., *ET AL.*: 'Effect of interface trap charges on performance variation of heterogeneous gate dielectric junctionless-TFET', *IEEE Electron Device Lett.*., 2012, **64**, (11), pp. 117–122
[26] Mishra A., Narang R., Saxena M., *ET AL.*: 'Impact of interfacial fixed charges on the electrical characteristics of pocket-doped double gate tunnel FET', *IEEE Trans. Device Mater. Reliab.*, 2016, **16**, (2), pp. 4731–4737
[27] Yang Y., Tong X., Yang L.-T., *ET AL.*: 'Tunneling field-effect transistor: capacitance components and modeling', *IEEE Electron Device Lett.*, 2010, **31**, (7), pp. 752–754

doi: 10.1049/mnl.2017.0869