Effective design technique for improvement of electrostatics behaviour of dopingless TFET: proposal, investigation and optimisation

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Rapid tunnelling junction formation is a much crucial issue with conventional sub-nanometre tunnel field-effect transistor (TFET) to obtain improved electrostatics characteristics. This task becomes more problematic and complicated for dopingless TFET as a result of wide tunnelling barrier at channel/source junction. In this regard, a new approach has been employed by implanting the metal angle (MA) inside the dielectric layer near channel/source joint to obtain enhanced electrical behaviour of the proposed structure. Employment of MA of small work-function increases electron density at channel/source interface to have improved electron tunnelling rate. Work-function optimisation of MA on RF/DC parameters is analysed in device optimisation part of this work. Simultaneously length optimisation of MA is also presented in the device optimisation section to ease the complex fabrication steps. In addition to these, circuit level performance of proposed and conventional structures is also analysed in this study.

1. Introduction: With several advancements in fabrication technology, CMOS industries are continuously following the Moore's prediction about the increment in transistor density per unit chip. However, for sustain and continuous increment in chip density, new emerging devices are needed to replace existing bulk metal–oxide–semiconductor field-effect transistor (MOSFET), which suffers from impermissible problems such as the restriction of sub-threshold swing (SS) of 60 mV/dec, short channel effects, random-dopant-fluctuations (RDFs) and complex fabrication steps for miniaturisation of the structure into the deep micron region [1–6]. In this concern, TFET is developed to minimise aforementioned drawbacks of MOSFET. TFET is having much reduced SS (<60 mV/dec) than the bulk MOSFET because of non-conventional carrier injection mechanism [7, 8]. TFET uses band-to-band tunnelling (BTBT) mechanism for electric conduction [9, 10]. However, RDFs is still a roadblock for attaining deep micron structure for TFET [11, 12]. Such hurdle exists with TFET because of much complex nano-fabrication steps.

Hence, charge plasma technique based dopingless TFET (DL-TFET) is introduced to minimise problems of doped TFET. In DL-TFET, an intrinsic film of silicon is used to induce different regions on it. Here, drain and source regions are developed on a intrinsic film by selecting proper work-functions of metal electrodes (source and drain) [2]. So fabrication complexity is remarkably reduced by this technique. However, small ON current is still a vital problem with dopingless devices because of wide tunnelling barrier at channel/source boundary and such problem become non-tolerable with miniaturisation of the device into the deep micron region [13]. Such problem also reduces fan-out capability of DL-TFET. Therefore, in proposed structure metal angle DL-TFET (MA-DL-TFET), the horizontal metal layer (HML) (3.9 eV work-function) is deposited into dielectric layer at channel/source junction for enhancing electrical parameters of dopingless devices. However, placement of a vertical metal layer (VML) of same work-function in the proposed structure gives electrical contact between HML and gate electrode [14]. Consequently, positive gate to source voltage ($+V_{gs}$) can be applied throughout the spacer region (L_{GS}) to reduce tunnelling barrier at channel/source junction. Such placement of metallic layers provides double impact of $+V_{gs}$ and metal angle (MA) work-function engineering on development of strong electron plasma layer at source/channel interface for having much improved electrical characteristics of the device. The combination of metallic layers (VML and HML) is called as MA. Simultaneously, HfO_2 has been used as oxide layer material for entire width of the structures for improved DC characteristics. For non-difficult deposition of metallic layers inside the dielectric region, thickness of dielectric is considered 3 nm. Position as well as work-function of MA induce high-density layer of electrons at channel/source interface effectively. Consequently, higher tunnelling rate of electron can be gained to have steep and high ON current along with advancement in threshold voltage (V_{th}). By using such design technique, a much improved SS (<5 mV/dec) is achieved at very low supply voltage (V_{ds}) as compared with conventional device. Such steeper SS can also be achieved by impact ionisation MOS (I-MOS), but the problem with this device is the requirement of very high supply voltage for avalanche breakdown for having desired steepness in transfer characteristics. Hence, aforementioned features show suitability of the proposed structure for ultra-small power analogue operations.

2. Structure dimensions and simulation setup: Cross-sectional pictures of dopingless TFET and proposed MA-DL-TFET are presented in Figs. 1*a* and *b*, respectively. In MA-DL-TFET, depth and length of HML are $T_{HML} = 1$ nm and $L_{HML} = 6$ nm, respectively, as illustrated in Fig. 2*a*. In a similar way, depth and length of VML are taken as $T_{VML} = 2$ nm and $L_{VML} = 1$ nm, respectively, for easy deposition inside the dielectric region. Further structure specifications and dimensions applied in TCAD simulation of both the devices are presented in Table 1. In addition to these structural characteristics, Shockley–Read–Hall recombination, non-local BTBT, trap-assisted tunnelling and Auger recombination models are enabled for ATLAS 2D device simulator [15].

3. Results and discussion: This section consists of comparative analysis of devices in the terms of DC/RF characteristics and linear behaviour.

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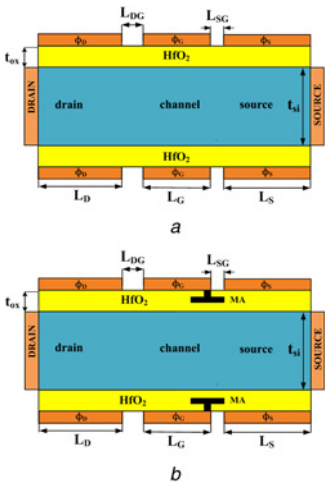

Fig. 1 *Schematic cross-section of*
a Dopingless TFET
b Metal angle dopingless TFET

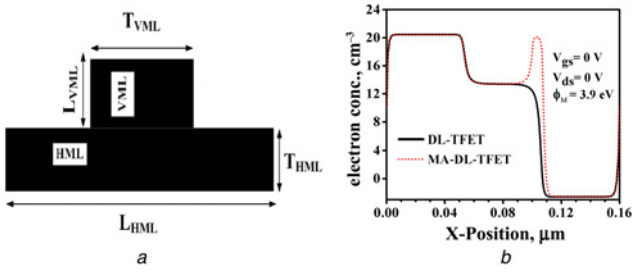

Fig. 2 *Graphical view of*
a Metal angle
b Deviation in electron concentration of devices under thermal equilibrium state

Table 1 Structural characteristics and size for different devices

Parameters name	Symbol	DL-TFET	MA-DL-TFET
wafer doping concentration	n_i	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}
length of source electrode	L_S	53 nm	53 nm
length of drain electrode	L_D	50 nm	50 nm
length of gate electrode	L_G	50 nm	50 nm
spacer thickness between source/gate electrode	L_{SG}	2 nm	2 nm
spacer thickness between drain/gate electrode	L_{DG}	5 nm	5 nm
silicon wafer depth	t_{si}	10 nm	10 nm
dielectric depth	t_{ox}	3 nm	3 nm
work-function of drain electrode	ϕ_D	3.9 eV	3.9 eV
work-function of gate electrode	ϕ_G	4.53 eV	4.53 eV
work-function of source electrode	ϕ_S	5.93 eV	5.93 eV
work-function of MA	ϕ_M	—	3.9 eV

3.1. DC characteristics: Abruptness at channel/source junction is an essential requirement for having steeper transfer characteristics of DL-TFET. In this concern, proposed structure (Fig. 1*b*) consists of an implanted MA of 3.9 eV work-function inside dielectric region near channel/source junction to have much improved DC characteristics. Fig. 2*b* depicts electron concentration deviation for devices (DL-TFET and MA-DL-TFET) in thermal state. Here, MA implantation produces the nozzle in electron concentration near channel/source joint for proposed device compared with DL-TFET. Similarly, Figs. 3*a* and *b* display energy band deviation of devices in thermal and ON states, respectively. Deposition of MA creates a notch in energy bands (conduction and valence) at channel/source interface for modified structure depicted in Figs. 3*a* and *b*. Development of such notch defines high density of electrons at channel/source interface for boosted tunnelling rate of electrons. Implantation of metal layers (VML and HML) in MA-DL-TFET causes increment in electric field below MA at channel/source junction as presented in Fig. 4*a*. Such boosted electric field near channel/source junction is an essential requirement for having enhanced tunnelling rate of electrons at same interface. In this regard, a comparative analysis between transfer characteristics of TFETs is illustrated in Fig. 4*b*. Here, much higher ON current (I_{ON}) with improved threshold voltage (V_{th}) and SS is gained for proposed device compared with conventional structure. DC characteristics extracted from Fig. 4*b* for both TFETs are presented in Table 2. Likewise, variations in energy band of TFETs for distinct values of V_{gs} are demonstrated in Figs. 5*a* and *b*, respectively. Here, it can be observed that increase in V_{gs} pushes energy bands downward for reducing tunnelling barrier at channel/source interface.

The presence of MA in modified structure decreases tunnelling barrier width at channel/source joint. Such placement of MA raises alignment of conduction band of channel with valance band of source for low values of V_{gs}. In addition to these, impact of energy band alignment for distinct magnitudes of V_{gs} upon

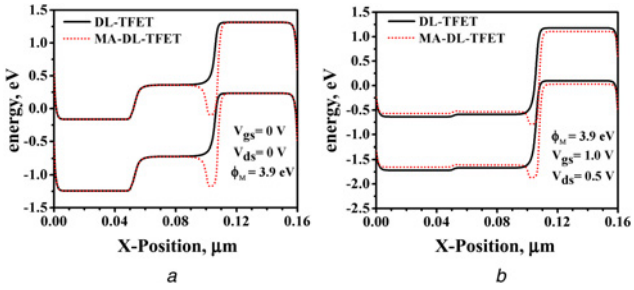

Fig. 3 *Energy band variation for both TFETs under*
a Thermal equilibrium
b ON state

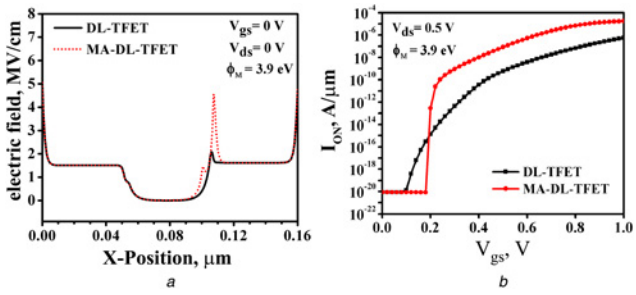

Fig. 4 *Deviation in*
a Electric field under thermal equilibrium state
b I_{ON}–V_{gs} characteristics for both TFETs

Table 2 DC characteristic analysis of devices

Parameters name	Symbol, unit	DL-TFET	MA-DL-TFET
ON current	I_{ON}, A/µm	5.71×10^{-7}	1.82×10^{-5}
leakage current	I_{OFF}, A/µm	8.63×10^{-21}	8.73×10^{-21}
sub-threshold swing	SS, mV/dec	13.6	4.37
threshold voltage	V_{th}, V	0.83	0.50

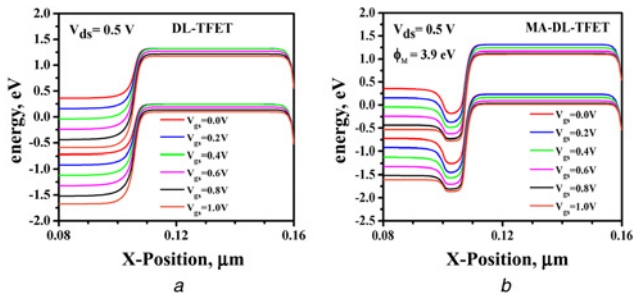

Fig. 5 *Energy band deviation for*
a DL-TFET
b MA-DL-TFET at different V_{gs}

electron tunnelling rate (ETR) can be visualised in Fig. 6*a*. In addition to ETR, current density of electron (J_n) under ON state for both the devices can be realised as shown in Fig. 6*b*. Here, J_n is much higher in channel and drain regions for the modified device in comparison with DL-TFET. Implantation of MA inside the proposed structure is the reason for high J_n.

3.2. Analogue/RF characteristics: For current scenario of deep micron devices, improved analogue and RF performance is an essential need for designing and modelling of high-frequency devices. Therefore, crucial analogue/RF characteristics such as transconductance (g_m), parasitic capacitance between gate/drain electrode (C_{gd}), cut-off frequency (f_T), maximum oscillating frequency (f_{max}), gain–bandwidth product (GBP), transit time (τ) and transconductance generation factor (TGF) are needed to be calculated for analysis of device performance. Here, transconductance (g_m) defines the capability of the transistor for converting minute changes in V_{gs} into the drain current. For having large bandwidth of an operational amplifier for RF operations, transconductance should be large enough. Fig. 7*a* illustrates transconductance

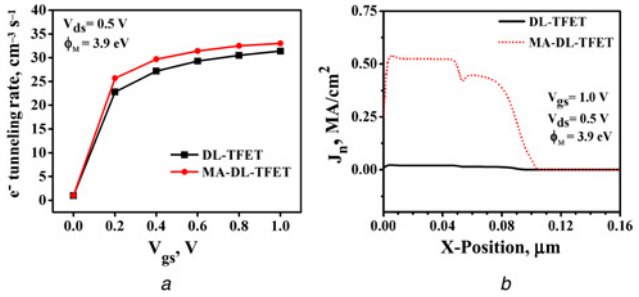

Fig. 6 *Graphical representation of*
a Electron tunneling rate
b Electron current density (J_n) for both TFETs

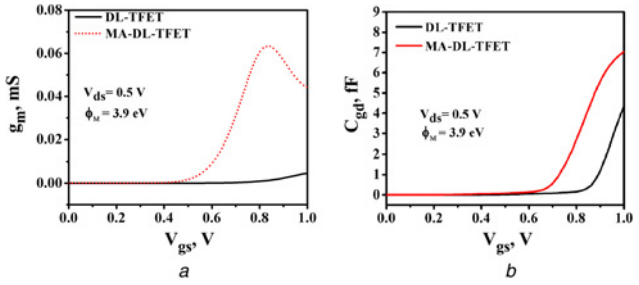

Fig. 7 *Deviation of*
a g_m
b C_{gd} for both devices

(g_m) variation for both TFETs. For proposed device, g_m increases rapidly after 0.6 V of V_{gs} and attain highest magnitude of 0.063 mS for 0.84 V. Further increase in V_{gs} results into the fall of g_m because of mobility deterioration of charges.

Here, a very high transconductance is gained for MA-DL-TFET compared with conventional structure at low value of V_{gs}. C_{gd} is an undesired capacitance, and it should be minimum for gaining high switching speed in high-frequency circuit. Its magnitude is dependent on parameters such as doping of channel, depletion width and L_{DG}. It acts like inversion and parasitic capacitances for large and small magnitudes of gate supply voltage, respectively [16]. Variation in C_{gd} with V_{gs} for both the structures is illustrated in Fig. 7*b*. Here C_{gd} is at higher side for the proposed structure because of MA placement. Although value of C_{gd} is higher for the proposed device, much higher g_m of the proposed structure suppresses the consequences of C_{gd} on other analogue/RF characteristics. In analogue performance, f_t has an huge role for estimating the device RF responses. f_t is the frequency at which short-circuit current gain of device become unit value [17], and presented as

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \tag{1}$$

Fig. 8*a* presents changes in f_T w.r.t. V_{gs} for both TFETs. Here, MA-DL-TFET has much improved f_T than DL-TFET due to enhanced transconductance. For MA-DL-TFET, f_T increases and attains highest value of 4.33 GHz for $V_{gs} = 0.7$V. After this value of V_{gs}, f_T decreases, because of mobility deterioration of charges and increment in C_{gd}. Similar approach is used to demonstrate GBP of TFETs as shown in Fig. 8*b*. Nature of GBP can be understood by the expression given below:

$$\text{GBP} = \frac{g_m}{20\pi(C_{gs} + C_{gd})} \tag{2}$$

f_{max} is defined as the frequency at which power gain drops to unit value. f_{max} is presented as

$$f_{max} = \sqrt[2]{\frac{f_T}{8\pi C_{gd} R_{gd}}} \tag{3}$$

Here dependency of f_{max} on C_{gs}, C_{gd} and g_m is understood by visualising the above-mentioned equation. Fig. 9*a* presents changes in f_{max} w.r.t. V_{gs}. Here, f_{max} of 0.68 MHz is achieved for MA-DL-TFET, it is very higher than f_{max} of conventional device. Very high g_m and moderate C_{gd} are the reasons for improved analogue performance of the proposed structure in comparison with conventional device.

TGF is an important characteristic which reflects the device efficiency to convert DC parameter (drain current) into the AC parameter (g_m).

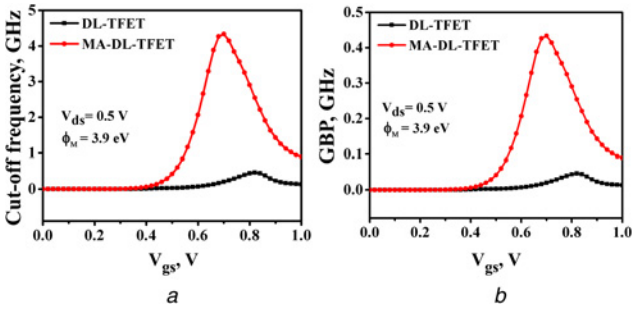

Fig. 8 *Deviation in*
a f_T
b GBP for both TFETs

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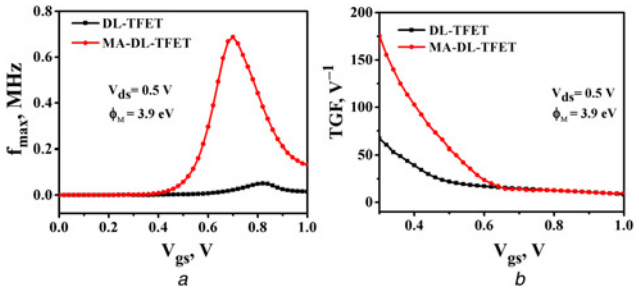

Fig. 9 *Deviation on*
a f_{max}
b TGF w.r.t. V_{gs} for both TFETs

TGF is plotted on graph from $V_{gs} = 0.3$ V, because of unimportant current below this value as depicted in Fig. 9*b*. Proposed structure is having highest magnitude of TGF at $V_{gs} = 0.3$ V. Increase in V_{gs} above 0.3 V originates from degradation in TGF for devices because of dominance of driving current on g_m at $V_{gs} = 0.3$ V. Transit time (τ) defines the time duration of charge carriers to be removed from channel. τ decides state transition quickness of device and presented as $\tau = 1/(2f_t\pi)$. Fig. 10*a* demonstrates variation of τ with V_{gs} for TFETs. In this figure, τ of proposed structure decreases sharply for increasing value of V_{gs} since f_t is dependent on V_{gs}. The low value of τ of MA-DL-TFET shows reduced sweep time of it in comparison to DL-TFET.

3.3. Linearity analysis: High signal-to-noise ratio is an essential need for enhanced characteristics of the device. In this concern, superior linear response of the device is a benchmark for distortionless output. For this, g_m is needed to be the constant for entire input voltage range. However in practical, g_m deviation is observed for TFET and MOS devices with variation in V_{gs}. Hence, linear characteristics such as g_{m3}, V_{IP2}, V_{IP3}, IIP3 and IMD3 are subjected for linearity measurement of devices. These characteristics are mathematically expressed as

$$V_{IP2} = 4 \times \left(\frac{g_{m1}}{g_{m2}}\right), \quad g_{mn} = \frac{1}{n!}\frac{\delta^n I_{ds}}{\delta V_{gs}^n} \tag{4}$$

$$V_{IP3} = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m3}}\right)} \tag{5}$$

$$\text{IIP3} = \frac{2}{3} \times \left(\frac{g_{m1}}{g_{m3} \times R_s}\right) \tag{6}$$

$$\text{IMD3} = \left[\frac{9}{2} \times g_{m3} \times (V_{IP3})^2\right]^2 \times R_s \tag{7}$$

Here value of R_s is 50 Ω for RF applications. Third-order transconductance coefficient (g_{m3}) deviation with V_{gs} is presented in Fig. 10*b*. Here, high magnitude of g_{m3} describes large nonlinearity of the device, which is minimum for MA-DL-TFET in comparison to DL-TFET. Simultaneously, position of operating point (DC) near zero crossover mark is also essential for linearity enhancement. Modified structure is having smaller zero crossover mark for defining improved linearity in comparison to DL-TFET. V_{IP2} presents the hypothesised input voltage for which first- and second-order harmonic voltages are same. MA-DL-TFET is having the highest magnitude of V_{IP2} in comparison to DL-TFET as presented in Fig. 11*a*. Similarly, V_{IP3} presents the hypothesise input voltage for which first- and third-order harmonic voltages are same.

High magnitudes of V_{IP2} and V_{IP3} are essential for advancement in linearity performance of the structure. High V_{IP3} at a smaller value of V_{gs} for MA-DL-TFET in comparison with DL-TFET is illustrated. Fig. 12*a* presents IIP3 deviation with V_{gs} and depicts high IIP3 for MA-DL-TFET in comparison to DL-TFET.

Implantation of MA is the reason for improved IIP3 for MA-DL-TFET. Inter-modulation distortion (IMD3) is an linearity characteristic which describes hypothesised inter-modulation current at which first- and third-order inter-modulation harmonic currents are same [18]. Low value of IMD3 is needed for distortion less system. Fig. 12*b* shows the smaller magnitude of IMD3 for modified structure in comparison with conventional device.

4. Optimisation: In this section, optimisation of MA-DL-TFET is performed by inspecting HML length (L_{HML}) and MA work-function (ϕ_M) deviation. Effect of deviation in L_{HML} on device characteristics is much necessary for MA implantation inside the device. Fig. 13*a* depicts deviation in I_{ON}–V_{gs} characteristics of MA-DL-TFET for the different L_{HML}. It illustrates non-countable deviation in I_{ON}, V_{th}, SS for different L_{HML} and values are presented in Table 3. However, slight increase in C_{gd} is detected with increase in L_{HML} as exhibited in Fig. 13*b*. Simultaneously, a slight degradation of cut-off frequency for increase in L_{HML} is shown in Fig. 13*c*.

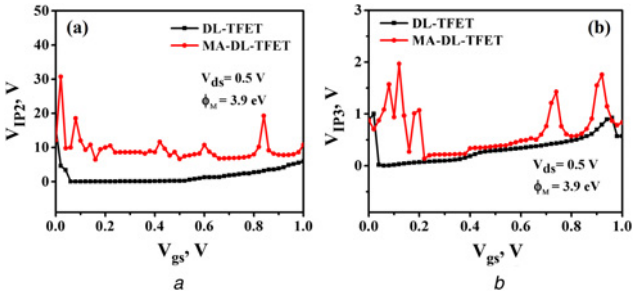

Fig. 11 *Deviation in*
a V_{IP2}
b V_{IP3} w.r.t. V_{gs} for TFETs

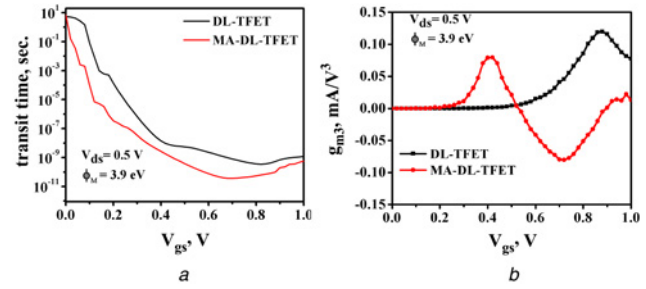

Fig. 10 *Deviation of*
a τ
b g_{m3} w.r.t. V_{gs} for both TFETs

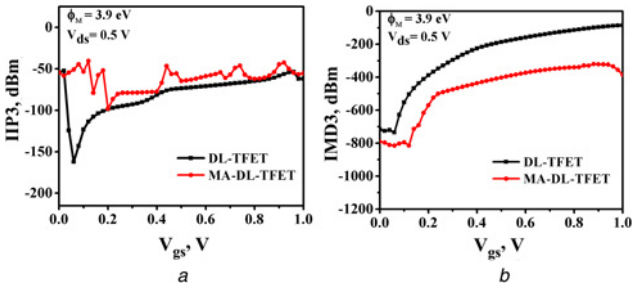

Fig. 12 *Deviation of*
a IIP3 (dBm)
b IMD3 (dBm) w.r.t. V_{gs} for TFETs

In addition to L_{HML} variation, outcome of ϕ_M deviation on DC/RF parameter is very important to have improved performance. Fig. 14*a* shows transfer characteristics of modified structure for various ϕ_M. Here, slight degradation of I_{ON} is detected for increasing value of ϕ_M.

Other parameters such as SS and V_{th} show negligible dependency towards ϕ_M variation as illustrated in Table 4. Simulated results give us the adaptability to choose different ϕ_M for easy fabrication steps. Fig. 14*b* illustrates variation in C_{gd} w.r.t. ϕ_M. Here, slight degradation of C_{gd} is detected with increasing value of ϕ_M. In addition to these, Fig. 14*c* shows negligible advancement in f_T with the increase in ϕ_M and such thing happens due to decrement in C_{gd}.

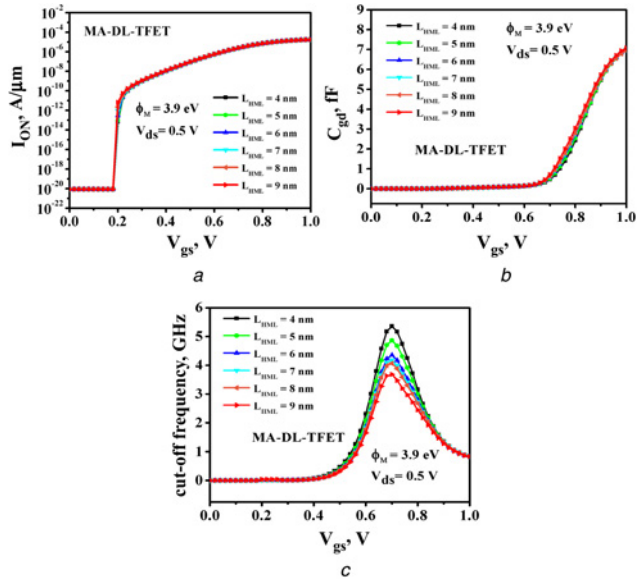

Fig. 13 *Deviation in*
a I_{ON}–V_{gs} characteristics
b C_{gd}, *(c)* f_T of MA-DL-TFET for various L_{HML}

Table 3 L_{HML} variation of MA-DL-TFET

L_{HML}, nm	I_{ON}, mA	I_{OFF}, A	V_{th}, V	SS, mV/dec
4	1.82×10^{-2}	8.72×10^{-21}	0.51	4.78
5	1.82×10^{-2}	8.73×10^{-21}	0.5	4.59
6	1.82×10^{-2}	8.73×10^{-21}	0.5	4.37
7	1.82×10^{-2}	8.73×10^{-21}	0.5	4.29
8	1.82×10^{-2}	8.73×10^{-21}	0.5	4.17
9	1.82×10^{-2}	8.73×10^{-21}	0.5	4.11

Table 4 ϕ_M variation of MA-DL-TFET

ϕ_M, eV	I_{ON}, mA	I_{OFF}, A	V_{th}, V	SS, mV/dec
3.7	1.90×10^{-2}	8.74×10^{-21}	0.5	4.15
3.8	1.87×10^{-2}	8.73×10^{-21}	0.5	4.28
3.9	1.82×10^{-2}	8.73×10^{-21}	0.5	4.37
4.0	1.75×10^{-2}	8.72×10^{-21}	0.51	4.48
4.1	1.68×10^{-2}	8.71×10^{-21}	0.51	4.54
4.2	1.58×10^{-2}	8.70×10^{-21}	0.51	4.69

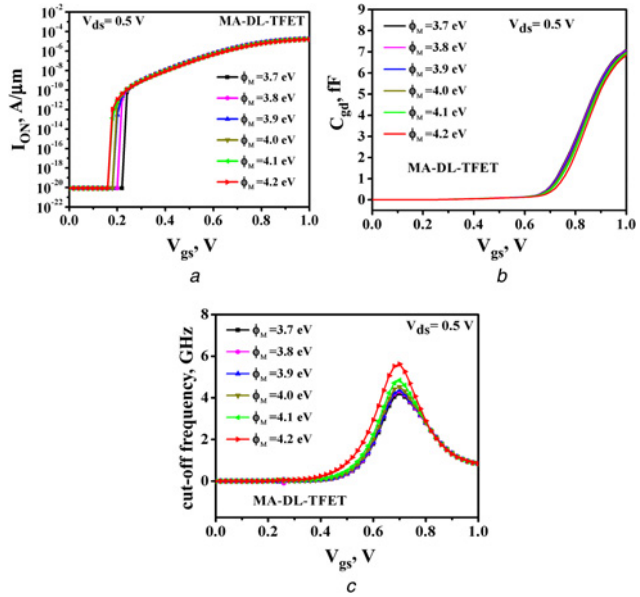

Fig. 14 *Deviation in*
a I_{ON}–V_{gs} characteristics
b C_{gd}
c f_T of MA-DL-TFET for various ϕ_M

5. Circuit level performance of the devices: This section presents performance evaluation of both TFETs for circuit applications. In this concern, inverter amplifiers are designed by using these TFETs. Due to the absence of correct analytical models for TFETs, a lookup table-dependent Verilog-A models are developed for implementing these devices at circuit level. This approach is very feasible for determining circuit level performance of new emerging structures, which has no proper model for its I_{ON}–V_{gs} characteristics [19, 20]. Here, TCAD data obtained from device parameters is used to develop lookup table based model for calculating *V–I* and *V–C* characteristics of the devices. Inverter amplifier containing N- and P-type structures is depicted in Fig. 15*a*.

Noise margin (NM) evaluation is performed through butterfly graph, achieved by combining the voltage transfer characteristics (VTCs) and inverse VTCs [19]. Figs. 15*b* and *c* show the NM calculation for DL-TFET and MA-DL-TFET, respectively. Here,

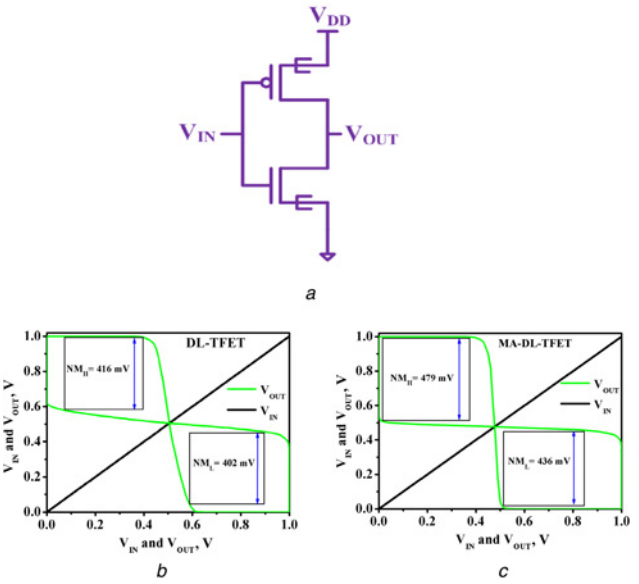

Fig. 15 *Graphical representation of*
a Inverter
b Butterfly curves of DL-TFET-based inverters
c Butterfly curves of MA-DL-TFET-based inverters for measuring NM

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Table 5 Inverter parameters for different TFETs

Parameters, unit	DL-TFET	MA-DL-TFET
τ_{PLH}, ps	384	309
τ_{PHL}, ps	104	41
τ_P, ps	244	175
τ_r, ps	791	657
τ_f, ps	511	374
NM_L, mV	402	436
NM_H, mV	416	479

MA-DL-TFET shows much improved NM than DL-TFET. In addition to NM calculation, transient response based inverter characteristics such as propagation delay (τ_P), high to low delay time (τ_{PHL}), low to high delay time (τ_{PLH}), fall time (τ_f) and rise time (τ_r) are calculated and demonstrated in Table 5. By observing characteristics in Table 5, it can be said that MA-DL-TFET has much improved performance than conventional device for low power applications.

6. Conclusion: Dopingless devices experience degraded DC and high-frequency characteristics due to less charge density at channel/source interface. Therefore, in MA-DL-TFET, MA of 3.9 eV work-function is implanted within the dielectric region nearby channel/source to diminish the tunnelling barrier. Consequently, high ETR from source end to channel region is earned to attain improvement in steepness and ON current with reduction in V_{th}. Implantation of MA also raises RF characteristics of MA-DL-TFET because of much higher g_m. Further, optimisation of HML length (L_{HML}) and MA work-function (ϕ_M) are presented to easy fabrication steps. It also facilitates to adopt varies sizes and ϕ_M for attaining optimal device performance.

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8. References

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