Passive voltage amplification in non-leaky ferroelectric–dielectric heterostructure

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This work presents the effect of ferroelectric thickness variation on properties (negative capacitance stabilisation, voltage amplification and capacitance enhancement) of ferroelectric–dielectric (FE–DE) heterostructure. For a better understanding of heterostructure, the study has analysed isolated ferroelectric capacitor first. Results clearly indicate the unstable nature of negative capacitance in ferroelectric capacitor. This negative capacitance can be stabilised by adding a dielectric capacitor in series with ferroelectric capacitor. Dielectric capacitor not only stabilises the negative capacitance state but is also responsible for the increase in capacitance of heterostructure. Afterwards dynamic response of FE–DE hetrostructure is studied. It is observed that thickness has strong dependence on ferroelectric parameters. With the increase in ferroelectric thickness, ferroelectric capacitance decreases and hence leads to voltage amplification. However, ferroelectric thickness should not be increased beyond critical thickness, as beyond critical thickness voltage amplification cannot be achieved without hysteresis.

1. Introduction: Rapid scaling in complementary metal–oxide–semiconductor industry has diminished gate control over the channel and hence has instigated the increase in power dissipation. Power dissipation has two main components, namely dynamic and static power dissipation. Reducing the supply voltage can be an effective measure to truncate dynamic power dissipation ($P_{\text{dyn}} \propto V_{DD}^2$), however reduction in V_{DD} leads to decrement in ON current and hence speed of transistor. So in order to maintain sufficient speed and ON current, $I_{\text{on}} \propto (V_{DD} - V_T)^{\alpha}$ (where α is 1–2) threshold voltage should be reduced. Lowering the threshold voltage leads to increment in OFF current ($I_{\text{OFF}} \propto 10^{-V_T/S}$) [1] and hence increment in static power dissipation of transistor ($P_{\text{OFF}} \propto I_{\text{OFF}}$). This contradicting requirement suggests that trade-off between performance and power dissipation always exists. However, one possible way to mitigate this problem is to reduce the subthreshold swing (SS) of the device. Reduction in SS allows the scaling of V_{DD} and V_T simultaneously without any compromise in performance and power dissipation. However, SS of classical field-effect-transistor (FET) cannot be reduced below the Boltzmann limit which is 60 mV/decade. This inability to reduce SS [2, 3] below Boltzmann limit is an important and enduring challenge. As a result, worldwide search for finding an ideal switch [4] that can overcome Boltzmann tyranny [5] and provide SS below 60 mV per decade is in progress. Ferroelectric oxide which owns the property of negative capacitance [6–9] can overcome the Boltzmann tyranny and reduce SS below 60 mV/decade [10–19]. However, negative capacitance state in ferroelectric oxide is unstable in nature [20]. This unstable nature of negative capacitance can be stabilised by adding a positive dielectric oxide in series with it (with certain conditions which are discussed afterwards). Ferroelectric oxide when used as gate oxide modifies the body factor (makes body factor less than one) and therefore reduces the SS below 60 mV/decade. This potential merit of reduced SS in conventional FET encourages us to study the ferroelectric–dielectric (FE–DE) heterostructure. Three important aspects of FE–DE heterostructure, capacitance enhancement [21], negative capacitance stabilisation and voltage amplification [22] have been studied. Schematic and circuit equivalent non-leaky FE–DE heterostructure is shown in Fig. 1. Presence of resistive component makes the capacitor leaky in nature, however still we are considering heterostructure as non-leaky, because resistive and capacitive components are independent of each other (means it is possible to have two different potentials at nodes A and B) and potential at node A is unaffected by the presence of resistance and solely depend on capacitance values. Recently, Khan *et al.* [20] have explored important aspects of leaky and non-leaky FE–DE heterostructure. However, in this Letter, we have restricted ourselves to the study of non-leaky heterostructure. In this non-leaky heterostructure, we have considered lead zirconium titanate (PZT, $PbZr_{0.43}Ti_{0.57}O_3$) and SiO_2 as ferroelectric and dielectric material, respectively. Properties of heterostructure have been analysed by varying ferroelectric thickness from 30 to 120 nm. With the increase in thickness of ferroelectric film, capacitance of isolated ferroelectric capacitor decreases which is responsible for voltage amplification and capacitance enhancement in heterostructure. PZT has been considered as it possesses several advantages over other ferroelectric materials like robustness towards film thickness variation, sufficient polarisation at low ferroelectric thickness. Also other advantages include reliability, high value of dielectric constant and most important nanosecond polarisation reversal [23]. SiO_2 has been selected because of ease of developing on silicon substrate by just oxidising the silicon wafer.

2. Isolated ferroelectric capacitor: When a voltage source is connected to isolated ferroelectric capacitor (shown in Fig. 2*a*), as per LK equation, relation between voltage across ferroelectric and charge across ferroelectric can be expressed as

$$V_{\text{F}} = \rho \frac{\text{d}Q_{\text{F}}}{\text{d}t} + \alpha Q_{\text{F}} + \beta Q_{\text{F}}^3 \tag{1}$$

where ρ is frictional inertia of the system. V_{F} and Q_{F} are voltage and charge across FE capacitor, respectively. α and β are anisotropy constants which are given by

$$\alpha = \frac{-3\sqrt{3}}{2}\frac{V_{\text{C}}}{Q_{\text{O}}} \quad \text{and} \quad \beta = \frac{3\sqrt{3}}{2}\frac{V_{\text{C}}}{Q_{\text{O}}^3} \tag{2}$$

V_{C} is coercive voltage and Q_{O} is remanent charge in ferroelectric material. Under steady-state condition, (1) can be expressed as

$$V_{\text{F}} = \alpha Q_{\text{F}} + \beta Q_{\text{F}}^3 \tag{3}$$

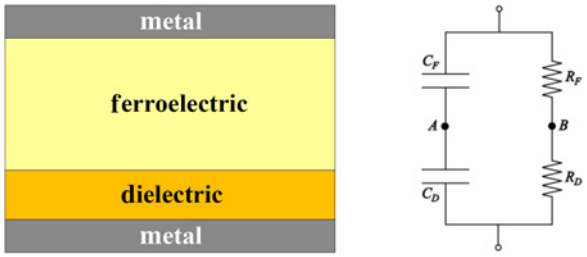

Fig. 1 *Schematic and circuit configuration of FE–DE heterostructure*

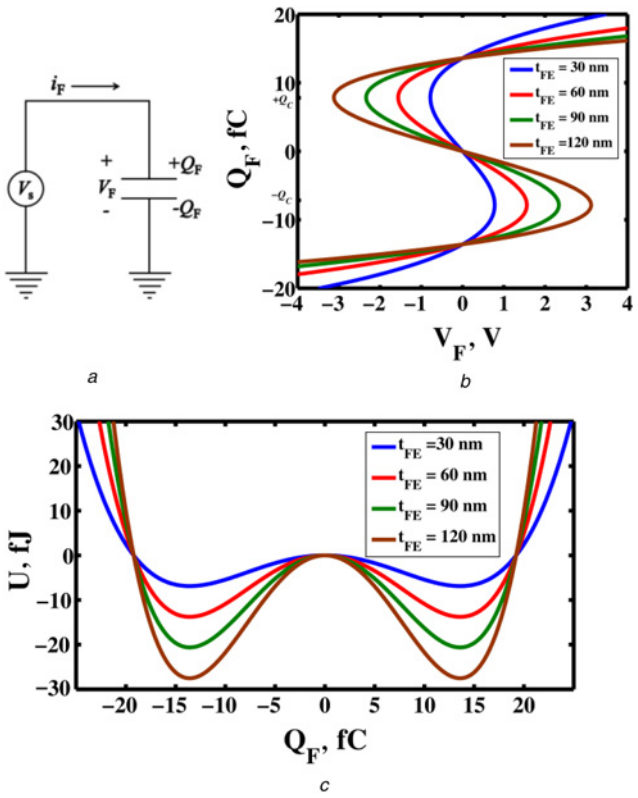

Fig. 2 *Response of isolated ferroelectric capacitor*
a Schematic of isolated ferroelectric capacitor connected to voltage source
b Charge versus voltage characteristics of isolated ferroelectric capacitor with different ferroelectric thickness
c Energy landscape for isolated ferroelectric capacitor with different ferroelectric thickness

Differentiating (2) with respect to Q_F results in ferroelectric capacitance which is given by the equation below:

$$C_F = \frac{dQ_F}{dV_F} \simeq \frac{1}{\alpha} = \frac{-2}{3\sqrt{3}}\frac{Q_O}{V_C} \tag{4}$$

Fig. 2*b* shows S-shaped, charge versus voltage characteristics of isolated ferroelectric capacitor in steady state at different ferroelectric thickness, which is obtained by solving (2). The slope of charge versus voltage characteristics is negative in between Q_C and $-Q_C$, where $Q_C = \sqrt{-\alpha/3\beta}$. Negative slope confirms negative capacitance in ferroelectrics as when voltage is increasing charge is decreasing in ferroelectric material. This negative slope is unstable at every thickness value of ferroelectric capacitor. Also as the thickness is increased ferroelectric capacitance starts decreasing which is evident from Fig. 2*b*. In all the calculations, we have used coercive field (E_C) and remanant polarisation (P_r) as 260 kV/cm and 30.2 μC/cm^2, respectively [24]. The thickness of ferroelectric oxide is varied from 30 to 120 nm in an interval of 30 nm. Area of capacitor plate is $A = 45\ \text{nm} \times 1\ \mu\text{m}$. For ferroelectric material free energy U can be expressed as even-order polynomial of charge Q_F

$$U = \frac{\alpha}{2}Q_F^2 + \frac{\beta}{4}Q_F^4 - Q_F V_F \tag{5}$$

Fig. 2*c* shows the double-well energy landscape of ferroelectric capacitor at different ferroelectric thickness. In double-well landscape if we try to put charge or polarisation on the top of the barrier it will fall down to one of the minima, hence confirming the unstable nature of isolated ferroelectric capacitor as discussed earlier. Results clearly indicate that $Q_F = 0$ is dynamically unstable solution. For stabilising the negative capacitance state in ferroelectric capacitor, dielectric capacitor is connected in series with it. Simulation results for this heterostructure have been discussed in the next section.

3. Ferroelectric capacitor connected in series with dielectric capacitor: The voltage source is connected to series combination of ferroelectric and dielectric capacitor as shown in Fig. 3*a*. For dielectric capacitor, thickness and dielectric constant are taken as 1 nm and 4, respectively. Negative capacitance in ferroelectric oxide can be stabilised if dielectric capacitance is less than negative of inverse of anisotropy constant ($C_D < -1/\alpha$) [15]. Dimension of dielectric capacitor ensures that $C_D < -1/\alpha$ or $C_D < |C_F|$ and makes negative capacitance state stable. Since it is the series combination of ferroelectric and dielectric capacitor, same amount of charge accumulates across both the capacitors, hence ($Q_F = Q_D$), also by Kirchhoff's voltage Law (KVL) applied voltage is equivalent to sum of voltage drop across ferroelectric and dielectric

$$V_S = V_F + V_D \tag{6}$$

$$V_F = \rho\frac{dQ_F}{dt} + \alpha Q_F + \beta Q_F^3 \tag{7}$$

$$V_D = \frac{Q_D}{C_D} = \frac{Q_F}{C_D} \tag{8}$$

$$V_S = \rho\frac{dQ_F}{dt} + \left(\alpha + \frac{1}{C_D}\right)Q_F + \beta Q_F^3 \tag{9}$$

Fig. 3*b* shows charge versus voltage characteristics of FE–DE heterostructure for different ferroelectric thickness in steady-state condition. Charge versus voltage characteristics of heterostructure do not contain any negative slope region ensuring hetrostructure is in positive capacitance state. Also due to series combination of capacitors same charge accumulates across both DE and FE capacitors, therefore for a particular value of charge, total energy (U) of heterostructure is equal to the sum of individual energy of ferroelectric (U_F) and dielectric capacitors (U_D)

$$U = U_F + U_D \tag{10}$$

$$U = \frac{\alpha}{2}Q_F^2 + \frac{\beta}{4}Q_F^4 - Q_F V_F + \frac{Q_F^2}{C_D} \tag{11}$$

Fig. 3*c* shows energy landscape for FE–DE hetrostructure at different ferroelectric thickness. The series combination of ferroelectric and dielectric capacitor minimises the total energy of system and hence stabilises negative capacitance state which is evident from the above figure. Also when a dielectric capacitor is added in series with ferroelectric capacitor, the double well in energy landscape will approach near to each other, as a result of which curve becomes flatter in nature leading to increase in capacitance of the heterostructure which is evident from flatness of energy landscape. (capacitance can be related to energy by relation: $1/C = (d^2U/dQ^2)$). Flatness in energy landscape is more at higher

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thickness; so at higher thickness capacitance enhancement of hetrostructure is more. This increase in the capacitance is violation of laws of electrostatics and circuit theory because in series combination of two positive capacitors, total capacitance will always be smaller than each one of them. Violation of this classical law can only be explained only if one of the capacitance is negative. Combination of both the capacitance is given by

$$\frac{1}{C}=\frac{1}{C_{\mathrm{F}}}+\frac{1}{C_{\mathrm{D}}} \tag{12}$$

Here C can be larger than C_{D} if C_{F} is negative in nature and $|C_{\mathrm{F}}| > C_{\mathrm{D}}$. Fig. 3*d* shows capacitance versus voltage characteristics of FE–DE heterostructure for different ferroelectric thickness. Capacitance enhancement can be observed in the figure, as combination of FE and DE capacitance is greater than dielectric capacitance which is only possible when one of the capacitance in negative. Results clearly indicate that $Q_{\mathrm{F}}=0$ is now a stable solution. Simulation results for FE–DE heterostructure conclude that state of negative capacitance in FE–DE heterostructure is stable in nature.

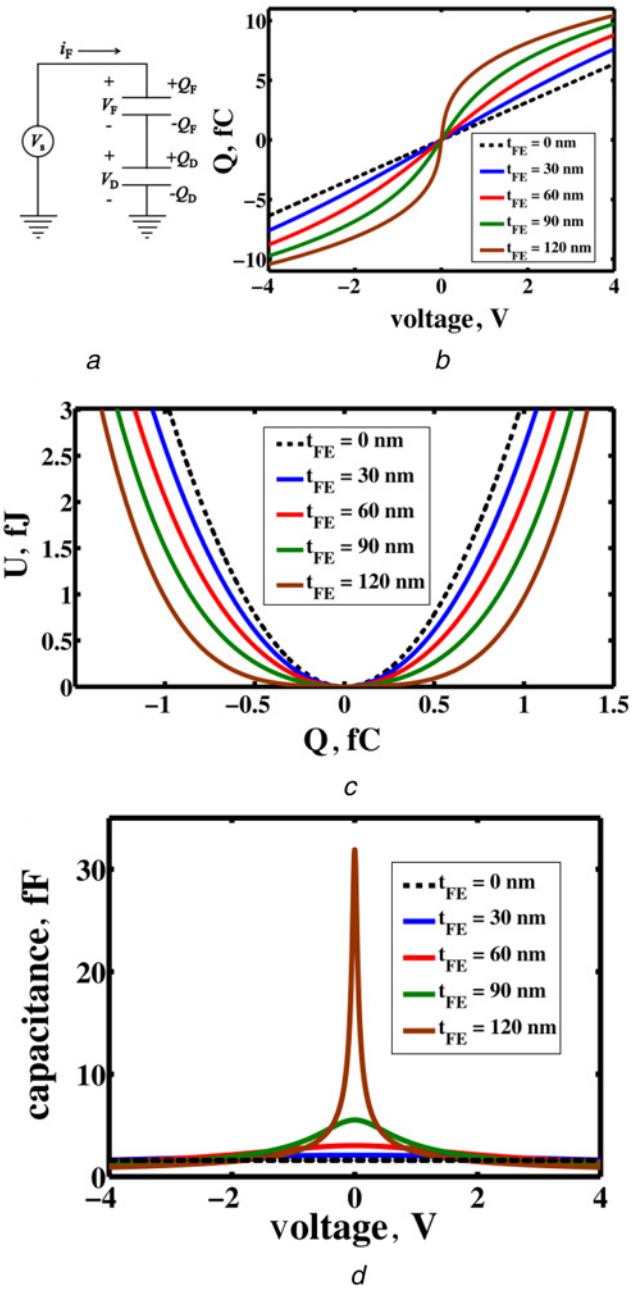

Fig. 3 *Response of FE-DE heterostructure*
a Series combination of FE–DE capacitor connected to voltage source
b Charge versus voltage characteristics of FE–DE heterostructure with different ferroelectric thickness
c Capacitance versus voltage for FE–DE heterostructure
d Energy landscape for FE–DE heterostructure with different ferroelectric thickness

4. Analysis of dynamic response: This section deals with dynamic response of FE–DE heterostructure. Dynamic response of heterostructure is obtained by solving (9) when a triangular pulse of frequency 100 MHz is applied at the input of heterostructure. Variation in charge with respect to time is shown in Fig. 4*a*, also voltage variation across dielectric capacitor with respect to time is shown in Fig. 4*b*. The relation between voltage across dielectric capacitor, ferroelectric capacitor and supply voltage can be written as

$$V_{\mathrm{D}}=V_{\mathrm{S}}-V_{\mathrm{F}} \tag{13}$$

$$V_{\mathrm{D}}=V_{\mathrm{S}}\times\left(1-\frac{V_{\mathrm{F}}}{V_{\mathrm{S}}}\right) \tag{14}$$

Solving further results in relation between V_{D} and V_{S} as

$$V_{\mathrm{D}}=V_{\mathrm{S}}\times\frac{C_{\mathrm{F}}}{C_{\mathrm{F}}+C_{\mathrm{D}}} \tag{15}$$

$$V_{\mathrm{D}}=V_{\mathrm{S}}\times\frac{|C_{\mathrm{F}}|}{|C_{\mathrm{F}}|-C_{\mathrm{D}}} \tag{16}$$

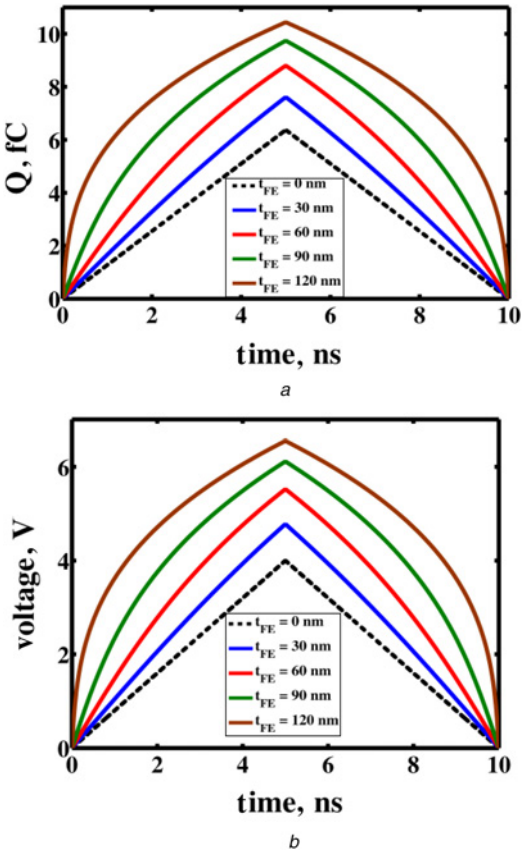

Fig. 4 *Dynamic response of heterostructure*
a Charge across FE–DE heterostructure at different ferroelectric thickness
b Voltage across FE–DE heterostructure at different ferroelectric thickness

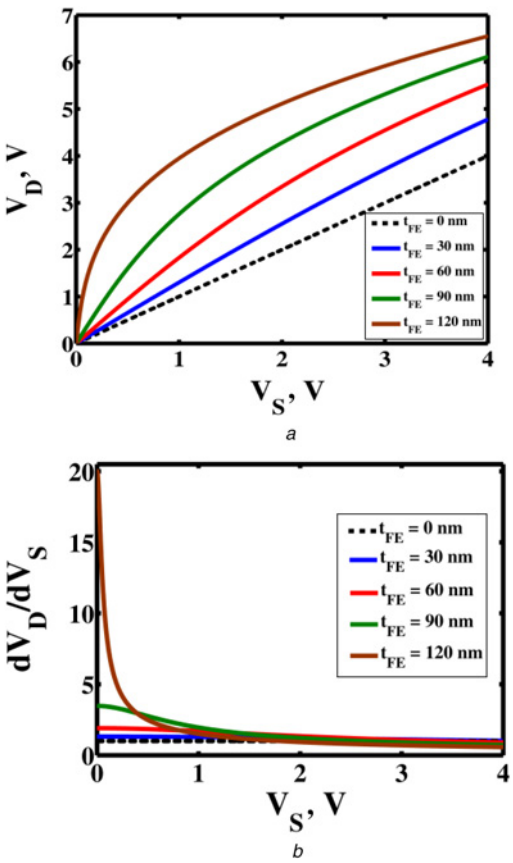

Fig. 5 *Voltage amplification in heterostructure*
a Voltage across dielectric versus supply voltage for FE–DE hetrostructure at different ferroelectric thickness
b Differential voltage amplification in FE–DE heterostructure at different ferroelectric thickness

This equation shows that V_D can be greater than V_S when $|C_F| > C_D$, which means smaller amount of change in V_S will induce large amount of change in V_D. Results clearly show that the voltage across dielectric is greater than the applied voltage; hence it justifies passive voltage amplification in FE–DE heterostructure. Fig. 5*a* shows plot of voltage across dielectric (V_D) versus supply voltage (V_S). It is clearly visible that increase in thickness leads to higher voltage amplification, but thickness cannot be increased arbitrarily, it has to be limited up to critical thickness, i.e. thickness of ferroelectric oxide should be less than the critical thickness. The condition for voltage amplification ($|C_F| > C_D$) or ($C_D < -1/\alpha$) provides the value of critical thickness for this FE–DE heterostructure. This critical thickness has been expressed in the following equation:

$$t_C = \frac{2}{3\sqrt{3}} \times \frac{Q_O}{E_C \times C_D} \tag{17}$$

where t_C is the critical thickness of ferroelectric material and rest all notations are same as discussed earlier. Critical thickness (t_C) is that thickness above which, voltage amplification cannot be achieved without hysteresis. So thickness of ferroelectric material should be lower than critical thickness, for obtaining voltage amplification without hysteresis. Fig. 5*b* shows differential voltage amplification dV_D/dV_S with respect to V_S in FE–DE heterostructure.

5. Conclusion: Unstable nature of negative capacitance in ferroelectric capacitor has been studied for different value of ferroelectric oxide thickness. This unstable nature can be stabilised by adding a dielectric material in series with ferroelectric capacitor. Negative capacitance in ferroelectric oxide makes the overall capacitance of heterostructure greater than dielectric capacitance (which gives a clear picture of capacitance enhancement in heterostructure) and thus smaller change in supply voltage leads to larger change in voltage drop across dielectric capacitor which justifies the voltage amplification in heterostructure. Higher voltage amplification can be achieved for larger thickness of ferroelectric oxide but ferroelectric thickness should be less than critical thickness so as to obtain voltage amplification without hysteresis.

6 References

[1] Yuan T., Ning T.H.: 'Fundamentals of modern VLSI Devices' (Cambridge University Press, Cambridge, U.K., 1998)
[2] Theis T.N., Solomon P.M.: 'It's time to reinvent the transistor!', *Science*, 2010, **327**, (5973), pp. 1600–1601
[3] Kobayashi M., Hiramoto T.: 'On device design for steep-slope negative-capacitance field-effect-transistor operating at sub-0.2 V supply voltage with ferroelectric HfO_2 thin film', *AIP Adv.*, 2016, **6**, (2), p. 25113
[4] Theis T.N., Solomon P.M.: 'In quest of the 'next switch': prospects for greatly reduced power dissipation in a successor to the silicon field-effect transistor', *Proc. IEEE*, 2010, **98**, (12), pp. 2005–2014
[5] Zhirnov V.V., Cavin R.K.: 'Nanoelectronics: negative capacitance to the rescue?', *Nature Nanotechnol.*, 2008, **3**, (2), pp. 77–78
[6] Khan A.I., Chatterjee K., Wang B., *ET AL.*: 'Negative capacitance in a ferroelectric capacitor', *Nature Mater.*, 2014, **14**, (2), pp. 182–186
[7] Catalan G., Jiménez D., Gruverman A.: 'Ferroelectrics: negative capacitance detected', *Nature Mater.*, 2015, **14**, (2), pp. 137–139
[8] Khan A.I., Bhowmik D., Yu P., *ET AL.*: 'Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures', *Appl. Phys. Lett.*, 2011, **99**, (11), p. 113501
[9] Appleby D.J.R., Ponon N.K., Kwa K.S.K., *ET AL.*: 'Experimental observation of negative capacitance in ferroelectrics at room temperature', *Nano Lett.*, 2014, **14**, (7), pp. 3864–3868
[10] Lin C.-I., Khan A.I., Salahuddin S., *ET AL.*: 'Effects of the variation of ferroelectric properties on negative capacitance FET characteristics', *IEEE Trans. Electron Devices*, 2016, **63**, (5), pp. 2197–2199
[11] Jain A., Alam M.A.: 'Stability constraints define the minimum subthreshold swing of a negative capacitance field-effect transistor', *IEEE Trans. Electron Devices*, 2014, **61**, (7), pp. 2235–2242
[12] Jain A., Alam M.A.: 'Proposal of a hysteresis-free zero subthreshold swing field-effect transistor', *IEEE Trans. Electron Devices*, 2014, **61**, (10), pp. 3546–3552
[13] Jain A., Alam M.A.: 'Prospects of hysteresis-free abrupt switching (0 mV/decade) in Landau switches', *IEEE Trans. Electron Devices*, 2013, **60**, (12), pp. 4269–4276
[14] Sharma A., Roy K.: 'Design space exploration of hysteresis-free $HfZrO_x$-based negative capacitance FETs', *IEEE Electron Device Lett.*, 2017, **38**, (8), pp. 1165–1167
[15] Salahuddin S., Datta S.: 'Use of negative capacitance to provide voltage amplification for low power nanoscale devices, *'Nano Lett.*, 2008, **8**, (2), pp. 405–410
[16] Salahuddin S., Datta S.: 'Can the subthreshold swing in a classical FET be lowered below 60 mV/decade?. Proc. IEEE Int. Electron Devices Meeting (IEDM), San Francisco, CA, 2008, pp. 1–4, doi: 10.1109/IEDM.2008.4796789
[17] Khan A.I., Salahuddin S.: 'Extending CMOS with negative capacitance', in King Liu T. & Kuhn K. (Eds.): CMOS and beyond: logic switches for terascale integrated circuits' (Cambridge University Press, Cambridge, MA, USA, 2015), pp. 56–76, doi: 10.1017/CBO9781107337886.006
[18] Yeung C.W., Khan A.I., Sarker A., *ET AL.*: 'Low power negative capacitance FETs for future quantum-well body technology'. IEEE 2013 Int. Symp. on VLSI Technology, Systems and Application (VLSI-TSA 2013), Hsinchu, Taiwan, 2013, pp. 1–2, doi: 10.1109/VLSI-TSA.2013.6545648
[19] Khan A.I., Yeung C.W., Hu C., *ET AL.*: 'Ferroelectric negative capacitance MOSFET: capacitance tuning & antiferroelectric operation'. IEEE 2011 Int. Electron Devices Meeting, Washington, DC, 2011, pp. 11.3.1–11.3.4, doi: 10.1109/IEDM.2011.6131532
[20] Khan A.I., Radhakrishna U., Chatterjee K., *ET AL.*: 'Negative capacitance behavior in a leaky ferroelectric', *IEEE Trans. Electron Devices*, 2016, **63**, (11), pp. 4416–4422

doi: 10.1049/mnl.2018.5172

[21] Kim Y.J., Park M.H., Lee Y.H., *ET AL.*: 'Frustration of negative capacitance in $Al_2O_3/BaTiO_3$ bilayer structure', *Sci. Rep.*, 2016, **6**, (1), p. 19039
[22] Khan A.I., Radhakrishna U., Salahuddin S., *ET AL.*: 'Work function engineering for performance improvement in leaky negative capacitance FETs', *IEEE Electron Device Lett.*, 2017, **38**, (9), pp. 1335–1338
[23] Li J., Nagaraj B., Liang H., *ET AL.*: 'Ultrafast polarization switching in thin-film ferroelectrics', *Appl. Phys. Lett.*, 2004, **84**, (7), pp. 1174–1176
[24] Saeidi A., Jazaeri F., Stolichnov I., *ET AL.*: 'Double-gate negative-capacitance MOSFET with PZT gate-stack on ultra thin body SOI: an experimentally calibrated simulation study of device performance', *IEEE Trans. Electron Devices*, 2016, **63**, (12), pp. 4678–4684