Hetero-material CPTFET with high-frequency and linearity analysis for ultra-low power applications

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In this work, the authors have focused on increasing the current driving capability, speed of operation, suppression of parasitic capacitance and ambipolarity of the charge plasma tunnel field effect transistor (CPTFET). Gate dielectric and hetero-material engineering are employed in the CPTFET to obtain better drain current. Introduction of high-k dielectric increases the injection of charge carriers in the intrinsic body while a low-energy bandgap III–V material reduces the tunnelling width leading to the increased rate of band-to-band tunnelling of electrons and thus, enhancing the ON-state current of the device. Hence, the proposed device shows superior performance when operated in regime of DC and high frequency. For reducing the ambipolar conduction in the device, a widely used concept of underlapping of gate electrode is employed which reduces the leakage current in the device. Further, to determine the reliability of the device at high frequency, an analysis of linearity parameters is carried out. The proposed device is highly reliable to function at high-frequency regime. Therefore, the overall introduction of gate dielectric engineering, hetero-material engineering and underlapping of gate electrode improves the performance and characteristics of CPTFET.

1. Introduction: In the present era of nano-scale electronic devices, the central idea of semiconductor industries is to focus on developing high-performance device at the affordable price with increased density of transistor in integrated circuits. Metal–oxide–semiconductor field effect transistors (MOSFETs) are considered over conventional bipolar transistor because of its reduced size and better driving current which leads to increased speed of operation. Further, downscaling of traditional MOSFET guided to the matter of short channel effects [1, 2]. These effects include variation in the threshold voltage (V_{th}) of the device, drain induced barrier lowering, velocity saturation and increased leakage current [1, 2]. Tunnel field effect transistor (TFET) is a device introduced over past few decades and has shown great advantages over traditional MOSFETs because of its unique working mechanism based on the phenomenon of band-to-band tunnelling (BTBT) within energy bands. Subthreshold slope (SS_{MOSFET}) of MOSFET is restricted to the value of 60 mV/decade as illustrated in (1), whereas TFET provided steeper on–off switching characteristic due to its capability of achieving subthreshold slope (SS_{TFET}) <60 mV/decade as described by (2), which makes it a potential contender to work in subthreshold region [3–5]. TFET has an architecture of $N^+ - I - P^+$ and hence, while fabricating N^+ and P^+ region rigorous amount of workforce is required to develop high doping concentration and sharp junction leading to increased cost of the fabrication process. New methods are been implemented to increase the performance of the device ensuring the fabrication compatibility

$$SS_{MOSFET} = \frac{\partial V_{gs}}{\partial I_{ds}} = \left(1 + \frac{C_d}{C_{ox}}\right)\frac{kT}{q}\ln 10 \simeq \frac{kT}{q}\ln 10 = 60\,\text{mV/decade}|(T = 300\,\text{K}) \quad (1)$$

$$SS_{TFET} = \frac{V_{gs} - V_{OFF}}{\ln(I_{TH}/I_{OFF})} \quad (2)$$

Charge plasma TFET (CPTFET) is one of the devices which helps in overcoming the fabrication problem of ultra-sharp doping profile and abrupt junction. This is done by implementing TFET by the formation of nano-scale region using deposition of metal work function rather than performing physical doping. This reduces both the cost and complexity of the fabrication process. Drain and source regions in CPTFET are developed by the potential applied to the two metal electrodes of appropriate work functions. However, it also suffers from low ON-state current as of its doped counterpart which leads to inferior performance at the high frequency. To tackle this issue, a number of methods were discovered: gate dielectric engineering [6], hetero-material engineering [7], gate work function engineering [6], drain work function engineering [7]. In order to overcome the aforementioned issue, a novel combination of hetero-material and gate dielectric engineering are employed in this study. Hetero-gate oxide CPTFET (HGO-CPTFET) induces large amount of charge carriers at the source and channel regions causing an increase in the rate of BTBT. Due to this, there is an intense improvement in the ON-state current of the device [8]. Further, implementation of hetero-material along with hetero-gate oxide leads to our proposed device hetero-gate oxide hetero-material CPTFET (HGO-HM-CPTFET). Hetero-material provides improved drain current as compared to conventional CPFET [9]. The proposed device employs a lower energy bandgap material of gallium antimonide (GaSb) in the source region. This material was analysed due to its recent study of the growth of GaSb on silicon with the help of molecular beam epitaxy (MBE) method [10]. A material GaSb contains a energy bandgap of value $E_g = 0.72$ eV and with the application of gate-to-source voltage, there is an increment in the electric field across source and channel junction. This causes contraction of energy bands at the junction of source and channel region which further provokes shrinking of tunnelling barrier width across the junction. Thus, the probability of tunnelling of electron gets increased ushering the enhancement in the ON-state current.

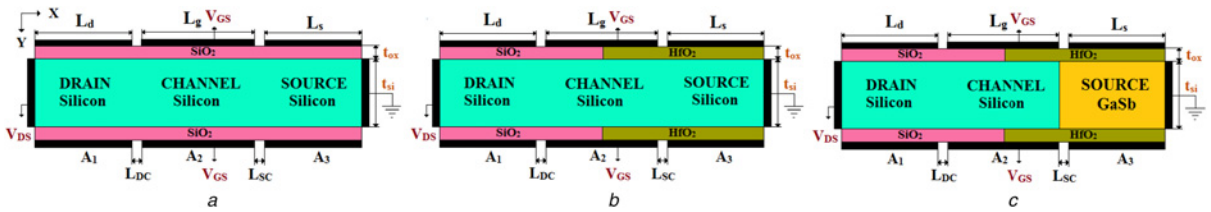

Fig. 1 *2D schematics of*
a CPTFET
b HGO-CPTFET
c HGO-HM-CPTFET

Furthermore, to reduce the ambipolar conduction in the device, the concept of underlapping on the gate electrode is acquired in which the length of gate electrode is reduced from the drain towards source end.

In the following manuscript, we have carried out a comprehensive analysis and study of conventional CPTFET and the proposed device concerning their DC response along with their high-frequency characteristics such as transfer characteristics ($I_{ds} - V_{gs}$), Gate-to-drain capacitance (C_{gd}), transconductance (g_m), gain-bandwidth product (GBP) and cut-off frequency (f_T). This Letter is divided into sections as follows. Section 1 gives the descriptions of the structure and simulation models of the devices. Section 2 represents the relative study of the performance of conventional CPTFET, HGO-CPTFET and HGO-HM-CPTFET. Section 3 illustrates the high-frequency analysis of the device. Section 4 represents the study of effect of spacing between gate and drain electrodes in the proposed HGO-HM-CPTFET. Section 5 describes the linearity analysis and corresponding performance of the above-mentioned device. At last, the conclusions from the study of these devices are enlightened in Section 6.

1.1. Device architecture: In this section, we have described the dimensions of the simulated device. The two-dimensional (2D) schematic views of CPTFET, HGO-CPTFET and HGO-HM-CPTFET are illustrated in Figs. 1*a–c*, respectively. The conventional CPTFET is made up of all silicon-based material while in HGO-CPTFET an additional gate oxide of hafnium oxide – HfO_2 ($k = 29$) is applied across the source–channel region extending throughout half the span of the above-mentioned device. The thickness of oxide is maintained at 1 nm finalised from previous studies [11]. HGO-HM-CPTFET introduces a low bandgap material of gallium antimonide (GaSb) at the source region as an alternative to silicon (Si) while the rest of the region employs silicon (Si).

In this Letter, all devices have an intrinsic body of concentration $n_i = 1 \times 10^{15}\,\text{cm}^{-3}$. Highly doped N^+-type drain and P^+-type source region are obtained by charge induction through the metal electrode having dissimilar work function. Hence, for an emergence of drain region with N^+-type doping, a metal hafnium ($\phi_{A_1} = 3.9\,\text{eV}$) having low work function is taken into consideration which helps in inducing electron in the intrinsic body and hence, it is named as drain electrode. While, platinum ($\phi_{A_3} = 5.93\,\text{eV}$) is a high work function metal used for formation of P^+ source region which helps to induce holes in the intrinsic body, thus, it is named as source electrode. A spacer of 2 and 5 nm is provided between source–gate and drain-gate electrode, respectively. This space accounts for the variations in charge carriers near the junction and is responsible for tunnelling probability across the junction. Table 1 depicts all the parameters considered for the study.

1.2. Realisation of the proposed device: For the realisation of HGO-HM-CPTFET, following steps have been performed. A silicon (Si) wafer of intrinsic concentration of $1 \times 10^{15}\,\text{cm}^{-3}$ is considered as the substrate. The selective growth of hetero-material is then done on the Si substrate. For this, initially a oxide layer is grown on substrate followed by photolithography and reactive ion etching. Thereafter, GaSb can be grown on Si trench with the help of solid-source MBE [12–15]. A hetero-gate oxide consisting of SiO_2 and HfO_2 is then grown on the substrate with the help of dry oxidation and low-pressure chemical vapour deposition [16]. This type of growth of hetero-gate oxide has been reported in [16]. Basically, a photo-lithography is performed on the wafer by implementing a mask on the drain region. This is done to protect the drain region during the etching process. Hydroflouric vapour is used to selectively etch the SiO_2 gate oxide at the source side, and then, a thin layer of 1 nm HfO_2 is grown at the etched area by the atomic layer deposition process. In order to remove the remaining HfO_2 grown on the regions of gate, source and drain, an anisotropic dry etching of HfO_2 needs to be carried out [16].

Table 1 Device parameters

Parameters	Values
channel length (L_{si})	50 nm
body thickness (t_b)	10 nm
oxide thickness (t_{ox})	1 nm
gate source spacing (L_{SC})	2 nm
drain electrode work function (ϕ_{A1})	3.9 eV
gate electrode work function (ϕ_{A2})	4.3 eV
source electrode work function (ϕ_{A3})	5.93 eV
gate drain spacing (L_{DC})	5 nm

1.3. Simulation models: The simulation study is performed on a simulator named as 2D-ATLAS, Silvaco TCAD (version 5.19.20. R) [17]. Various models have been employed in the simulation of the device. Since TFETs are based on the quantum phenomenon of tunnelling, BTBT and bandgap narrowing models are taken into account for narrowing of the bandgap. The ON-state analysis of TFET extensively utilise BTBT model. For the numerical solution, Wentzel–Kramer–Brillouin method is employed. The model of non-local BTBT is taken into account for simulations to incorporate the physical effect of phenomenon termed as quantum tunnelling across channel/source and channel/drain junction. Other simulation models such as Shockley–Read–Hall recombination model, concentration-dependent mobility, Fermi-Dirac statistics and field-dependent mobility are all incorporated in the simulation. In order to consider the mismatch in the lattice, Kronig–Penney band model is utilised [17].

2. DC analysis of device: In this section, we have analysed several working states of the device with the assistance of energy band diagram and carrier concentration. A noticeable variation in DC and high-frequency attributes of above-mentioned device is observed due to employment of hetero-material at source region and hetero-gate oxide in the oxide layer. These variations can be observed in Figs. 2*a–d* and 3*a–d*.

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2.1. Energy band diagram: In OFF-state condition $V_{gs} = 0$ V, it is clearly noticed that the charge carriers cannot tunnel across the junction from valence band to conduction band of source to channel region depicted in Fig. 2*a*. This happens due to the broadening of bandgap at channel/source junction leading to the widening of tunnelling width. On the analysis of ON-state condition of the device $V_{gs} > 0$ V represented in Fig. 2*b*, it is noticed that because of hetero-material and gate-dielectric engineering, there is aggressive shrinkage in width of tunnelling barrier at the interface of source and channel region. Tunnelling probability of the charge carriers is increased due to narrowing of barrier width allowing a huge number of charge carriers to flow across the junction. When positive gate voltage is applied, charge carriers get the acceptable energy to tunnel through the bands which develop ON-state current in the device. Fig. 2*b* shows HGO-HM-CPTFET has shortest barrier width than others while bandgap at drain region is quite significant which makes it difficult for charge carriers to tunnel through the junction.

Thermal equilibrium state $V_{gs} = V_{ds} = 0$ V is depicted in Fig. 2*c*. From the figure, it is observed that there is no tunnelling of charge carriers as tunnelling width is not narrow enough to pass charge carriers through the junction. Also, there is no motion of charge carriers as no potential is applied at drain and source electrodes of the device. In the ambipolar state, the gate is biased with a negative potential of $V_{gs} = -0.5$ V. It is depicted from Fig. 2*d* that width of tunnelling is getting narrower at drain–channel junction. Hence, a leakage current is produced due to tunnelling at drain–channel region.

2.2. Carrier concentration: In all these states, the majority charge carriers concentration is maintained at a constant level with the help of source electrode and concentration of minority charge carriers exhibits different behaviour across the device. On the other hand, at the drain region, drain electrode helps to maintain the concentration of majority charge carriers and shows different behaviour for minority carrier concentration. In the channel region, there is an increment in the carrier concentration because of tunnelling phenomenon between energy bands. The carrier concentration of OFF-state is presented in Fig. 3*a*. Due to narrow bandgap at drain–channel interface (Fig. 2*a*), the concentration of holes increases in the channel region due to tunnelling at drain–channel interface. At the same junction, an accumulation of charge carriers can be illustrated from Fig. 3*a*.

Under ON-state condition, the electron concentration in the channel enhances as observed from Fig. 3*b*. This is because of narrowing of width of tunnelling barrier across the interface due to source and channel regions and hence, charge carriers get accumulated leading to ON-state current. In the thermal equilibrium, the concentration of electrons and holes shows symmetrical behaviour in the channel region as illustrated in Fig. 3*c*. This happened because as device is debarred from any kind of biasing and thus, there is no movement in the energy band (Fig. 2*c*) leading to no existent of accumulated charge carriers. Under ambipolar state, tunnelling width at drain–channel junction reduces (Fig. 2*d*) leading to tunnelling of holes which increases its concentration in channel as illustrated in Fig. 3*d*.

3. High-frequency analysis: This section evaluates the comparative study of afore-mentioned devices under high-frequency [radio frequency (RF)] conditions. All devices are evaluated in the ON-state and it is clearly observed from Fig. 4 that there is an enhancement in the ON-state current due to gate-dielectric and hetero-material engineering. In this device, a low bandgap material GaSb helps in shrinking of width for tunnelling across the junction of source and channel (Fig. 2*b*). This reduction allows stress-free motion of charge carriers from valence band to conduction band of source-to-channel region. At ($V_{gs} < V_{th}$), there is reduction of tunnelling path across channel and drain junction (Fig. 2*d*). Hence, holes gets tunnel through conduction band to valence band leading to increase in the OFF current in the device. In HGO-HM-CPTFET, this tunnelling width is maintained at large value so that there is less tunnelling of holes. Hence, the tunnelling

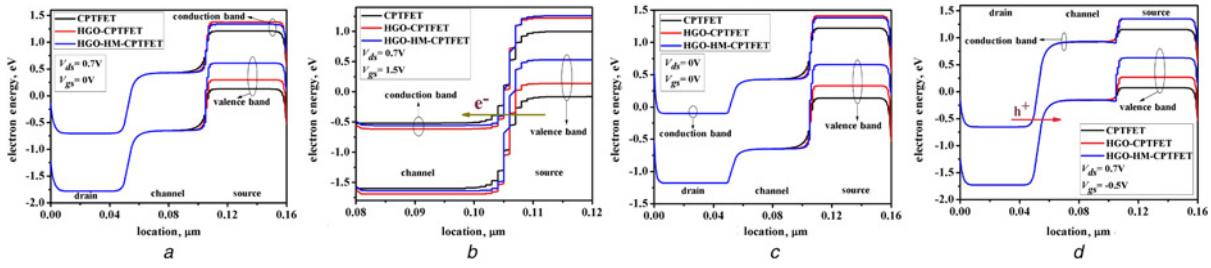

Fig. 2 *Energy band diagram of CPTFET, HGO-CPTFET and HGO-HM-CPTFET under states of*
a OFF
b ON
c Thermal equilibrium
d Ambipolar

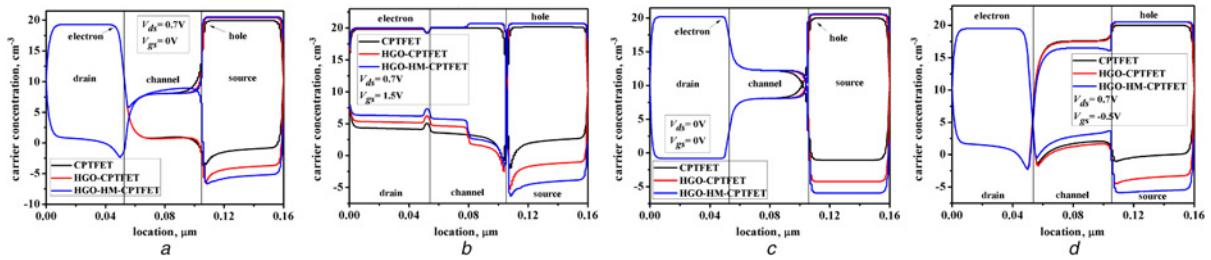

Fig. 3 *Carrier concentration of CPTFET, HGO-CPTFET and HGO-HM-CPTFET under states of*
a OFF
b ON
c Thermal equilibrium
d Ambipolar

of electrons across channel and source region leads to the development of ON-state current. The variations in current are also due to the presence of spacer width between the metal electrodes which determine the rate of tunnelling. There is an increment in the value of ON-state current due to the deterioration of spacer width between source and gate electrodes. On the other hand, OFF current declines with increase in spacer width between drain and gate electrodes.

When positive voltage is applied on the gate electrode $V_{gs} = 1.5\,V$ and drain electrode $V_{ds} = 0.7\,V$, the parameters obtained are listed in Table 2. The threshold voltage (V_{th}) of the device can be enumerated by the concept of constant current in which a constant current of $I_{ds} = 10^{-7}\,A/\mu m$ is maintained for analysis. The HGO-HM-CPTFET has a subthreshold slope (SS) of 39.5 mV/decade and it shows lower subthreshold slope in comparison with conventional Si-based CPTFET.

Gate-to-drain capacitance (C_{gd}), gate-to-source capacitance (C_{gs}) and their summation gate-to-gate capacitance (C_{gg}) are the parasitic capacitances present in the device. Of all these capacitance, C_{gd} also known as Miller capacitance is well thought-out to be superior among all the other capacitances [18]. Presence of parasitic capacitance plays an important role in high-frequency applications, as these capacitances affect the performance of the device drastically. Therefore, it is necessary to analyse these parasitic capacitances for these devices with their application in high-frequency circuits. Even if these capacitance cannot be removed, its value should be kept low to make the device feasible for RF applications. The expression for C_{gd} is

$$C_{gd} = \frac{\partial Q_g}{\partial V_{ds}} \tag{3}$$

where Q_g is termed as gate charge and V_{ds} is drain voltage.

Graphical analysis of gate-to-drain capacitance (C_{gd}) with reference to gate-to-source voltage (V_{gs}) is depicted in Fig. 5*a*. Lower value of C_{gd} is obtained in case of conventional CPTFET in comparison to other. This is due to the introduction of bandgap and dielectric engineering in other device (Figs. 1*b–c*). As material of device is changed, its electrical properties also get changed. Therefore, a comparison is made between HGO-CPTFET and HGO-HM-CPTFET. From Fig. 5*a* the value of C_{gd} for HGO-HM-CPTFET is less as compared to HGO-CPTFET due to declination in density of states. Also, the potency of capacitive coupling is reduced at the gate–drain junction, making this device suitable for high-frequency regime. On increasing the value of V_{gs}, the genesis of inversion layer increases across the channel and thus, barrier between drain and channel starts to reduce. Thus, an increment in the value of C_{gd} is observed with increment of V_{gs}. There is an early rise in the value of C_{gd} in HGO-HM-CPTFET as compared to other CPTFET and this shows its capability of switching at high speed.

Fig. 5*b* demonstrates the behaviour of transconductance (g_m) with reference to gate-to-source voltage (V_{gs}) of all above-mentioned devices. Change in output ON-state current to change in input gate voltage defines the transconductance

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{4}$$

where I_{ds} is drain current and V_{gs} is gate-to-source voltage.

From Fig. 4, it is clearly noticeable that the value of ON-state current in HGO-HM-CPTFET is greater than conventional CPTFET and HGO-CPTFET. This is because of employment of GaSb having a lower energy bandgap at source–channel junction by which the shortening of tunnelling width takes place at hetero-material. Also, introduction of hetero-gate oxide HfO_2 amplifies the ON-state current by inducing large number of charge carriers compared to conventional gate oxide of SiO_2. The combined effect of hetero-material and hetero-gate oxide helps to increase drain current, thereby improving the transconductance of the device. Better sensitivity is obtained due to increment in the current and hence, in small voltage considerably large current is obtained. The switching speed of device gets increased along with high efficiency.

GBP and cut-off frequency (f_T) are the two crucial features in the investigation of high-frequency response. When current gain of the circuit attains the value of unity, cut-off frequency is obtained at that

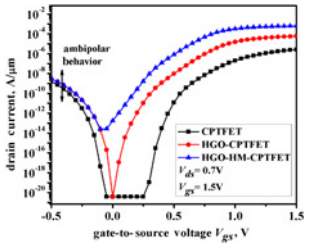

Fig. 4 $I_{ds} - V_{gs}$ *of*
a CPTFET
b HGO-CPTFET
c HGO-HM-CPTFET

Table 2 Comparison of transfer characteristics

Device	I_{ds}, A/μm	V_{th}, V
CPTFET	2.6×10^{-6}	0.93
HGO-CPTFET	5.9×10^{-5}	0.61
HGO-HM-CPTFET	0.63×10^{-4}	0.38

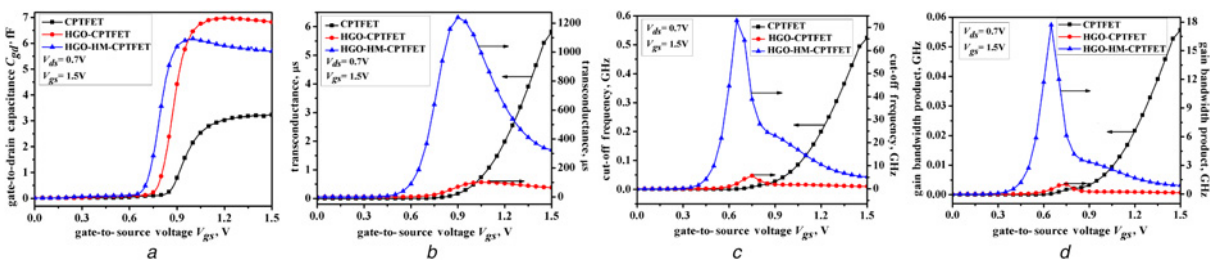

Fig. 5 *Performance analysis*
a C_{gd}
b g_m
c f_T
d GBP of CPTFET, HGO-CPTFET and HGO-HM-CPTFET

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particular frequency. The expression for f_T is

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \simeq \frac{g_m}{2\pi(C_{gg})} \quad (5)$$

The perusal of cut-off frequency (f_T) with regards to gate-to-source voltage (V_{gs}) is illustrated in Fig. 5*c*. The cut-off frequency of HGO-HM CPTFET is comparatively much higher than conventional CPTFET and HGO-CPTFET. This increment is caused due to the incorporation of low bandgap material of GaSb at the source region which enhances the ON-state current. Thus, there is an increment in g_m and decrement in the C_{gd}. Hence, it improves the cut-off frequency of the device and from Fig. 5*c*, it is noticed that at lower gate voltage, the value of f_T increases because of improvement in g_m. Then it attains its maximum peak value and starts to degrade because of the combined effect of reducing g_m and increment in C_{gd}.

At a constant value of 10, the parameter obtained from the multiplication of bandwidth with gain of the device is described as GBP. The behaviour of GBP is similar to that of cut-off frequency as shown in Fig. 5*d*. As a result, a similar kind of observation is obtained as in the case of f_T. Therefore, higher the drain voltage greater is the performance of the device. The expression for GBP is

$$\text{GBP} = \frac{g_m}{20\pi C_{gd}} \quad (6)$$

4. Optimisation of space between gate and drain electrodes (UL): This section explains the concept of under-lapping of gate electrode at the drain–channel region. The energy band diagram of HGO-HM-CPTFET with optimisation of underlap is represented in Fig. 6*a*. The device is simulated under the ON-state condition. From the given figure, it is illustrated that with variation of underlap length of gate electrode at drain–channel region has no affect on the energy band diagram across source–channel region. Therefore, a minor variation is only observed in the ON-state current as depicted in Fig. 6*b*. Underlap of gate electrode affects the energy band position at the interface of drain and channel region leading to variation in the ambipolar conduction of the device.

From Fig. 6*b*, it is noticed that underlapping of gate electrode reduces the ambipolar conduction in the proposed device. The ON-state conduction is not affected by underlap of gate electrode. As gate length decreases from the drain end, the field across drain–channel interface starts to reduce leading to increase in the tunnelling width which makes it difficult for holes to tunnel through drain–channel junction to reach the channel region. This reduces the leakage current in the device and makes the proposed device more reliable for applications. UL = 10 nm shows great potential because of suppressed leakage current without affecting the ON-state current. For UL > 15 nm, ON-state current in the HGO-HM-CPTFET shows decrement in its value. This is due to shortening of gate electrode which results in loss of its

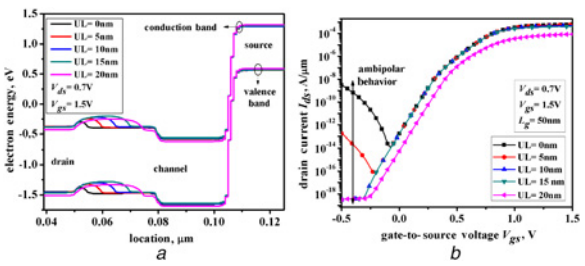

Fig. 6 *Effect of different UL on*
a Energy band diagram
b I_{ds}–V_{gs} of HGO-HM-CPTFET

controllability over the channel region, hence affecting the DC as well as high-frequency characteristics of the HGO-HM-CPTFET. From Table 3, it is observed that increase in underlap length reduces the C_{gd} of the device because of shrinking of inversion layer on the drain end of the device. This enhances the switching capability for digital applications without having any influence on the ON-state current. As there is minimal variations in ON-state current, g_m of the device also shows minor variations with the increment in the underlap length. Therefore, the f_T of the device enhances with increased underlap length because of rapidly decreasing C_{gd} and steadily decreasing g_m. GBP of the device also shows similar behaviour as that of f_T.

5. Linearity analysis: An assertion is required to obtain minimised distortion of the signal in the present-day communication systems. Along with minimised distortion, the high speed of the device determines its aptness while operating in DC and analogue/RF regime. To get a system with enhanced linearity performance, transconductance (g_m) of the device ought to be persistent over a wide range of input signal. However, non-linear behaviour occurs in MOSFETs and TFETs too, because of variations of g_m over input signal [19]. The linearity distortion responses like VIP2, VIP3, IIP3 and IMD3 are investigated to counter-balance the effect of non-linearity in the device [20]

$$g_{mn} = \frac{1}{n!}\frac{\delta^n I_{ds}}{\delta V_{gs}^n} \quad (7)$$

$$V_{IP2} = 4 \times \left(\frac{g_{m1}}{g_{m2}}\right) \quad (8)$$

$$V_{IP3} = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m3}}\right)} \quad (9)$$

$$\text{IIP3} = \frac{2}{3} \times \left(\frac{g_{m1}}{g_{m3} \times R_s}\right) \quad (10)$$

$$\text{IMD3} = \left[\frac{9}{2} \times (\text{VIP3})^2 \times g_{m3}\right]^2 \times R_s \quad (11)$$

where $R_s = 50\,\Omega$ is utilised majorally in RF applications. The extrapolating input gate voltage is constituted as VIP2 in which a similar first-order harmonic voltage including second-order harmonic voltage is obtained. Identical harmonic voltages of first- and third-order are obtained by the extrapolating input voltage denoted by VIP3. Similarly, the extrapolated input power designated by IIP3 has first- and third-order harmonic powers to be identical. The third-order intermodulation distortion is described by the IMD3 which has the power of intermodulation components of fundamental and third-order are equivalent to one another [21]. In order to have a device with lower distortion, the parameters of VIP2, VIP3 and IIP3 need to be high so as to increase the linearity performance while IMD3 needs to be lowered [20].

Fig. 7*a* denotes the comparison of VIP2 with implemented gate-to-source voltage for CPTFET, HGO-CPTFET and

Table 3 High-frequency analysis

Parameters	Space between gate-drain electrode (UL)				
	0 nm	5 nm	10 nm	15 nm	20 nm
C_{gd}, fF/μm	5.7	5.08	4.25	3.42	6.51
g_m, μs	1260	1220	1140	1050	152
f_T, GHz/μm	72	84.8	95.5	105	22.9
GBP, GHz/μm	16.5	21.9	26.9	31.8	7.42

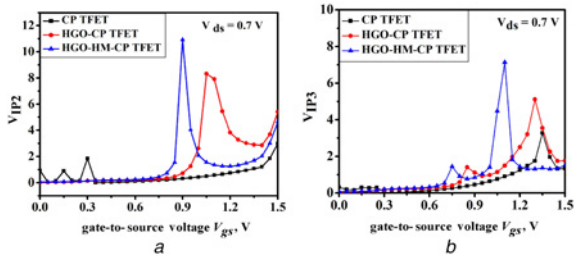

Fig. 7 *Variations of*
a VIP2
b VIP3 as a function of gate-to-source voltage V_{gs} for CPTFET, HGO-CPTFET and HGO-HM-CPTFET

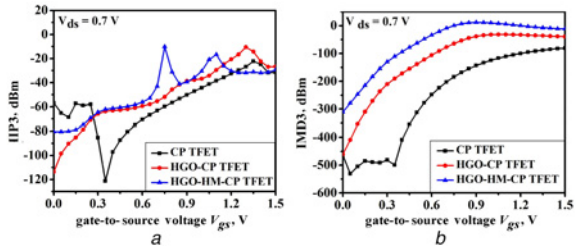

Fig. 8 *Variations of*
a IIP3
b IMD3 as a function of gate-to-source voltage V_{gs} for CPTFET, HGO-CPTFET and HGO-HM-CPTFET

HGO-HM-CPTFET. VIP2 is an imperative linearity metrics which resolves the distortion features in the several DC parameters. A large value of VIP2 is preferred for acquiring high linearity and lower distortion performance in the above-mentioned device. It is evident from Fig. 7*a* that HGO-HM-CPTFET signifies a inflated value of VIP2 in contrast to other devices. This happened because of the incorporation of lower energy bandgap material of GaSb at the source. Fig. 7*b* illustrates the comparative analysis of VIP3 with regards to applied gate-to-source voltage for devices. It is clear from this figure that a high peak is viewed for HGO-HM-CPTFET as compared to the counterpart of it. Moreover, peak of VIP3 is altered towards lower gate bias which affirms that it is accomplished to attain better linearity.

The variation of IIP3 with input gate voltage for proposed devices is demonstrated in Fig. 8*a*. It clearly reflects a peak is observed in IIP3 for HGO-HM-CPTFET as compared to the latter devices and also the peak is shifted towards lower gate bias which replicates in better linearity and lower distortion. Fig. 8*b* depicts the change in IMD3 with change in applied gate-to-source voltage. The origination of IMD3 is caused by the non-linearity in the device. This non-linearity is revealed by the static characteristics of transistor which leads to profligacy of signal in wireless system [19]. Therefore, it is significant to emphasise that the IIP3 power in Fig. 8*a* presented by HGO-HM-CPTFET is greater than IMD3 depicted in Fig. 8*b*, which ensures immunity against hot-carrier effect, and provides improved power, thereby enabling a reduction in intermodulation distortion.

6. Conclusion: From above analysis, it is noticed that the increase in the ON-state current of the HGO-HM-CPTFET is due to the contribution of both the lower energy bandgap material of GaSb at the source region and high-k dielectric of HfO_2. The proposed device shows better performance at high-frequency regime than conventional Si-based device. The reduction of ambipolarity of the device is carried out by optimising the spacing between gate–drain electrode and it is found that for UL = 10 nm, the HGO-HM-CPTFET gives superior results for low-power devices. The study of linearity performance of the HGO-HM-CPTFET shows its competency towards varying working conditions. Therefore, the proposed device shows great potential to be utilised in ultra-low power applications for its better DC and RF performance.

7. References

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