Impact of gate material engineering on ED-TFET for improving DC/analogue-RF/linearity performances

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To avoid the fabrication complexity and cost of nanoscale devices, a dual metal gate (DMG) in polarity controlled electrically doped tunnel field-effect transistor (ED-TFET) has been introduced first time for DC, analogue/radio frequency (RF) and linearity performance improvement. The formation of n+ drain and p+ source regions are done by applying polarity biases of PG-1 as 1.2 V and PG-2 as −1.2 V, respectively, over the silicon body in DMG-ED-TFET. Different analogue/RF and linearity performance metrics of DMG-ED-TFET are evaluated using ATLAS device simulator and compared with that of ED-TFET. The figure of merits (FOMs) studied in this work for DMG-ED-TFET are in terms of transconductance, gate-to-drain capacitance, gain bandwidth product, cut-off frequency and linearity parameters such as third-order transconductance coefficient (g_{m3}), VIP3, IIP3 and IMD3. From the simulations, it is found that DMG-ED-TFET achieves significant improvement in these FOMs as compared to ED-TFET due to introduction of dual metal at gate electrode (gate workfunction engineering). The work has also optimised the proposed device to attain optimum analogue/RF and linearity performance.

1. Introduction: According to the past reports [1, 2], the metal–oxide–semiconductor field-effect transistor is facing many issues due to downscaling of short channel effects which are the reasons for threshold, drain induced barrier lowering, off-state current and high leakage current. At present, these problems are solved by the new device named as tunnel field effect transistor (TFET). TFET works on the basis of band-to-band tunnelling mechanism and it has more benefits like low leakage current, low switching energy and also its subthreshold slope (SS) is below the 60 mV/dec [3]. TFET also suffer from fabrication process, i.e. random doping fluctuations with high leakage current and thermal budget [4–6]. These issues are resolved by charge plasma (CP)-TFET [7–9]. CP-TFET works on the workfunction engineering; it improves the DC performances of the device along with analogue/radio frequency (RF) figure of merits (FOMs) up to some extent. These are improved by using gate dielectric engineering, hetero-materials [10, 11] but still they are limited due to presence of tunnelling width of CP-TFET is larger at source–channel junction which will produce low-ON current.

To overcome the aforementioned issues, a new concept of electrically doped TFET (ED-TFET) [12–14] has been introduced. In this device, drain and source regions are developed by applying external voltages over polarity gates (PGs) on intrinsic substrate [15], this phenomenon is advantageous to create better abruptness at S/C interface, which consequently results in improvement in DC performances as compared to CP-TFET. However, the ED-TFET also faces the problem of poor RF performance, harmonic distortion as well as linearity related issues for low-noise RFIC designs in advanced wireless communication, same as doped-TFET and CP-TEFT. So, to resolve this problem, a novel structure of dual metal gate electrically doped TFET (DMG-ED-TFET) has been proposed. This structure improves the RF performance and analyses the device suitability in the presence of strong interference by maintaining the linear operation even while receiving weak signals. Furthermore, in this work, we have made a comparative analysis of the DC characteristics and analogue/RF FOMs gate-to-drain capacitance (C_{gd}), cut-off frequency (f_T), transconductance (g_m), gain bandwidth product (GBP), and also linearity FOMs third-order transconductance coefficient (g_{m3}), third-order voltage intercept point (VIP3), third-order input intercept point (IIP3) and third-order intermodulation (IMD3) behaviours between the conventional ED-TFET and proposed DMG-ED-TFET has been given.

Rest of the paper is arranged as follows. Section 2 describes device geometry, dimensions used for simulations and technology aided computer design models. Section 3 presents results and discussion which deals with the device characteristics, analogue/RF analysis and linearity performance. Section 4 represents the optimisation part for the proposed device. Finally, Section 5 is devoted for the discussion of highlights of the paper as conclusion.

2. Device design parameter and simulation setup: Figs. 1*a* and *b* show the device structures of ED-TFET and DMG-ED-TFET, which consist of PG and control gate (CG). External voltage of 1.2 and −1.2 V is applied on PG to create drain and source regions over silicon substrate, respectively. Further, the proposed DMG-ED-TFET contains dual metal CG electrode, i.e. (CG = tunnel gate + auxiliary gate). Nikil silicide (NiSi), a mid-band gap material of 0.45 eV workfunction [15, 16], is used for Schottky contacts. All the device parameters are given in Table 1.

All the simulations have been performed by using silvaco ATLAS 3.20 R [17]. For mathematical computation, non-local band-to-band tunnelling (BTBT) model is essential to estimate tunnelling phenomenon. The non-local BTBT model uses Wentzel-Kramer-Brillouin (WKB) approach for measuring the tunnelling probability using electron–hole wave vector throughout the tunnelling path. Further, Auger recombination, Shockley Read Hall, recombination model, Fermidirac Static model have been incorporated for simulation purpose.

3. Performance analysis

3.1. DC characteristics: In this section, DC characteristics of conventional ED-TFET and the proposed device DMG-ED-TFET have been shown in a comparative manner.

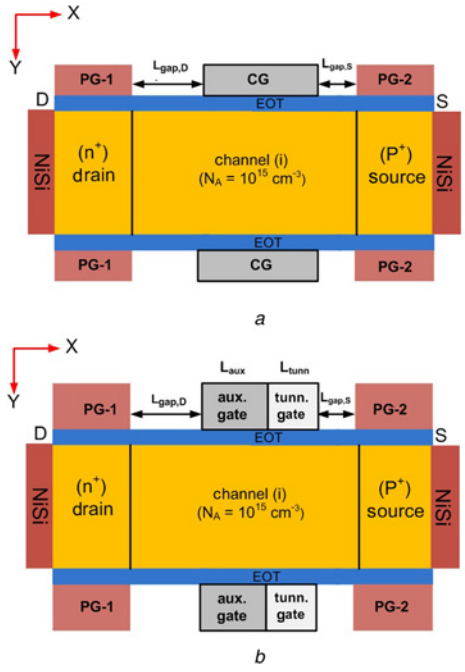

Fig. 1 *Cross-sectional view of*
a Electrically doped tunnel field effect transistor
b Dual metal gate electrically doped tunnel field effect transistor (proposed device)

Table 1 Device design parameters

Parameter name	Symbol	Value	Unit
gate length	L_g	50	nm
gate oxide thickness	T_{ox}	0.8	nm
silicon film thickness	T_{si}	10	nm
channel doping	N_{ch}	1×10^{15}	cm^{-3}
tunnel gate length	L_1	20	nm
auxiliary gate length	L_3	30	nm
drain length	L_d	50	nm
source length	L_s	50	nm
source gap length	$L_{gap,S}$	5	nm
drain gap length	$L_{gap,D}$	20	nm
polarity gate (PG-1) voltage	PG-1	1.2	V
polarity gate (PG-2) voltage	PG-2	−1.2	V
tunnel gate workfunction	ϕ_1	4.2	eV
auxiliary gate workfunction	ϕ_3	4.7	eV

Fig. 2*a* shows the energy band diagram of both devices in OFF-state, the effect of lower workfunction at tunnel gate can be seen by the same figure, which results in more band bending for DMG-ED-TFET rather than ED-TFET due to higher electron concentration in channel at source/channel junction. Further, when V_{gs} is applied, energy bands of channel region goes down and because of lower workfunction of tunnel gate ϕ_{tun}, tunnelling width becomes narrower for DMG-ED-TFET as shown in Fig. 2*b*. It confirms high ON-state current for DMG-ED-TFET as given in Fig. 2*c*. Further from the figure, it is found that drain current behave as exponential function of V_{gs} after the V_{th} and get saturated after a certain value of V_{gs}. Enhanced DC characteristics like better ON-state current, steep SS and low V_{th} for the proposed device (DMG-ED-TFET) can be realised by the same figure. Due to higher tunnelling rate from source to channel in DMG-ED-TFET, consequences of high drain current at the same $V_{gs} = 1.2$ V can be pictured out in Fig. 2*d*. Figure presents drain current versus

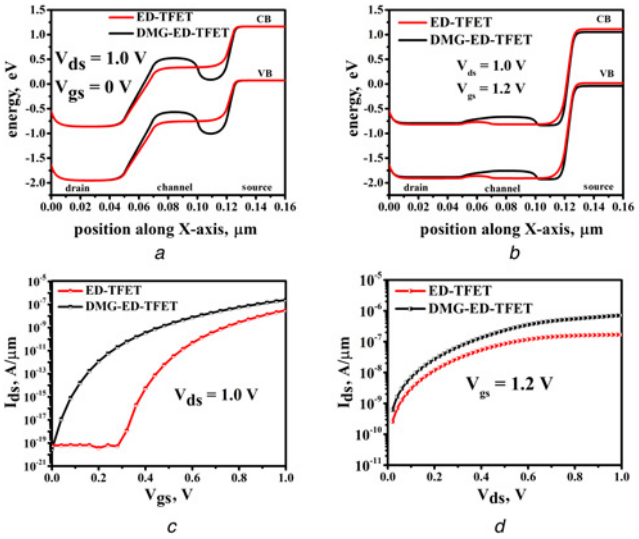

Fig. 2 *Comparison of DC characteristics for ED-TFET and DMG-ED-TFET*
a Energy band along the length of device in OFF-state
b Energy band along the length of device in ON-state
c Transfer characteristics
d $I_{ds} - V_{ds}$ characteristics

V_{ds} curve, where I_D increases with V_{ds} and settle down after 0.8 V for both devices.

3.2. Analogue/RF performances for the proposed device (DMG-ED-TFET): In this section, we have investigated RF performance of the ED-TFET and DMG-ED-TFET. To evaluate the RF performance of devices, transconductance (g_m), gate–drain capacitance (C_{gd}), cut-off frequency (f_T), GBPs is needed. All these parameters are obtained at 1 MHz input port terminal.

In the analysis of all RF parameters, g_m plays a key role in obtaining the higher f_T and GBP. In designing of analogue circuits, g_m decides the gain of the circuit. Transconductance can be calculated by the ratio of change in the drain current to change in V_{gs} at fixed drain bias; it defines the sensitivity of device. Fig. 3*a* shows the

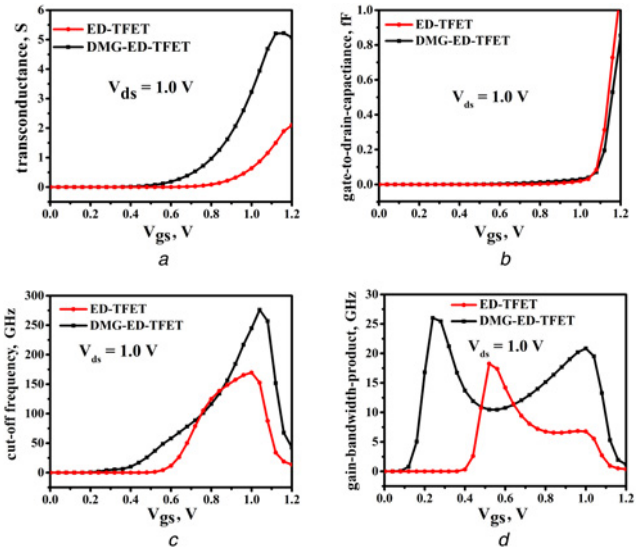

Fig. 3 *Comparative plots of ED-TFET and DMG-ED-TFET*
a Transconductance
b Gate-to-drain capacitance
c Cut-off frequency
d Gain bandwidth product

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variation in g_m with respect to V_{gs} for ED-TFET and DMG-ED-TFET. Initially g_m increases with V_{gs} and after a certain value of V_{gs}, it falls due to mobility degradation. Further, the proposed device (DMG-ED-TFET) shows higher g_m as compared to the conventional device by several orders due to the presence of tunnel gate having workfunction ϕ_{tun}. C_{gd} is a miller capacitance, which decides the switching speed and device behaviour at higher frequencies. Fig. 3*b* gives variation in C_{gd} with respect to V_{gs} for both devices, where DMG-ED-TFET shows a little lower capacitance rather than ED-TFET due to the presence of tunnel gate, which results in trivial change in channel abruptness at drain/channel interface. Apart from these, one of the important FOM for RF analysis is cut-off frequency (f_T). It is analysed when current gain drops to unity [13, 14, 18], and can be written as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{1}$$

From Fig. 3*c*, it is seen that f_T increases initially with V_{gs} because of increasing behaviour of g_m but after a certain value of V_{gs}, C_{gd} also dominates and g_m start falling, which gives combine effect on f_T and it starts falling. Further GBP is given by bandwidth times DC gain [13], which can be calculated by

$$\text{GBP} = \frac{g_m}{20\pi C_{gd}} \tag{2}$$

It follows the same trends and reasons as followed by f_T, shown in Fig. 3*d*.

3.3. Linearity performance of the proposed device: Nowadays, in designing of wireless application systems, complementary metal–oxide–semiconductor technology with low IMD is required for maintaining the linearity performances. Better linearity gives the less number of higher order IMD terms and results in low distortion at output. In this section, to analyse and rectify the nonlinearity problems in terms of VIP3, IMD3, IIP3, g_{m3} [19, 20] for the proposed device DMG-ED-TFET and ED-TFET have been expressed as follows:

$$\text{VIP3} = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m3}}\right)} \tag{3}$$

$$\text{IIP3} = \frac{2}{3} \times \left(\frac{g_{m1}}{g_{m3} \times R_s}\right) \tag{4}$$

$$\text{IMD3} = \left[\frac{9}{2} \times (\text{VIP3})^2 \times (g_{m3})\right]^2 \times R_s \tag{5}$$

where $R_s = 50\ \Omega$ is generally chosen for RF applications. The study of VIP3 is one of the important FOMs which calculate the distortion characteristics from DC parameters. VIP3, IIP3 must be high enough and IMD3 should be low enough for better linearity and distortion performance [20]. VIP3 is extrapolated input voltage point where first and third harmonic voltages are same and IIP3 denotes the equal input power relation between first and third harmonic powers.

The g_{m3} should have lower zero crossover point, which decides the DC operating point to give the best possible performance. Fig. 4*a* shows the change in g_{m3} with respect to V_{gs} for both the devices ED-TFET and DMG-ED-TFET, it confirms lower zero crossover point for DMG-ED-TFET. Fig. 4*b* depicts the variation in VIP3 as a function of gate-to-source voltage. The singularity point or peak point in VIP3 is determined at low gate voltage for DMG-ED-TFET. It means the proposed device DMG-ED-TFET requires lower gate voltage to operate in moderate inversion region and the peak of VIP3 indicates the cancellation of third-order harmonic by device internal feedback around second-order nonlinearity. Fig. 4*c* presents changes in IIP3 with increase in V_{gs}, it

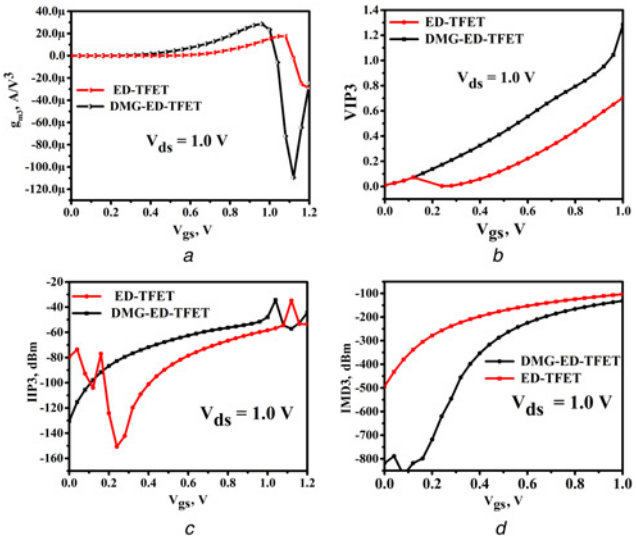

Fig. 4 *Comparative plots of ED-TFET and DMG-ED-TFET*
a g_{m3}
b VIP3
c IIP3
d IMD3

shows kink in IIP3 for DMG-ED-TFET at early V_{gs} as compared to ED-TFET. From the biasing point of view for optimum device performance early kink in IIP3 is needed, which corresponds to zero crossover point of g_{m3}. It means DMG-ED-TFET shows the better linearity response rather than ED-TFET. The IMD3 is one of the important linearity parameter, which comes from nonlinearity executed by $I_D - V_{gs}$ characteristics of the TFET; presence of IMD3 leads distortion in wireless communication systems. So, Fig. 4*d* shows the minimised IMD3 with respect to V_{gs} for the proposed device DMG-ED-TFET as compared to ED-TFET, which is an essential requirement to check the linearity performance.

4. Optimisation: In the optimisation of tunnel gate workfunction (ϕ_{tun}), it is varied from 4.1 to 4.7 eV and the auxiliary gate workfunction (ϕ_{aux}) is kept constant at 4.7 eV. Figs. 5*a* and *b*

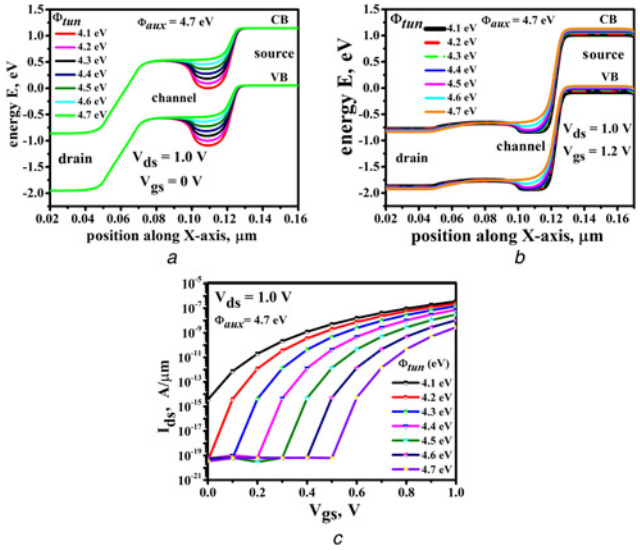

Fig. 5 *Energy bands along the length of device for different ϕ_{tun} and $\phi_{aux} = 4.7$ eV*
a OFF-state
b ON-state
c I_{ds} versus V_{gs} characteristics

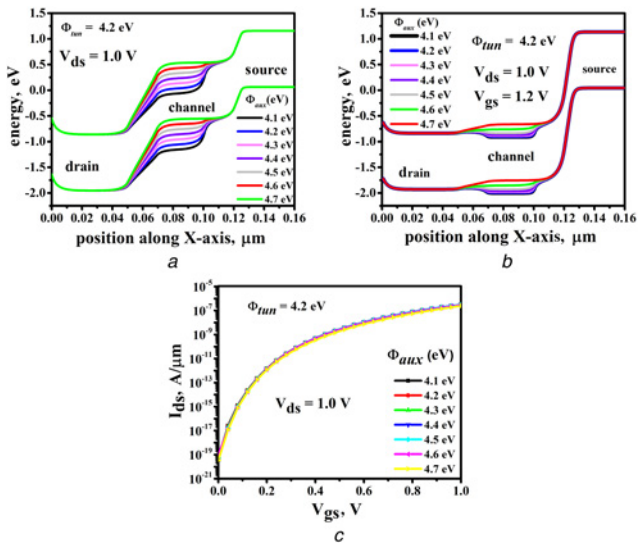

Fig. 6 *Energy bands along the length of device for different* ϕ_{aux} *and* $\phi_{tun} = 4.2$ *eV*
a OFF-state
b ON-state
c I_{ds} versus V_{gs} characteristics

show the effect of ϕ_{tun} variations on energy bands of the proposed device DMG-ED-TFET in OFF and ON states. In both the figures, it is seen that as we increase the workfunction of tunnel gate, tunnelling width at source/channel junction increases and tunnelling of carriers from source to channel get reduced. It results in degradation in ON-state current, SS and increment in V_{th} as depicted in Fig. 5*c*, which illustrate I_D versus V_{gs} curve for DMG-ED-TFET for different ϕ_{tun}. Same figure demonstrates, if ϕ_{tun} goes below 4.2 eV, then leakage current increase 10^4 times, opposite to that, reduction in ON-state current with increment in SS and threshold voltage has been found with increment in ϕ_{tun}. Similarly, now the auxiliary gate workfunction (ϕ_{aux}) varied from 4.1 to 4.7 eV and the tunnel gate workfunction (ϕ_{tun}) kept constant at 4.2 eV.

Figs. 6*a* and *b* show energy band diagram of DMG-ED-TFET in ON and OFF-state for different (ϕ_{aux}) ranging up from 4.1 to 4.7 eV. Since auxiliary gate is placed near drain channel junction, variation in (ϕ_{aux}) causes movement in energy bands under channel region, as shown in same figures. Deviation of energy bands does not affect tunnelling width at source/channel interface, so drain current remains independent from variation of (ϕ_{aux}) as shown in Fig. 6*c*. The figure indicates almost same drain current as a function of V_{gs} for complete range of ϕ_{aux}. Above optimisation gives optimised values of $\phi_{aux} = 4.7$ eV and $\phi_{tun} = 4.2$ eV and provide space for choosing the appropriate workfunction to reduce the fabrication complexity and cost efficiency.

5. Conclusion: In this work, comparative analysis of ED-TFET with DMG-ED-TFET has been studied. The conventional ED-TFET suffers from poor DC, RF and linearity performances but the proposed device (DMG-ED-TFET) has overcome those problems. Lower workfunction of tunnel gate (i.e. 4.2 eV) reduces the tunnelling barrier at source–channel interface, and enhances the device performance in terms of linearity (g_{m3}, VIP3, IIP3 and IMD3), DC and RF (C_{gd}, f_T, GBP) characteristics. Further optimisation of tunnel gate workfunction and auxiliary gate workfunction assist to select appropriate workfunction, i.e. 4.2 and 4.7 eV, respectively.

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