Reliability improvements in SOI-like MOSFET with ESD and self-heating effect

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Published in Micro & Nano Letters; Received on 2nd May 2018; Revised on 26th June 2018; Accepted on 24th July 2018

A new structure of N-type Silicon-on-insulator (SOI)-Like Bulk Silicon (N-SL-BS) metal–oxide–semiconductor field-effect transistor (MOSFET) is proposed to improve the reliability of SOI MOSFET mainly with regards to their self-heating effect and electro-static discharge (ESD) events based on two-dimensional numerical simulation. The new device employs p/n–/p + structure on Si, in which the n-layer is made of Si carbide (SiC), a wide bandgap material. The built-in electric field fully depletes the n-SiC layer and forms an SOI-like feature with a p + layer underneath. Simulations are first implemented in self-heating conditions, to investigate their drain current and temperature ramping. More importantly, ESD pulses assuming the human body model are applied to test their response and observe which device was first to fail using an *I–V* curve and hole current density distribution. Results show that the new device exhibits superior reliability when compared with a traditional SOI MOSFET. The avalanche breakdown voltage improves nearly 33% and the highest temperature of the global device is more than three times lower than that of an SOI MOSFET subjected to ESD pulses with a peak current of 7 mA.

1. Introduction: The reliability of silicon on insulator (SOI) devices can be challenged by their inferior thermal dissipation or electro-static discharge-induced (ESD) failures. These two problems lead to self-heating effects (SHEs) and low avalanche voltages when ESD events occur because accumulated carriers prevented by the buried oxide (BOX) are easily collected by the drain [1]. Also, the sharp increase in temperature can cause the silicon (Si) to melt and conduct path formation between the source and drain [2].

Several attempts have been made to solve these issues including using a Si germanium region as a well to decrease SHEs [3]. ESD protection divided into external protection and self-protection has been proposed by previous researchers with significant achievements. In terms of external protection, Z^2-field-effect transistor (FET) (zero subthreshold swings and zero impact ionisation FET) devices, fabricated using ultra-thin body and BOX SOI technologies and an integrated SOI substrate-diode structure have proven to be the ideal devices of the SOI circuits [4, 5]. In terms of self-protection, Zhang *et al.* [6] proposed a laterally diffused MOS (LDMOS)–Si-controlled rectifier device to replace the typical LDMOS to achieve LDMOS self-protection. However, the study of the self-protection within SOI devices is still unexplored. It will be an important progress if we try to make improvements to its self-protection.

In this Letter, a self-protection device (N–SL–BS) is proposed to solve the two problems mentioned above. The device adopts a p/n–/p + structure using Si carbide (SiC), with improved thermal conductivity to solve the first problem, the thermal conductivity coefficient of SiC is 59 W/m K, whereas that of Si dioxide (SiO_2) is only 1.4 W/m K [7, 8]. Moreover, the p + layer is a low carrier-life region. This means carrier recombination occurs at increased speeds, thereby avoiding carrier accumulation and solving the second problem [9].

Generally, ESD robustness is measured using the avalanche breakdown voltage (V_{t1}), the holding voltage to maintain a parasitic bipolar operation (V_h), and the failure current (I_{t2}).

2. Simulation of device and basic characteristic: In this section, the normal operation of the SOI and N–SL–BS devices is simulated. Figs. 1*a* and *b* show the schematics of N–SL–BS and SOI devices, respectively, and the device parameters are shown in Table 1. The n-doped regions beside the drain and source prevent short channel effects from occurring. Fig. 2 shows the I_{ds}–V_{gs} curves and the output characteristics. The output characteristic curves show that the average I_{ds} of the N–SL–BS device is slightly lower than that of the SOI device while neglecting SHEs. It is also seen from the I_{ds}–V_{gs} curves that the threshold voltage of the N–SL–BS device is larger than that of the SOI device. This implies that the short channel effect within SOI devices is worst than that in the N–SL–BS device. This is mainly due to the floating body effect within SOI devices. Thus, accumulated charge can increase the body potential and lead to the reduction of the threshold voltage. In short, the new structure has similar performance in common state.

Two Si/SiC heterojunctions are contained within the N–SL–BS device. Stress, which is induced by lattice mismatch, always exists at heterojunctions and has a negative impact on the quality of the heterojunction. This is the most important issue limiting the feasibility of production of real N–SL–BS devices. The epitaxy of Si/SiC thin films with a p/n–/p + structure has previously been studied [10, 11]. Although the isostructural lattices of Si and 4H-SiC present a high lattice mismatch that leads to a strain-induced surface roughening of the Si layer during growth, Si atoms would preferentially incorporate in the peaks as this is energetically favourable, leading to the partial relaxation of the lateral strain [12]. It is shown that the effect of strain-induced surface roughening is enhanced with increasing thickness of the grown layers, up to a maximum root mean square of 700 nm extracted for the Si sample. Thus, the strain-induced surface roughening is reduced as the thickness of the epitaxial Si layer within the N–SL–BS device is only 50 nm, and the stress induced by lattice mismatch between the 4H-SiC and the Si layer can be ignored. Therefore, higher-quality Si/SiC thin film heterojunctions can be achieved.

3. SHEs and ESD response: The models used include the Aorora mobility model and the Shockley–Read–Hall recombination model which uses concentration-dependent lifetimes. The thermal contact

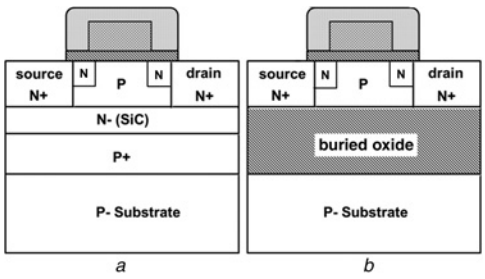

Fig. 1 *Device schematics for*
a N–SL–BS device
b SOI device

Table 1 Device parameters of N–SL–BS/SOI MOSFET

Device parameters	N–SL–BS	SOI
N^+ source/drain doping, cm^{-3}	1.0×10^{20}	1.0×10^{20}
p-type Si film doping, cm^{-3}	3.0×10^{18}	3.0×10^{18}
thickness of p-type Si film, nm	50	50
n^- SiC doping, cm^{-3}	1.0×10^{15}	—
thickness of n^- SiC, nm	5	—
P^+ region doping, cm^{-3}	1.0×10^{19}	—
n-type LDD (Lightly Doped Drain) doping, cm^{-3}	2.0×10^{18}	2.0×10^{18}
thickness of n-type LDD, nm	30	30
thickness of P^+ region, nm	30	—
BOX insulator thickness, nm	—	100
gate oxide thickness, nm	10	10
gate work function, eV	4.15	4.2
p substrate doping, cm^{-3}	1.0×10^{15}	1.0×10^{15}
gate channel length, nm	60	60

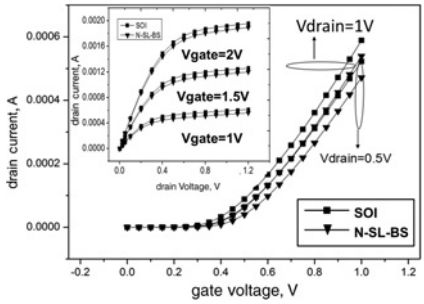

Fig. 2 *I_{ds}–V_{gs} curves and output characteristics of N–SL–BS and SOI MOSFET*

position is at the bottom of the device and external temperature is 300 K. Drain voltage increases from 0.04 to 0.84 V and the gate voltage is maintained at 1 V. Fig. 3 shows how drain current and device temperature vary with respect to drain voltage. The device temperature is measured at the centre of the Si film within the device. It can be observed that the drain current of the SOI device has decreased in the presence of SHE compared with the drain current with no SHE (NSHE). This is a typical change caused by the SHE. The low thermal conductivity of the BOX layer traps the heat and leads to SHE. However, the N–SL–BS device generated identical curves under these two conditions (SHE and NSHE). This is due to the lack of BOX layer and the high thermal conductivity of 4H-SiC. The temperature of the SOI device is significantly higher than that of the N–SL–BS device at relatively high drain voltages. This implies that the new structure proposed reduces SHEs.

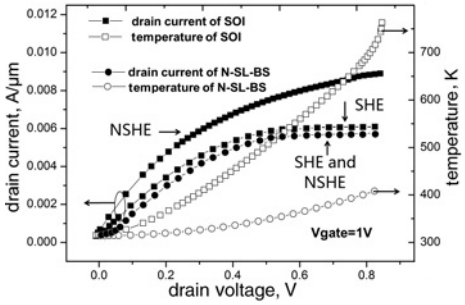

Fig. 3 *Drain current (with and without the SHE) and temperature under self-heating with 1 V gate voltage of SOI and N–SL–BS devices*

In this Letter, the human body model (HBM) is used to simulate the ESD pulse since it commonly occurred in real device applications. Different amplitudes of transient current are fed to the drain terminal with a rise time of 10 ns and an exponential decay time of 150 ns, which are the standard parameters of HBM. Specifically, peak currents of 1, 4, and 7 mA are supplied and the parameters of V_{t1}, I_{t1}, and V_h are measured to investigate the ESD responses of the two devices. The thermal environment is kept the same as before. Fig. 4 shows the I_{ds}–V_{ds} curves of the SOI and N–SL–BS devices under the HBM test with peak currents of 1, 4, and 7 mA. Obviously, the slope of the I_{ds} of the N–SL–BS device is less than that of the SOI device. It demonstrates that the on-resistance of the N–SL–BS device is less than that of the SOI device. The larger on-resistance results in greater temperature ramp-up, and eventually thermal failure. This is because the dielectric constant of SiC is smaller than that of SiO_2 and electrons and holes are easier to inject into the substrate. When the peak current amplitude is increased to 7 mA, it is found that the I_{ds} of the SOI device exhibits an obvious second snapback which does not exist in that of the N–SL–BS device. The main reason is that the potential in the depleted region is deeper in the film, forming a second bipolar path which is related to the floating-hole zone in the Si film [13, 14]. Since the SOI has the floating body effect, it builds up a floating holes zone. Although the second snapback does not represent secondary breakdown, the second bipolar path formation and its current increase are also threats to the device.

In general, higher V_{t1}, lower V_h, and lower R_{on} are ideals for improved ESD responses [15]. Figs. 5 and 6 show V_h and V_{t1} of the devices, respectively. The exact values of V_h and V_{t1} are shown in Table 2. It can be seen that the holding voltages (V_h) of the SOI device are higher than those of the N–SL–BS device, regardless of the peak current. For example, with a peak current of 1 mA, the holding voltage of the N–SL–BS device is 0.7 V, whereas that of the SOI device is 0.75 V. The increased carrier concentration within the N–SL–BS device extends the carrier lifetime

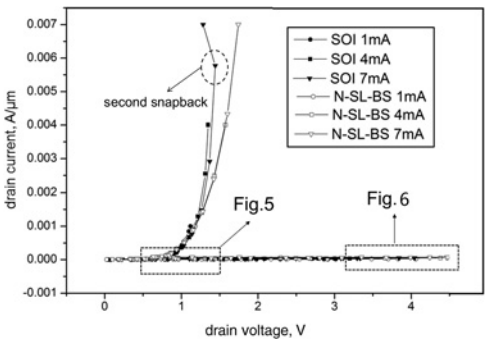

Fig. 4 *I_{ds}–V_{ds} curves of SOI and N–SL–BS devices under HBM test with peak currents of 1, 4, and 7 mA*

doi: 10.1049/mnl.2018.5124

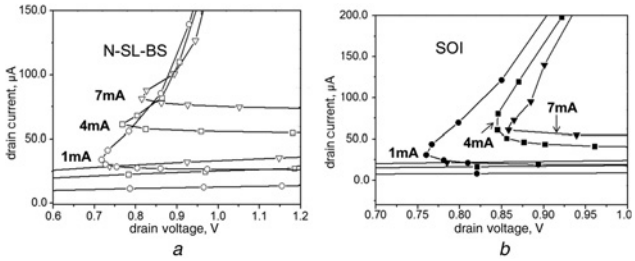

Fig. 5 *Magnification of V_h of N–SL–BS and SOI under ESD test with peak currents of 1, 4, and 7 mA*
a N–SL–BS device
b SOI device

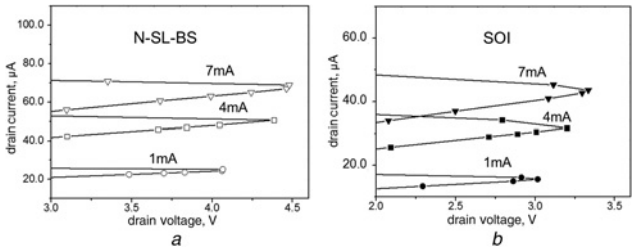

Fig. 6 *Magnification of V_{t1} of N–SL–BS and SOI under ESD test with peak currents of 1, 4, and 7 mA*
a N–SL–BS device
b SOI device

Table 2 Exact values of V_h and V_{t1}

	N–SL–BS		SOI	
	V_h, V	V_{t1}, V	V_h, V	V_{t1}, V
1 mA	0.70	4.1	0.75	3.0
4 mA	0.75	4.4	0.84	3.2
7 mA	0.82	4.5	0.85	3.4

in the base. So the amplification factor β of the parasitic bipolar is larger and the holding voltage is reduced [16]. As the value of the peak current increases, the holding voltage increases too. In this situation, the large injection effect is remarkable in SOI so the base effective width becomes narrower. The carrier recombination rate is less and it increases carrier lifetime.

In Fig. 6 and Table 2, it can be seen that the V_{t1} of the N–SL–BS device is higher than that of the SOI device, regardless of the peak current. For example, with a peak current of 1 mA, the V_{t1} of the N–SL–BS device is about 4.1 V and that of the SOI device is 3.0 V. When the device experiences an ESD pulse, the electric field of drain begins to increase. When the electric field of the space charge region reaches the critical point, the p-n junction experiences avalanche breakdown. In the N–SL–BS device, the depleted layer is larger so the avalanche breakdown voltage is greater.

To investigate the influence of the doping concentration on the ESD response, the concentration of the n-SiC layer is increased from 10^{15} to 10^{19} cm^{-3} with a fixed p+layer concentration of 10^{19} cm^{-3} and the concentration of the p+layer increased from 10^{15} to 10^{19} cm^{-3} with a fixed n-SiC layer concentration of 10^{15} cm^{-3} in Fig. 7. It shows that V_{t1} increases by about 1 V when the p+layer concentration is increased or the n-layer concentration is decreased. Thus, heavy doping of the p+layer and light doping of the n-SiC layer is adopted to increase the depletion

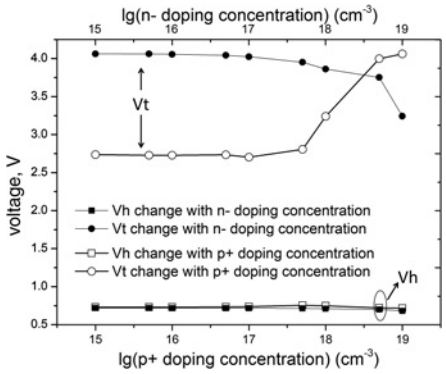

Fig. 7 *V_{t1} and V_h vary with respect to n-layer or p-layer concentration changes. When n-layer concentration changes, the p-layer concentration is fixed at 10^{19} cm^{-3} and when p-layer concentration changes, the n-layer concentration is fixed at 10^{15}cm^{-3}*

zone, and consequently the V_{t1}. On the other hand, V_h is unaffected by changes in the doping concentrations.

4. Structure feature and device failure: The main problem with SOI devices is that the SiO_2 layer provides thermal insulation which results in poor thermal dissipation along the vertical direction [17]. To study this further, Fig. 8 shows the temperature distributions of the two devices with peak currents of 1, 4, and 7 mA. It is clear that as the peak current amplitude increases, the temperatures of both devices increase. Yet, the temperature of the SOI device is significantly higher than that of the N–SL–BS device. This shows that the n-SiC and p+layers offer improved heat transfer compared with the SiO_2 layer in SOI devices. Given that the temperature of the SOI device ramps up to 1700 K, and the melting point of Si is 1685 K [18], it is likely that the PN junction will be short-circuited when the Si melts and a conduction path is formed.

To observe this phenomenon, the holes current density within the Si film is measured. If the Si melts and forms a conduction path between the source and drain, the holes will flow through the PN junction to the drain region, thereby raising the holes current density in the drain region. Fig. 9 shows the holes current density

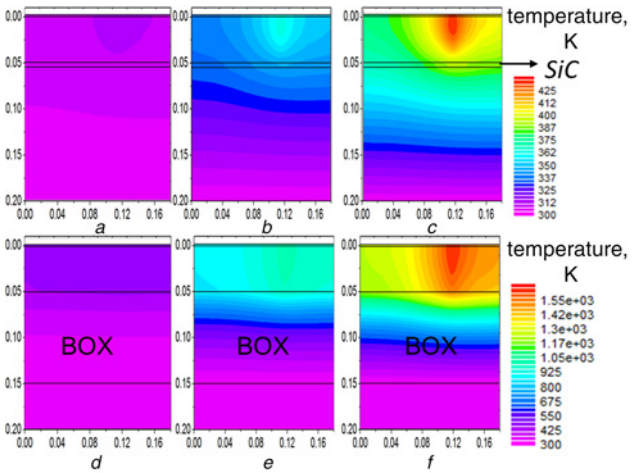

Fig. 8 *Temperature distributions under HBM test with peak currents of*
a 1 mA of N–SL–BS
b 4 mA of N–SL–BS
c 7 mA of N–SL–BS
d 1 mA of SOI
e 4 mA of SOI
f 7 mA of SOI

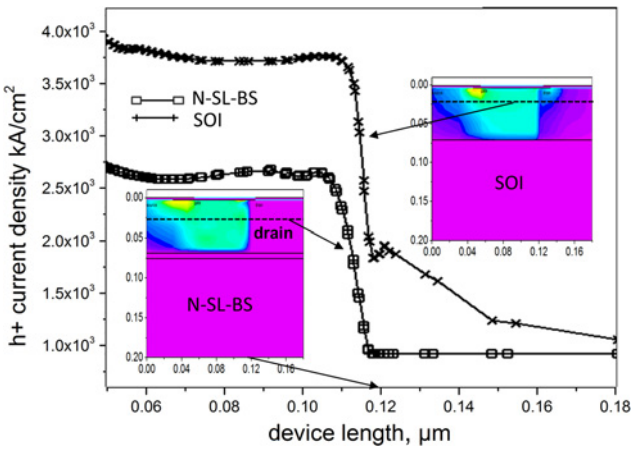

Fig. 9 *Hole current density within the SOI and N–SL–BS devices under HBM test with 7 mA peak current*

within the SOI and N–SL–BS devices under the HBM test with 7 mA peak current. The current density curve is obtained along the device width at the length of 0.02 μm, as indicated by the dashed lines in the device feature pictures shown as insets. It can be seen that there is a sharp drop in the hole current density at the boundary of the drain and source within the N–SL–BS device but there is a taper in the holes current density at the boundary within the SOI device. Clearly, the SOI device has failed, as evidenced by the raised holes current density in the region under the drain.

5. Conclusion: This Letter proposes an N–SL–BS device with a p/n–/p + structure using SiC to reduce SHE and improve the ESD response. In the above simulations, it has been shown that, compared with the typical SOI metal–oxide–semiconductor FET (MOSFET), the N–SL–BS device has reduced SHEs and achieved a 1.1 V increment in V_{t1} and a 0.05 V decrement in V_h under HBM test with a peak current of 1 mA. Besides, the second snapback phenomenon observed in the drain current of the SOI device has been eliminated. Simulation results have also verified that the temperature of the N–SL–BS device is more than 1000 K lower than that of the SOI device under a 7 mA ESD pulse. In short, the proposed device is well self-protected. Other aspects of the device's reliability may be investigated in future.

6. Acknowledgments: This work was supported in part by the National Natural Science Foundation of China (grant no. 61774052) and in part by the Excellent Youth Foundation of Zhejiang Province of China (grant no. LR17F040001).

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doi: 10.1049/mnl.2018.5124