Investigation of RF and linearity performance of electrode work-function engineered HDB vertical TFET

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This work realises a hetero-dielectric buried oxide vertical tunnel field effect transistor (HDB VTFET) and investigates its radio frequency (RF) and linearity characteristics. First time, the concept of hetero-dielectric buried oxide (BOX) in VTFET is used to obtain the superior improvement in terms of different RF and linearity figure of merits such as C_{gs}, C_{gd}, C_{gg}, f_T, Gain Bandwidth Product (GBP), τ, Transconductance Frequency Product (TFP), Transconductance Generation Factor (TGF), g_{m2}, g_{m3}, VIP_2, VIP_3, IIP_3, IMD_3 and 1-dB compression point. Also, the influence of HfO_2 BOX length scaling on these FOMs is analysed. The results reveal that the HDB VTFET can be a promising contender to replace bulk metal-oxide semiconductor field-effect transistors in analogue/mixed signal system-on-chip and high-frequency microwave applications and the accuracy of this device is validated by TCAD Sentaurus simulator.

1. Introduction: In the present scenario, the advancement in modern wireless and mobile communication industry requires cost-effective and highly efficient radio frequency (RF) designs capable to handle weak signals for high-performance communication systems. To enhance the signal quality, the two important candidates are low-noise and high-power amplifiers. On the other hand, the existence of higher-order harmonics causes the non-linear behaviour of the device owing to the loss of information [1, 2]. Therefore, it is the primary concern to choose the device which ensures the minimal influence of inter-modulation distortions and high-order harmonics on the reliability of the device [3, 4]. Thus, a novel device having a lower value of subthreshold slope (SS) is required. For this purpose, field effect transistors (FETs) are chosen as the basic building blocks to design such type of systems. In metal-oxide semiconductor FETs (MOSFETs), the current-switching process includes thermionic emission mechanism through which carriers over an energy barrier inject from the source to the channel. This gives an essential limit in terms of the steepness of SS around 60 mV/decade at room temperature [5, 6]. In previous years, to overcome the essential limit, several novel devices have been designed. They include emerging devices such as nanoelectromechanical FETs, impact ionisation metal-oxide semiconductor (MOS) devices, dopingless-impact ionisation MOSFET (IMOS) devices, tunnel FETs (TFETs) and so on [7, 8]. Among them, TFET has been considered as the most promising potential device for ultra-low-power applications.

TFETs have received a lot of attention by providing the low value of OFF-current and SS below 60 mV/decade at room temperature because electron flow is controlled by band-to-band tunneling (BTBT) mechanism [9–12] and they can achieve a higher ratio of I_{ON}/I_{OFF} compared to MOSFETs [13]. Recently, various techniques such as high-k dielectric materials [14], multi-gate TFET technology [15, 16], hetero-based architectures [17–20], source pocket based devices [21], junction-less concept based devices [22, 23] have been investigated to boost the drain current. It is also investigated that hetero-dielectric buried oxide (HDB) offers a significant decrease in the ambipolar behaviour in TFET by controlling tunnelling width at the channel-drain interface [24]. In addition to these benefits, TFETs exhibit enhanced RF and linearity performance. The RF and linearity analysis is still an unexplored area in HDB vertical FET (HDB VTFET) and needs to be analysed too.

This Letter investigates the RF and linearity performance of HDB VTFET, underlapped channel drain HDB VTFET (UCD-HDB VTFET) and channel drain HDB VTFET (CD-HDB VTFET). The proposed structure includes HfO_2 below the drain region, SiO_2 below the source and channel regions, and two metal electrodes for source and drain with different work-functions on an intrinsic film grown over SiO_2 and HfO_2, respectively. HDB VTFET design is optimised for different BOX lengths of HfO_2 dielectric i.e. 60, 70 and 80 nm.

2. Device structure and parameters: Figs. 1*a–c* represent the schematic diagrams of proposed HDB VTFET, UCD-HDB VTFET and CD-HDB VTFET. HDB VTFET consists of SiO_2 under the source-channel regions, HfO_2 under the drain region. This device is having $L_{BS} = 110$ nm while $L_{BH} = 60$ nm. Similarly, UCD-HDB VTFET is the same as HDB VTFET, except that it comprises of HfO_2 under the drain-underlapped channel region. This device is having $L_{BS} = 100$ nm while $L_{BH} = 70$ nm. Similarly, CD-HDB VTFET is the same as HDB VTFET, except that it comprises of HfO_2 under the drain-channel region. This device is having $L_{BS} = 90$ nm while $L_{BH} = 80$ nm. Two spacers of HfO_2, having a dielectric constant of 22, of lengths 20 and 40 nm are used as a first spacer at the gate–drain electrode and a second spacer at source–gate electrode, respectively [25]. The proposed device comprises of metal M_2 (platinum) at source electrode, metal M_3 (molybdenum) at drain electrode and metal M_1 at the gate electrode.

All simulations are carried out with 2D Sentaurus TCAD simulation tool. BTBT model, bandgap narrowing model, Shockley–Read–Hall (SRH) model, drift-diffusion current transport model, Auger recombination, Lombardi mobility model is used for simulations to attain optimised results [26]. Table 1 shows the list of device simulation parameters.

3. Simulation results and discussion: This section represents the performance of RF and linearity characteristics.

3.1. Performance analysis of RF characteristics: The effect of parasitic capacitance is important to consider when a device works at a higher frequency. This parasitic capacitance is responsible for circuit oscillation at high-frequency which results in signal distortion. Therefore, these capacitances must be suppressed to reduce the signal distortion. As compared to other capacitances, C_{gd} play a crucial role to degrade the device performance. Therefore, it must be suppressed.

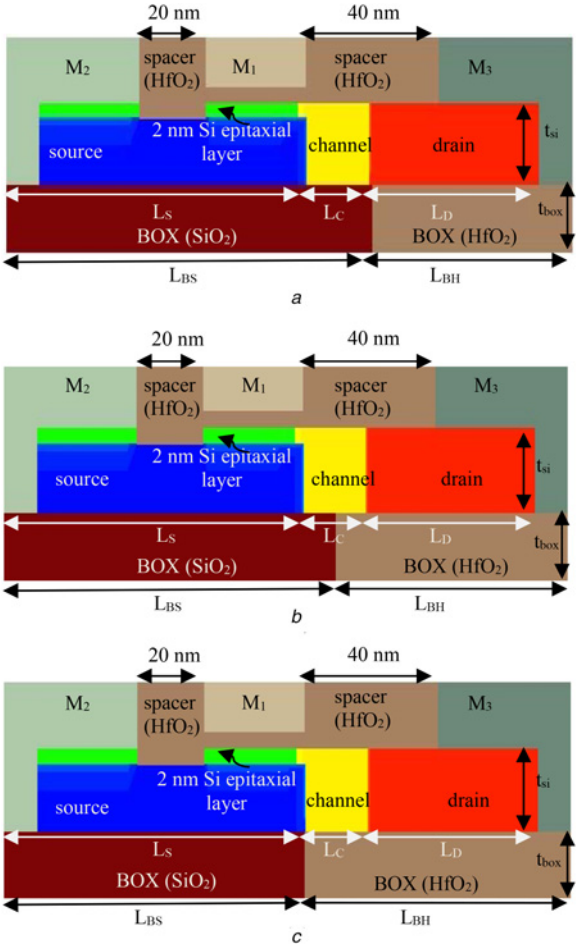

Fig. 1 *Schematic diagram of*
a HDB VTFET (L_{BH} = 60 nm)
b UCD-HDB VTFET (L_{BH} = 70 nm)
c CD-HDB VTFET (L_{BH} = 80 nm)

Transconductance (g_m) demonstrates the amplification capability of the device and can be formulated as

$$g_m = g_{m1} = \frac{\partial I_{ds}}{\partial V_{gs}}\ (\mathrm{A/V}) \tag{1}$$

where I_{ds} is the drain current and V_{gs} is the gate voltage. Comparison of transconductance for different BOX length devices is shown in Fig. 2*a*. UCD-HDB VTFET has shown the larger value of transconductance.

Fig. 2*b* shows that as a potential barrier at source-channel region decreases, it results in a decrease of C_{gs} with increase in V_{gs}. In HDB VTFET and UCD-HDB VTFET, C_{gs} is comparatively similar and higher in a comparison to CD-HDB VTFET owing to the presence of low-k BOX below the source and underlapped source-channel regions.

On the other hand, C_{gd} increases with increase in V_{gs} as a result of enhancing the potential barrier at the channel-drain region as depicted in Fig. 2*c*. In HDB VTFET and UCD-HDB VTFET, C_{gd} is comparatively similar and lower than CD-HDB VTFET owing to the presence of high-k BOX below the drain and underlapped channel-drain regions. It is noticed that HDB VTFET and UCD-HDB VTFET attained a slightly smaller value of total capacitance than CD-HDB VTFET as clarified in Fig. 2*d*, which is essential to reduce signal distortion.

To use the device for wireless applications, other RF parameters in terms of f_T, GBP, τ, TFP and TGF are also calculated. Fig. 3*a* demonstrates the changes in f_T with respect to V_{gs}. f_T is expressed as the frequency at which device operates and makes the short-circuit current gain falls to unity and calculated as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2}$$

HDB VTFET and UCD-HDB VTFET have almost similar and higher value of f_T as a result of the higher value of g_m than CD-HDB VTFET as observed in Fig. 3*a*. GBP is computed for certain DC gain of ten and calculated as

$$\mathrm{GBP} = \frac{g_m}{20\pi C_{gd}} \tag{3}$$

GBP plays an important role to offer the trade-off between bandwidth and gain for a given device. Fig. 3*b* depicts that higher value of GBP is obtained in HDB VTFET than UCD-HDB VTFET and CD-HDB VTFET as a result of a decrease in the value of C_{gd}. Another prominent parameter τ plays a vital role in RF circuits. It measures the time required by the charge carriers to travel the distance between source and drain regions and decides the switching speed. τ variation with V_{gs} is depicted in Fig. 3*c*. It is the reciprocal of f_T and formulated as

$$\tau = \frac{1}{2\pi f_T} \tag{4}$$

From the above equation, it can be observed that higher switching speed leads to a better response to the device. Thus, it can be noticed in Fig. 3*c* that better switching speed is obtained in HDB VTFET and UCD-HDB VTFET than CD-HDB VTFET. Further, TFP is another key parameter to

Table 1 Device simulation parameters

Parameter	HDB VTFET	UCD-HDB VTFET	CD-HDB VTFET
channel thickness (t_{si}), nm	10	10	10
BOX thickness (t_{box}), nm	8	8	8
oxide thickness (t_{ox}), nm	2	2	2
drain length (L_D), nm	50	50	50
channel length (L_C), nm	20	20	20
source length (L_S), nm	80	80	80
SiO_2 BOX length (L_{BS}), nm	110	100	90
HfO_2 BOX length (L_{BH}), nm	60	70	80
work function (φ_{M2}), eV	5.93	5.93	5.93
work function (φ_{M3}), eV	3.9	3.9	3.9
work function (φ_{M1}), eV	4.8	4.8	4.8
channel concentration (N_C), cm^{-3}	5×10^{15}	5×10^{15}	5×10^{15}
drain concentration (N_D), cm^{-3}	5×10^{18}	5×10^{18}	5×10^{18}
source concentration (N_A), cm^{-3}	5×10^{20}	5×10^{20}	5×10^{20}

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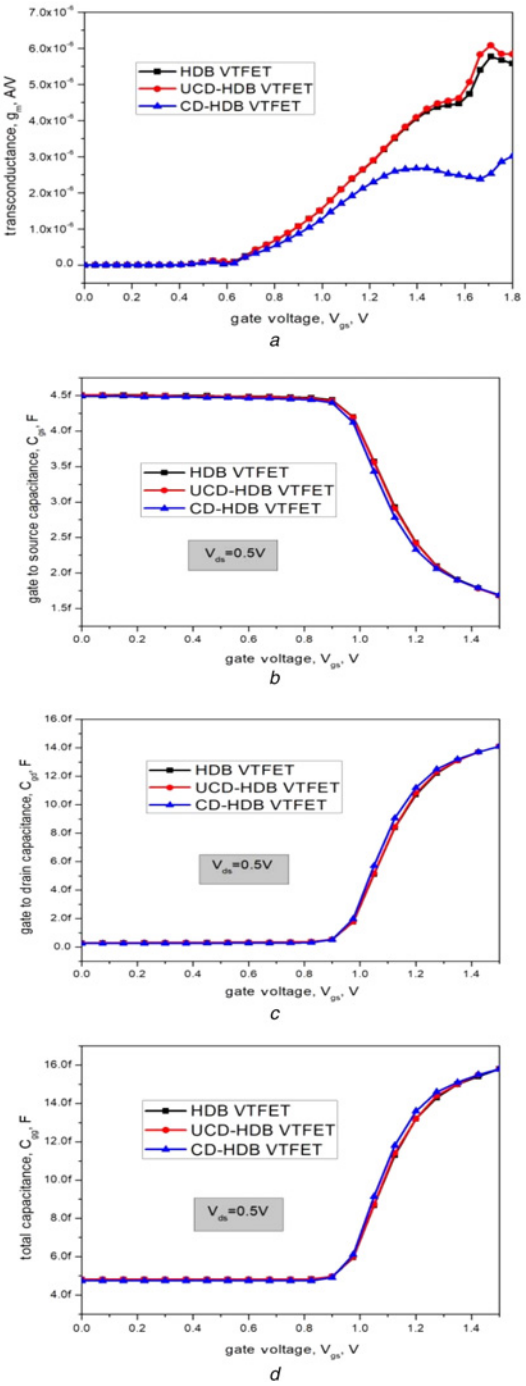

Fig. 2 *Variation of*
a g_m
b C_{gs}
c C_{gd}
d C_{gg} with respect to the gate voltage

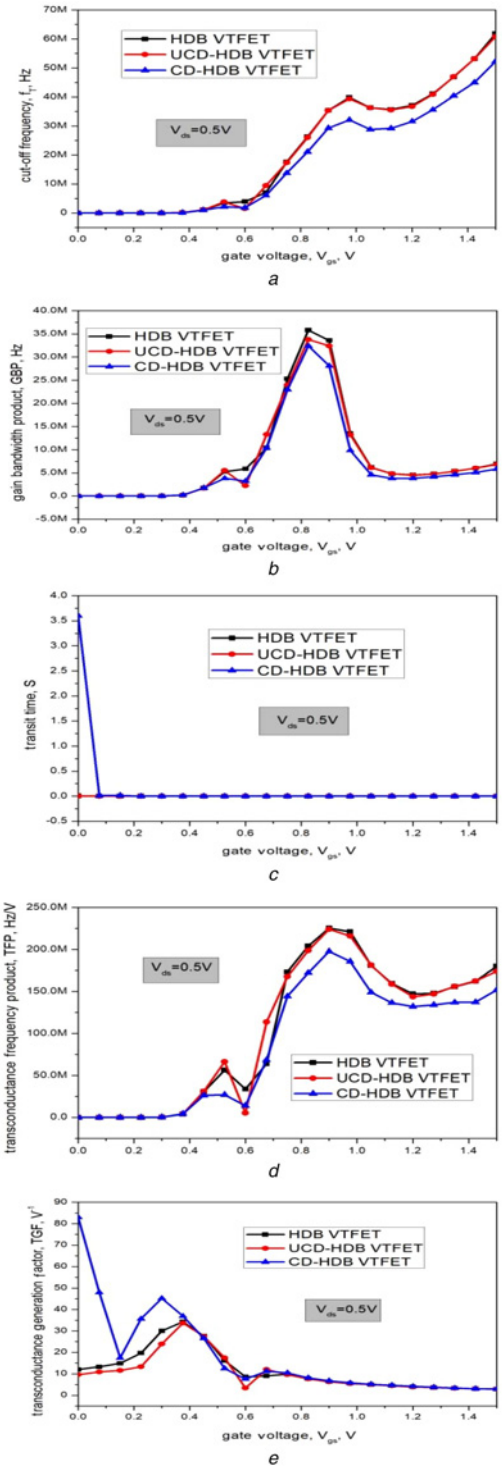

Fig. 3 *Variation of*
a f_T
b GBP
c Transit time
d TFP
e TGF with respect to the gate voltage

analyse the device behaviour for high-speed designs and is defined as

$$\text{TFP} = \left(\frac{g_m}{I_{ds}}\right) \times f_T \tag{5}$$

HDB VTFET and UCD-HDB VTFET have higher values of TFP than CD-HDB VTFET due to higher g_m as illustrated in Fig. 3*d*. TGF, also known as device efficiency, refers to the device ability to transform DC parameter (drain current) into AC parameter (g_m) and is calculated as

$$\text{TGF} = \frac{g_m}{I_{ds}} \tag{6}$$

The comparative plot of device efficiency is shown in Fig. 3*e*, where CD-HDB VTFET indicates higher efficiency than HDB VTFET and UCD-HDB VTFET.

3.2. Performance estimation of linearity characteristics: Linearity parameters are important for analysing device performance for RFIC designed system at the high-frequency regime.

The distortion must be minimum in the output signal over the required input voltage range for a system to be sustainable at high frequencies. The important parameters for linearity analysis of device are a third-order derivative of transconductance (g_{m3}) second-order voltage intercept point (VIP_2), third-order voltage intercept point (VIP_3), third-order intermodulation intercept point (IIP_3), third-order intermodulation distortion (IMD_3) and 1-dB compression point [27] which can be defined as below:

$$\mathrm{VIP}_2 = 4 \times \frac{g_{m1}}{g_{m2}} \tag{7}$$

$$\mathrm{VIP}_3 = \sqrt{24 \times \frac{g_{m1}}{g_{m3}}} \tag{8}$$

$$\mathrm{IIP3} = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} \times R_s} \tag{9}$$

$$\mathrm{IMD3} = R_s\left[4.5 \times \left(\mathrm{VIP}_3^3\right) \times g_{m3}\right]^2 \tag{10}$$

$$1\mathrm{-dB} = 0.22\sqrt{\frac{g_{m1}}{g_{m2}}} \tag{11}$$

where $R_s = 50\,\Omega$ is considered and $g_{mn} = \left(\partial^n I_{ds}/\partial V_{gs}^n\right)$, $n = 1, 2, 3, \ldots$

At first, g_{m2} and g_{m3} are discussed which may interfere with the frequency and leads to non-linearity. In this concern, g_{m3} is assumed to be a dominant parameter as compared to g_{m2}. Hence, the amplitudes of g_{m2} and g_{m3} must be smaller for the suppression of non-linear distortions in the output signal, because it is the main reason for distortion. Fig. 4*a* illustrates the lower peak value of g_{m2} for CD-HDB VTFET and UCD-HDB VTFET as compared to HDB VTFET. Fig. 4*b* demonstrates that HDB VTFET and CD-HDB VTFET give a lower peak value of g_{m3} as compared to CD-HDB VTFET.

In VIP_2, first and second order harmonics are equal. Fig. 5*a* shows the amplitude of VIP_2 of UCD-HDB VTFET is higher at low V_{gs} in comparison to HDB VTFET and CD-HDB VTFET which is required to attain the high linearity. In VIP_3, the first and third harmonics are equal. Fig. 5*b* depicts the higher peak value of VIP_3 of CD-HDB VTFET than HDB VTFET and UCD-HDB VTFET which results in a higher degree of linearity. The comparative graph of IIP_3 is demonstrated in Fig. 5*c*, where IIP_3 is higher for CD-HDB VTFET. Another important linearity parameter is IMD_3 in which the first and third harmonics are equal. It gives the degeneracy in the communication system. Fig. 5*d* shows the minimal value of IMD_3 with V_{gs} for CD-HDB

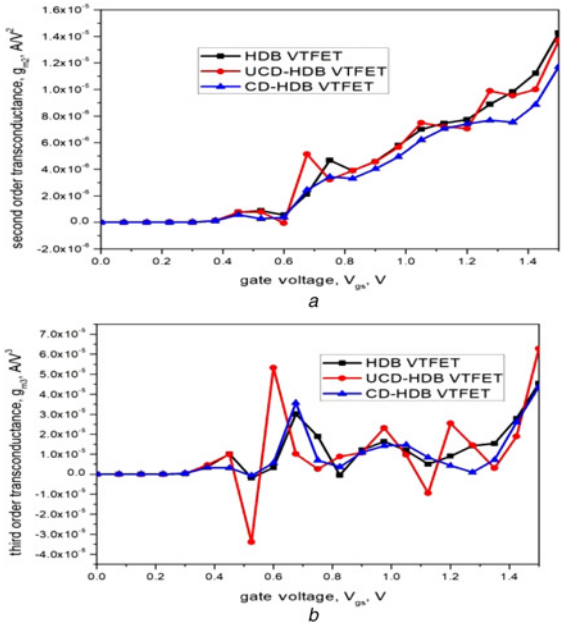

Fig. 4 *Variation of*
a g_{m2}
b g_{m3} with respect to the gate voltage

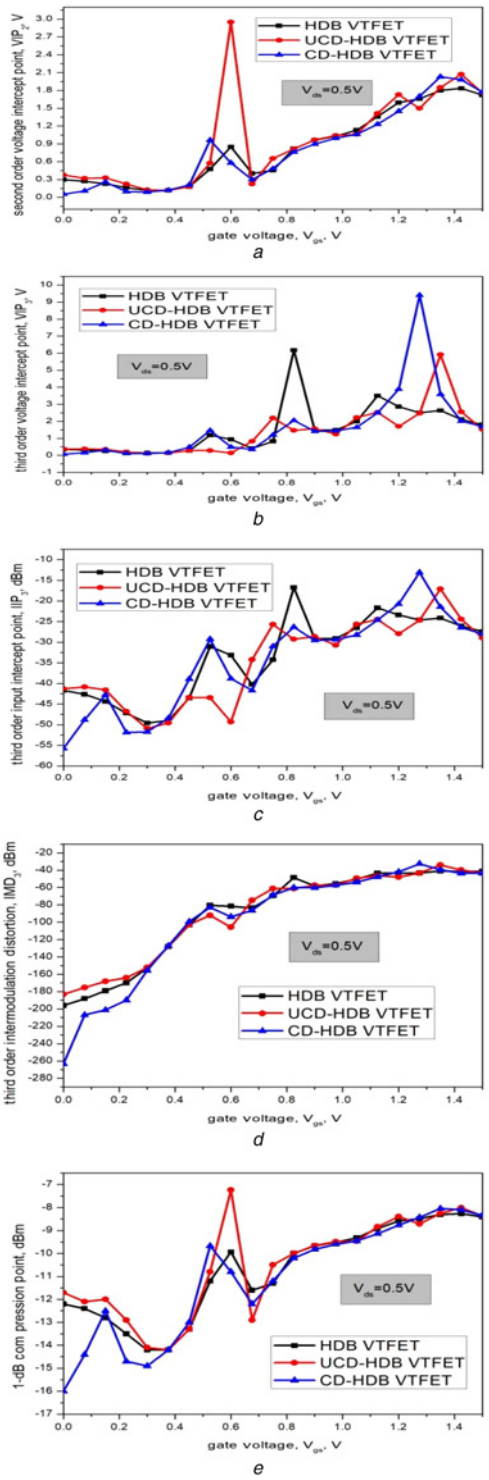

Fig. 5 *Variation of*
a VIP_2
b VIP_3
c IIP3
d IMD3
e 1-dB compression point with respect to the gate voltage

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VTFET than HDB VTFET and UCD-HDB VTFET which is necessary for a distortion-free communication system. 1-dB compression point gives the minimal value of input power from its model value to drop the gain by 1-dB. Fig. 5*e* illustrates the higher peak value of 1-dB compression point of UCD-HDB VTFET at lower gate voltage which is responsible to attain lower distortion and higher linearity.

4 Conclusion: The first time, the concept of HDB in air-bridge based VTFET is used to investigate the RF and linearity performance. It is observed that the RF performance of HDB VTFET and UCD-HDB VTFET is almost similar and better than CD-HDB VTFET. On the other hand, linearity analysis of VIP_3, IIP_3, IMD_3 for CD-HDB VTFET is superior due to a smaller value of g_{m3} which results in higher device efficiency. The lower value of g_{m2} offers the superior performance of VIP_2 and 1-dB compression point for UCD-HDB VTFET. These results reveal that high-k dielectric underlapped below channel region does not affect much the RF performance but results in higher linearity due to a minimal value of second-order transconductance (g_{m2}). Therefore, this device is a significant choice for mixed-signal SOC applications.

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