Symmetric dual gate insulator-based FinFET module and design window for reliable circuits

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High-k spacer and gate insulator materials have been exhaustively studied nowadays for the enhancement of electrostatic control and reduction of short-channel effects in scaled devices. The work presents a high-performance and charge trap tolerant FinFET module at 10 nm gate length. Dual layer gate insulator (inner low-k and outer high-k) introduces to reduce charge trapping from the channel and outside into the gate oxide. It reduces the gate leakage current by 51.6% compared to conventional FinFET. Further, they demonstrate single charge trapping (SCT) induce effects and proposed optimised high-k spacer width of the SCT tolerant design. SCT analysis is presented in different high-k spacer materials and back-gate voltages. Process variation sources such as line edge roughness and line width roughness are also analysed for the circuit design.

1. Introduction: Deposition of a metal gate on high-k dielectric HfO_2 is known to generate an oxygen vacancy (OV) defects. Positively charged OVs in the dielectric effect the gate electrostatics and modulate the effective gate work function (WF). The OVs also increase the number of dangling bonds at the silicon–insulator interface [1, 2]. Recently, various results were published relating to the inversion charge density in FinFET structures. Researcher shows improved inversion charge density in nanoscale FinFETs at the presence of a sharper electric field with high-k gate insulators [3]. The inversion charge density is important to understand charge trapping, where the charge injection into the bulk dielectric, affects the single charge trap (SCT) and bias temperature instability in addition to the interface degradation [4]. Moreover, the SCT induced noise, bias temperature instability, and process variations (PVs) are the major issues for future device development. SCT in the semiconductor has the long history when it has predicted by Wallmark and Marcus [5]. It becomes one of the primary sources of functioning errors in highly scaled technologies [6].

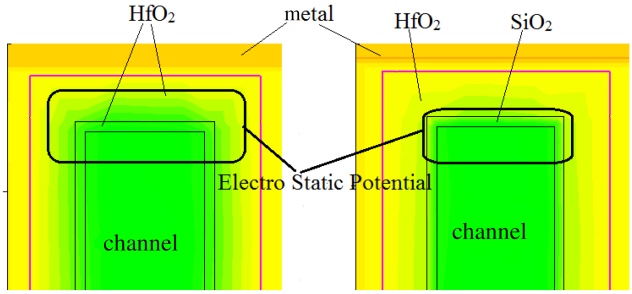
Universe (space) contains the number of high energy particles such as α, β and *COSMIC* rays. These high energy particles may trap into the semiconductor devices through the IC package and make a circuit unstable. Major reliability issues come when these particles trap into the silicon–insulator interface [7]. This analysis is disused by Fan *et al.* [8] for the single gate and individual (double) gate-based FinFETs. They determine the dynamic current due to trapping and de-trapping of charge carriers. Further, he did the SCT analysis for tunnel FinFET with varying WF, it extended for FinFET, Si/Fe nanowire field-effect transistors (FETs) [9]. Artola *et al.* [10] also found that SCTs become a major source of reliability losses. As all the above mention works present the SCT analysis for low-k gate insulator-based FinFETs. Dual-k gate insulator reduces the significant charge trapping effect into the gate insulator and dual-k asymmetric spacer-based FinFET (SDS-FinFET) helps to improve inversion charge [11]. In the proposed work, dual-k insulator and symmetric high-k inner space use to improve reliability and performance, respectively. Proposed optimised high-k space length along with low-k spacer technology also reduce SCT effects by reducing the fringing electric field. SCT is also analysed for independent gate FinFET and gives the solution how this can compensate using back gate biasing. Further, we also studied the effect of the device structure, i.e. 3D SDS-FinFET versus FinFET structure. We did a PV analysis along with SCT and proposed a probabilistic design window using a Gaussian distribution-based 5000 Monte Carlo (MC) simulations.

The remaining part of the paper is organised as follows. In Section 2, we describe the simulation setup and calibration of the 10 nm symmetric high-k spacer FinFET. In Section 3, we present the analysis of SCT effects for SDS-FinFET. The SCT effect of spacer width optimisation is also discussed in this section. PV along with SCT analysis and probabilistic circuit design window discusses in Section 4. The final recommendation and conclusion of the work are presented in Section 5.

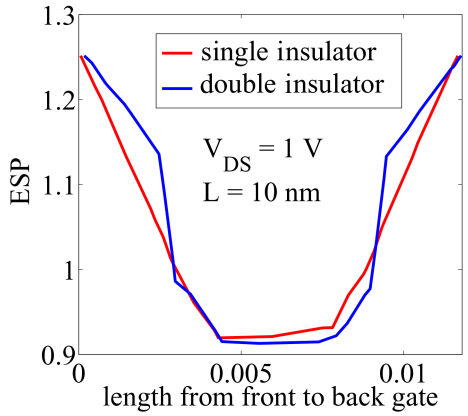
2. Device structure and model calibration: The proposed symmetric dual high-k spacer FinFET (SDS-FinFET) is simulated using Synopsys 3D TCAD device simulator [12]. We use appropriate physical models for the proposed device simulation to consider carrier mobility, scattering, SCT and the effects of lateral and perpendicular fields. The gate leakage current is simulated using direct tunnelling model along with the fixed charge carrier. The mobility degradation at the semiconductor–insulator interface is simulated using the Lombardi mobility model. The single trapped charge model adopted for the SCT analysis as discussed in Synopsys TCAD service manual [12]. The PV effect is simulated using tilt and distorted channel according to line edge roughness (LER) and line width roughness (LWR). Different device samples are generated for TCAD. The simulation data are the further model using system Verilog for spice simulation.

The device structure consists of a square shaped silicon fin under the insulating layer at gate regime. The gate terminal grew using a metal layer implantation over the insulating layer. We proposed gate insulator engineering using inner (over silicon) low-k (SiO_2) and over its high-k (HfO_2) materials as shown in Fig. 1*a*. Inner low-k gate-insulator reduces total dangling bond density at silicon–insulator interface which decreases bias temporal instability, hot-carrier injection (HCI) and other direct/indirect charge trappings whereas outer high-k dielectric reduces the short-channel effects, gate leakage current, and drain induced barrier lowering (DIBL). The electrostatic potential in a channel for single (high-k) and double (low- and high-k) layer gate-insulator-based FinFET is shown in Fig. 1*b*. The result shows the small spread in the potential for proposed SDS-FinFET. The proposed device reduces the gate leakage current by a very high margin as shown in Fig. 1*c*.

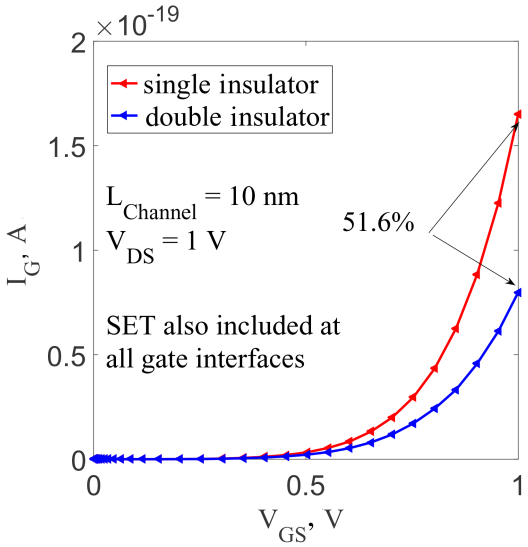
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a

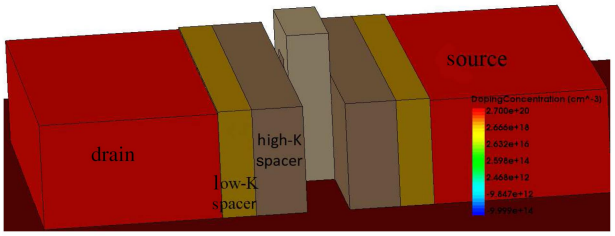


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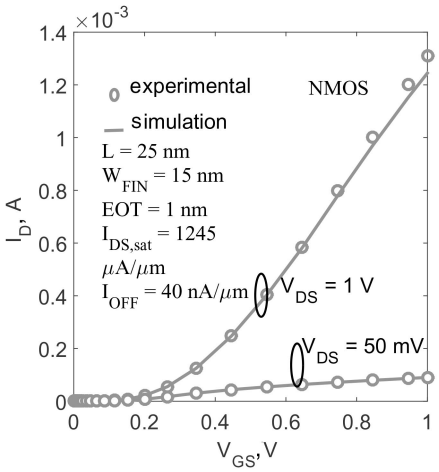


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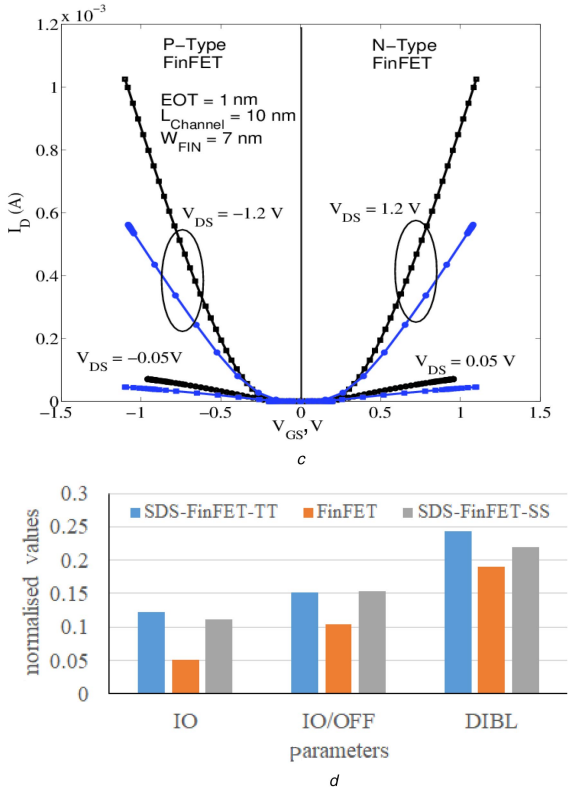
Fig. 1 *Proposed SDS-FinFET and their analysis*
a 2D cross-section view of proposed double gate insulator-based FinFET
b Electro static potential with, respective, length
c Gate leakage current due to direct and indirect charge trapping



a



b



c d

Fig. 2 *Comparative analysis of proposed SDS-FinFET*
a Cross-section view of symmetric dual-k spacer FinFETs Calibration of TCAD models with experimental data at
b $L_G = 25$ nm
c Conventional and proposed SDS-FinFET ($L_G = 10$ nm)
d Normalised design metrics comparison among the conventional and SDS-FinFET

As the proposed device improves ON current and reduces gate leakage current hence increase the ON/OFF current ratio. Moreover, practical fabrication over a silicon of HfO_2 is also difficult, whereas in the proposed device first SiO_2 fabricated on silicon hence it also allows practical fabrication. Further, the source and drain have the Gaussian doping profile which forms the ohmic junction and improves the ON current [13]. The channel region has the uniform doping profile at 1×10^{15} cm^{-3}. The 2D cross-section of the proposed device is shown in Fig. 2*a*.

We calibrate the simulation setup with experimental data (fabricated devices) of channel length 25 nm [14] and the results are as shown in Fig. 2*b*. Our simulations show excellent matching at low and high V_{DS}. The calibrated device is scaled according to keep the TCAD device structure, channel doping, the source-drain doping profiles as per the fabricated device. These are taken

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according to meet the specifications of ITRS 2015 projections [15]. The additional dual-k gate insulator and symmetric dual-K spacers are introduced. Symmetric dual high-k spacer-based FinFET consisted of inner high-K (HfO_2) and outer low-K spacer (Si_3N_4). Further, the inner high-k and outer low-k spacer width are also optimised for the largest possible performance. The method of fabrication of dual-k spacer is already discussed in [16, 17] therefore, experimental device fabrication is possible for proposed device. The device dimension, doping and other parameters of the proposed device are shown in Table 1.

Fig. 2*c* shows the comparative $I - V$ characteristics for proposed SDS-FinFET and standard FinFET. The improvement in digital performance metrics is using SDS-FinFET structure over the conventional FinFET with increasing spacer permittivity as shown in Fig. 2*d*. SDS-FinFET shows the improvement in drive current with an almost 40–80% reduction in OFF-state leakage current (I_{OFF}) than conventional FinFET. Inner spacer permittivity (K) varied from 3.9 to 25, with a reduced DIBL of 69% and sub-threshold slope of 7.5%. Therefore, SDS-FinFET device with higher inner-spacer permittivity comprehensively outperforms the conventional, high-k and SDS-FinFET devices with lower inner spacer permittivity. The optimised length high-k with low-k spacer also improves ON current due to reduced parasitic capacitance and scattering due to electric fields across the source. Further, we analysed the SCT for N-type and P-type FinFETs for the proposed device [18].

3. Single charge trapping analysis: In this section, we discuss the effects of SCT on proposed SDS-FinFET [7]. Our investigations focus on the change in the I_D induced by the trapping of an individual electron in an acceptor type interface state at the Si/SiO_2 interface in n-FinFET. The analysis is done for n-type FET hence a negatively charged trap is placed at the Si/SiO_2 interfaces to simulate the altered drain current [9]. Simulation is carried out for different trap positions (at mid-channel at the top, front and back gates). The channel sidewall interface with gate oxide for all three shorted gates (front, back and top) is divided into different horizontal regions (from source to drain), denoted by A, B and C regions, respectively, as shown in Fig. 3*a*. It is used to analyse SCT effect at different SiO_2/Si interfaces of the Fin under the gate. The trap can be seen at the SiO_2/Si interface by the observed total-interface charges in the channel as shown in Fig. 3*a* for proposed SDS-FinFET.

The origin of SCT induced noise is the alternate capture and emission of charge carriers at discrete trap levels near the Si/SiO_2 interface which changes the electron density as shown in Figs. 3*b* and *c*. On the other hand, a charged trap state has an influence on the local mobility near its position due to coulomb scattering. Hence, SCT also affects the coulomb scattering, which degrades the carrier mobility. Therefore, SCT reduces the performance of the design which makes circuit unstable and reduces the ON current as shown in Fig. 3*d*.

The change in ON current due to SCT can be presented by the error in the current. SCT induced error amplitude increases

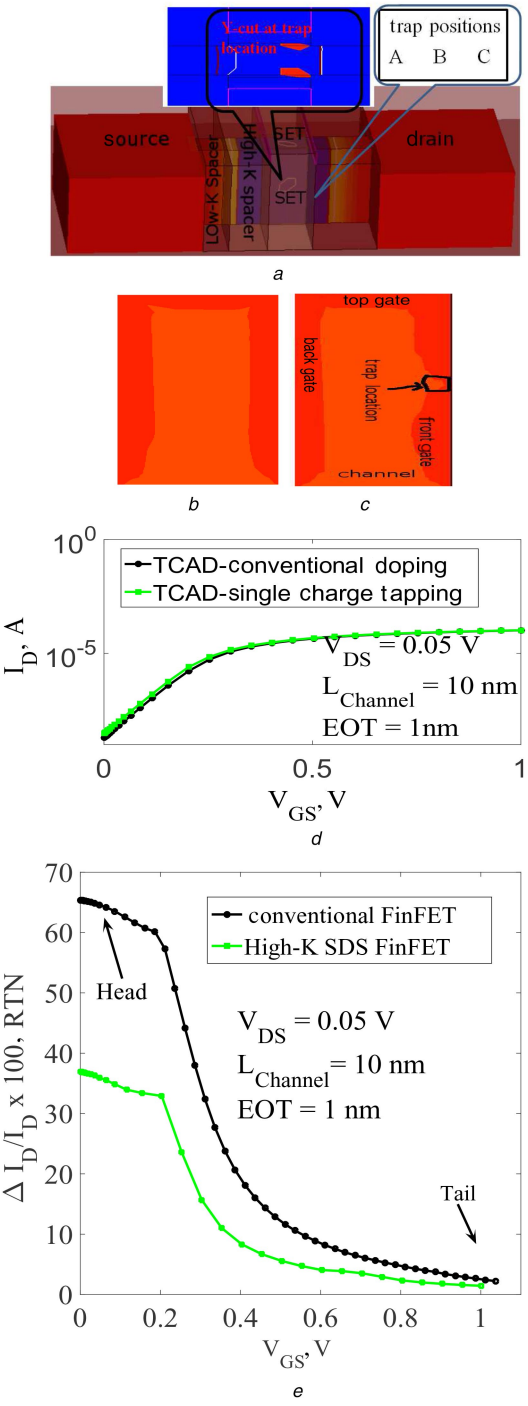


Fig. 3 *Comparative SCT analysis for proposed SDS-FinFET*
a Trap charge concentration at $Si–SiO_2$ interface
b electron current density without
c and with SCT
d Variation in drain current under SCT
e SCT induced error amplitude for SDS and standard FinFET

Table 1 Device parameters of proposed device as per ITRS 2015 [15]

S. no.	Device parameter	ITRS projection value
1	physical gate length, L_G	10 nm
2	equation oxide thickness, EOT	1 nm
3	fin thickness, T_{si}	6 nm
4	supply voltage, V_{DD}	1 V
5	channel doping, N_A	10^{15} cm^{-3}
6	source/drain doping, N_D	2.7×10^{20} cm^{-3}

with reduced screening effect at lower V_{GS}. Therefore, the error is modelled as follows [19]:

$$\frac{\Delta I_D}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_T}\Delta V_T \quad (1)$$

The SCT induced error amplitude is proportional to the change in the trap induced threshold voltage (V_T) and it is inversely proposal to the sub-threshold slope. The error amplitude in the sub-threshold

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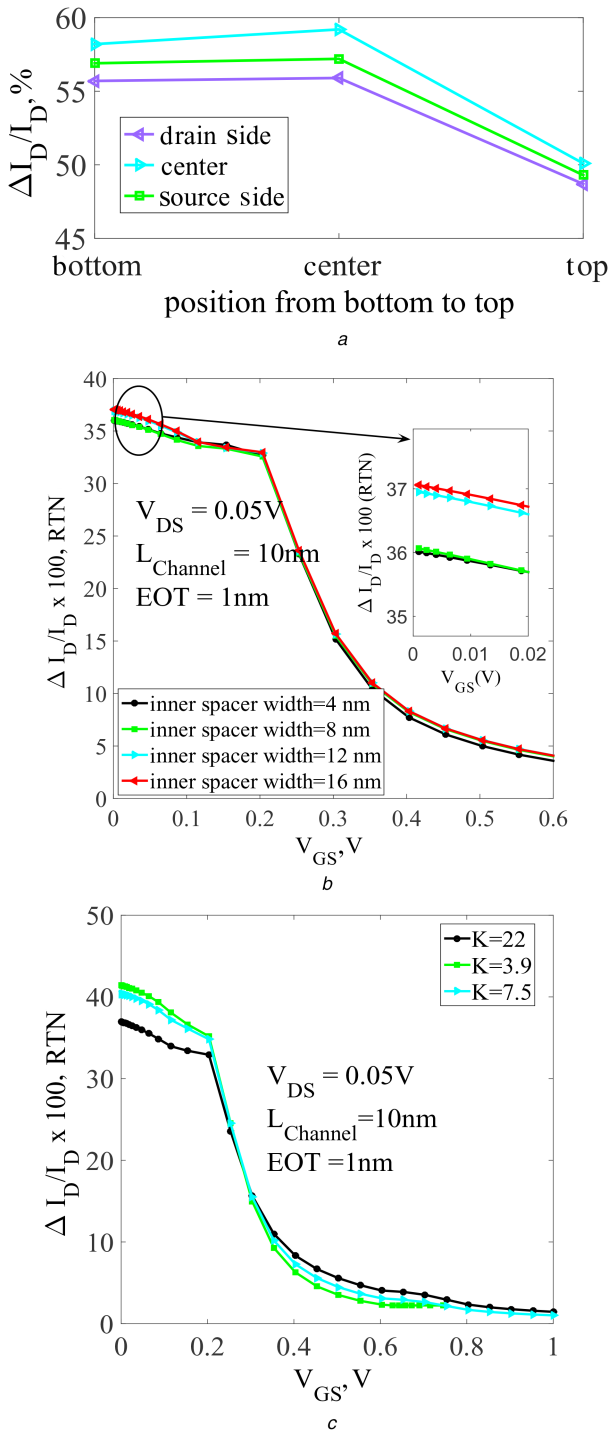


Fig. 4 *SCT induced error analysis for proposed SDS-FinFET*
a SCT induced error amplitude for trap locations across 3D FinFET sidewall interface
b SCT induced error amplitude for spacer width
c SCT induced error amplitude for different inner spacer materials

mode of operation ($V_{DS} = 0.05$ V) for different gate voltage is shown in Fig. 3*e*. As all the gates are shorted for the proposed device (SDS-FinFET) hence, we did SCT analysis for all gates. For the validation of the simulation results, we compared the simulation results with conventional SOI FinFET [19, 20]. The SDS-FinFET shows reduce error amplitude than conventional FinFET and decrease with increased V_{GS}. After observation of the simulation results reveal that SCT induced error amplitude decreases for SDS-FinFET, because, electric field induced by trap charges is reduced by the means of the inner high-k spacer.

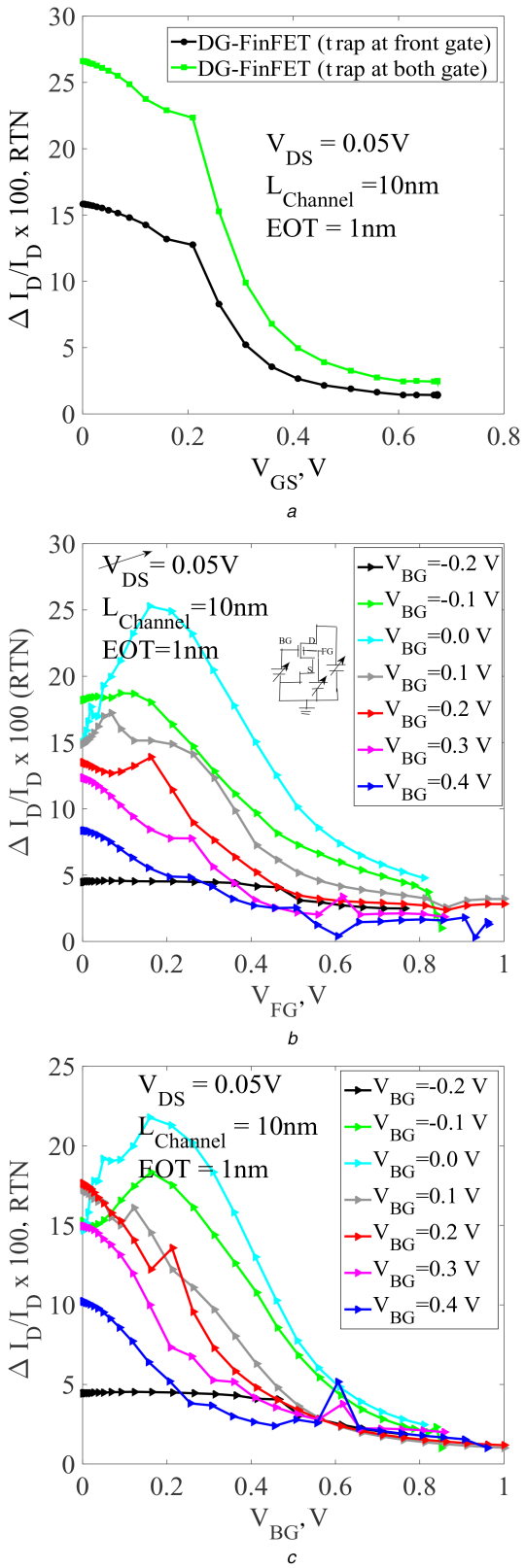


Fig. 5 *SCT induced error analysis for front and back biasing*
a SCT induced error amplitude for DG-FinFET
b Front gate (V_{FG}) and
c Back-gate (V_{BG}) biasing for independent-gate mode

Introduction of an inner low-k spacer reduces barrier at G/S and G/D underlap due to trapped charges. Therefore, inner low-k spacer also helps to reduce the field effect. The outer high-k spacer is used to improve the performance of the device.

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Fig. 4*a* shows the SCT induced error amplitude for SCT at different Fin regions (at SiO_2/Si interfaces). Similar to bulk MOSFET, the significant SCT effect is found in the trap located near the middle region between the source and drain (region B), and the SCT induced error amplitude decreases toward the source/drain (regions A and C). The trap situated near the bottom of the sidewall interface is very close to the path with high sub-threshold current, due to the fringing drain field sensitivity through buried oxide in the lightly doped (Fin) channel.

The top gate has very less control over the channel due to horizontal and vertical electric fields which shows the minimum effect of SCT. Previous studies also show very smaller SCT effects on FinFET than MOSFET. Further, we analysed the impact of the spacer width on SCT induced error amplitude so that we can give solution for stability and SCT tolerant FinFET device. Fig. 4*b* shows the SCT induced error amplitude for different spacer widths (from 4 to 16 nm). SDS-FinFET shows minimum error amplitude at 12 nm spacer width, i.e. it has a maximum tolerant at this spacer width, whereas error amplitude increases below and above of 12 nm space width. Further, error amplitude is also analysed for different spacer materials.

Different insulator materials show varying charge carrying capacity due to their permittivity. We have used HfO_2 as the high-k dielectric for outer spacer having the permittivity of $K = 25$. We have done SCT analysis for low-k and high-k spacers materials. Fig. 4*c* shows the SCT induced error amplitude for different spacer materials and it shows that high-k spacer material reduces the error amplitude than low-K inner spacer insulators (SiO_2, Si_3N_4) because high-k insulators reduce the fringing electric field effectively than low-k insulators.

Further, the SCT analysis is done for the individual double FinFET (DG-FinFET). In this order, Fig. 5*a* shows the SCT induced error amplitude on front-gate voltage (V_{FG}) with a single trap placed at the centre of the front-gate. It is demonstrated that the SCT induced error amplitude is significantly smaller than SCT at both the gates. While operating in an independent-gate mode, the current-conduction path can be modulated by back-gate voltage (V_{BG}). As the conduction path shifts closer to the charged trap, more conducting carriers are affected by the perturbed potential, thus resulting in larger error amplitude. It is observed that negative (or positive) V_{BG} exhibits a larger error amplitude for the trap located at the centre of the front-gate (or back-gate) interface. The modulation of the current-conducting path by V_{BG} has also resulted in the opposite dependence of error on V_{BG} (trapping at both gates) as shown in Fig. 5*b*. For the trap located at the front-gate interface, smaller back-gate (V_{BG}) bias exhibits higher impact, whereas the opposite trend is observed for the trap placed at the back-gate interface. It is also noticed that the V_{FG} increases to a moderate value, more carriers are generated at the front gate to screen the influence of the charged trap, and the error amplitude starts to decrease as shown in Fig. 5*c*.

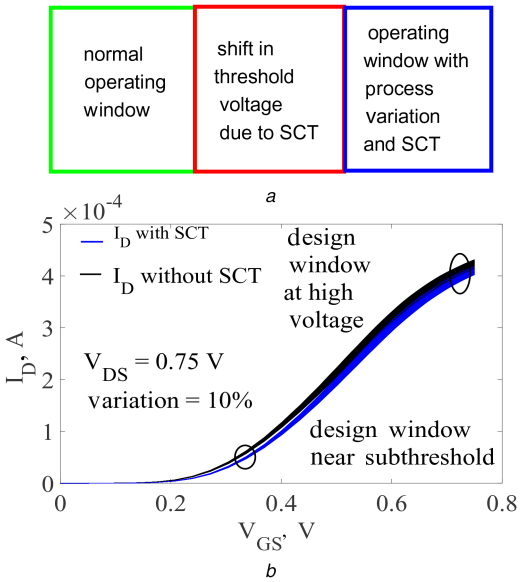


Fig. 6 *Design window analysis under PV and SCT*
a Circuit design window under considering PVs
b Variation in ON current due to PV with and without SCT

4. PV analysis:: The PV sources increase with the continued scaling of the semiconductor devices. The PV-aware integrated circuit design is a prime requirement for the sophisticated defence and space applications. PV changes the functionality of the most sensitive circuits such as SRAMs and sense amplifiers which are designed to be stable, reliable and symmetric circuits. Hence, to

Table 2 Design window under PV and SCT

S. no.	Device Parameter	Calculated value
1	minimum I_D	1.94×10^{-8}
2	maximum I_D	4.3×10^{-4}
3	minimum I_D with SCT	1.3×10^{-8}
4	maximum I_D with SCT	4.2×10^{-4}

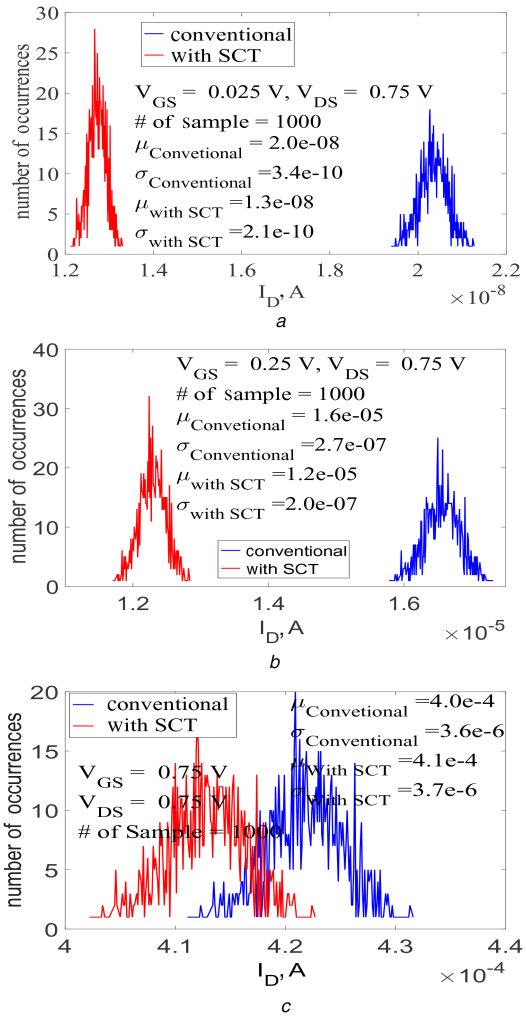


Fig. 7 *Gaussian distribution curves using 1000 Monte Carlo simulation for ON current under ±10% PV. Curves showing the deviation in ON current due to PV with and without SCT*

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understand the stability and reliability under process dependent parameter variation is crucial to find the design window available for sophisticated circuits design.

First, we introduce the $\pm 10\%$ PV effect into the device dimensions and measure the variation in ON current. The measured ON current under SCT along with PV is shown in Fig. 6*b*. The result shows the wide window for ON current due to PV whereas SCT gives periodic variation in I_{ON} (like inter-die). Hence scale device required wide circuit design window. As per the analysis, the probabilistic design window for the FinFET under the PV and SCT is shown in Fig. 6*a*. As the I_{ON} of the device shifted due to SCT, hence, the mean value of the designer window also shifts as shown in Fig. 6*b*. Based on calculated parameter the designer values for design window is shown in Table 2 so that the circuit can be worked in the sub-threshold/normal mode of operations. We determined the statical ON-current value using 1000 MC simulation for stable circuit design under SCT and PV. The calculated mean value and standard deviation under PV at the different drain and gate voltages are shown in Fig. 7. It is seen that the PV effect degrades with SCT under different voltages. As mean (μ) and standard deviation (δ) degraded under SCT, hence the PV effect decreases but performance also degraded. When designing considers both PV and SCT together, then the design window becomes wider than nominal.

5. Conclusion: We have proposed novel high-performance FinFET module using dual high-k gate insulators and dual-k symmetric spacers. A dual layer gate insulator has been proposed to reduce the dangling bond which reduces gate leakage current, bias temporal instability, and hot-carrier injection. We also investigated the impacts of SCT induced error amplitude on shorted and individual-gate high-k symmetric spacer-based FinFETs. SCT changes with varying spacer width (up/down) and maximum SCT induced effects have been observed at 12 nm inner high-k spacer width for proposed device. The SCT effect on IG-FinFET has been analysed for different front and back-gate voltages. Further, the PV along with SCT analysis has been done and a probabilistic design window using MC simulation has been proposed for proposed device. The proposed design window under SCT and PV analysis will be useful for modern reliable chip designs for defence and space applications.

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