Design structure of tunnel FET by combining thermionic emission with tunneling phenomenon

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This study proposes a novel electrically doped tunnel field effect transistor (ED-TFET), which combines thermionic emission and band to band tunnelling by using an additional metal source (MS) of appropriate work function (WF; 3.9 eV) by forming an ohmic junction between metal and silicon. The ohmic junction is created below the channel region near the source channel junction by depositing of appropriate workfunction metal (lower than silicon) which injects extra electrons through over the barrier along with band to band tunneling (BTBT) in the channel of the device. Therefore, a drastic improvement in the ON state current is observed which is numerically about 107 times greater than conventional ED-TFET. Furthermore, the radiofrequency figures of merit such cut-off frequency, gain band width product, and maximum oscillating frequency are enhanced by $\sim 10^6$, 20 and 1000 times, respectively, however, intrinsic gain and transconductance generation factor have nearly 66.66 and 14.28% improvement compared to conventional ED-TFET. Furthermore, the concepts of drain underlapping and dual metal gate have been used to checkout OFF-state current and negative conductance as a final proposal. In addition, this study has also investigated the performance variations in the proposed structure due to the WF change of CG2, length of L_{D1} and position of MS.

1. Introduction: Increased functionality, reduction in cost per unit chip-area, lower power consumption and higher radiofrequency (RF) performance are some of the advantages of scaling metal oxide semiconductor field effect transistors (MOSFETs) [1]. The dimensions of Si MOSFET have been downscaled by three orders of magnitude in the last few decades using the scaling guidelines proposed by Dennard *et al.* in the early 1970s [2]. However, it has been observed that as MOSFET enters into the nanometre range it suffers from numerous disadvantages such as high leakage current, various short channel effects, and large parameter variations [3, 4]. In the process of scaling, the supply voltage is also scaled down which leads to the decrease in V_{th} and causes a rise in the leakage current [5]; these concerns impose a limit on the scaling of MOSFETs. According to the International Technology Roadmap for Semiconductors road map tunnel field effect transistors (TFETs) are an excellent replacement for MOSFET in low-power applications as the carrier injection from source to channel is through quantum mechanical tunnelling [6, 7]. In addition, for improving the TFETs performance several ideas have been given by researchers such as the usage of high-K dielectric [8], dual drain electrode [9], optimised doping of source region [10], strain engineering [11], gate-metal work function engineering [8], insertion of metal strip near the source/channel region [12], band gap engineering at source side [13], n+ doped pocket insertion at source/channel interface in physically doped TFET [14] and many others. Conventional physically doped TFETs also face difficulty in maintaining abrupt tunnelling junctions due to the diffusion of dopant atoms, known as random dopant fluctuations (RDFs). RDFs have adverse effects on the TFET performance such as the variation in threshold voltage, drain-induced current enhancement and degraded subthreshold swing (SS) [15, 16]. In order to resolve these issues, concepts of electrical doping [17, 18] and junctionless TFET have been proposed [19, 20]. Though junctionless TFET has higher ON state current and lower threshold voltage, but it still retains issues of physical doping (fabrication complexity) and costly thermal annealing techniques. Thus electrically doped TFET (ED-TFET) is used to resolve the issues arising from physically doped and junctionless TFET.

The Letter proposes an electrically doped metal source TFET (ED-MS-TFET), which has improved DC parameters and high-frequency performance as compared to ED-TFET by depositing a layer of the MS of appropriate work function (WF) below channel within the dielectric box. The introduction of MS in the channel region drastically improves the I_{ON} due to the excess electrons provided by the MS in the vertical direction. The excess carriers coming through ohmic junction get merged with horizontally tunnel electrons provided by the source and behave as a supplement for improving device performance. The proposed concept enhances the DC and RF parameters up to the unmatched level as compared to the conventional one. Furthermore, drain underlapping and gate WF engineering are used to suppress the ambipolarity and leakage current, respectively by preserving improved DC/RF FOMs in dual metal gate ED-MS-TFET (DMG-ED-MS-TFET). The techniques of atomic layer deposition such as chemical vapour deposition or phase vapour deposition can be used to deposit the thin layers of SiO_2, HfO_2 and MS [21, 22]. MS can be fabricated by molybdenum (Mo) as the WF of Mo can be tuned up to 3.9 eV and below by high dose of nitrogen implantation and maintaining the dopant atom concentration 6×10^{15} atoms/cm^2 with 80 keV implantation energy for annealing conditions at 700°C for 15 min [23]. The organisation of the Letter is as follows – Section 2 is a description of the device and its simulation. Section 3 presents the DC and RF characteristics of the proposed device in a comparative manner. While Section 4 describes the optimisation of various parameters and finally Section 5 has the findings of the research summed up as a conclusion.

2. Device description and simulation setup: The cross-sectional view of ED-TFET, ED-MS-TFET, and DMG-ED-MS-TFET can be seen in Figs. 1*a*–c. In ED-MS-TFET and DMG-ED-MS-TFET, drain and source regions are developed by applying 1.2 V and −1.2 V to form n+ and p+ regions, respectively. Mid band gap material nickel silicide (NiSi) is used with 0.45 eV barrier height for drain and source contacts. The metal electrodes are deposited over a thin layer of HfO_2, which acts as a barrier to prevent the formation of silicide between metal and silicon. The additional metal

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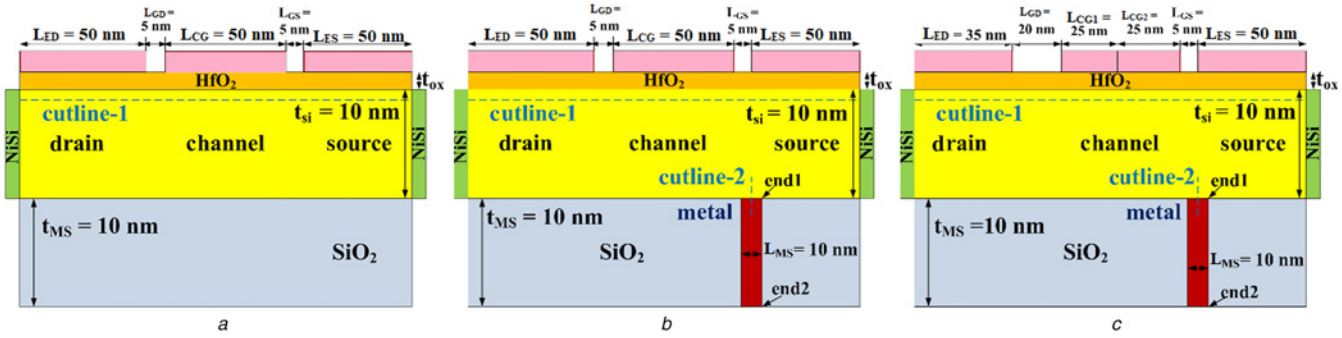

Fig. 1 *Device structure of*
a ED-TFET
b ED-MS-TFET
c DMG-ED-MS-TFET

source (MS) is deposited below the silicon layer near the source/channel junction. Thickness and length of MS is 10 nm. For all the devices the substrate doping concentration is 10^{15} cm^{-3}, silicon body thickness is 10 nm and oxide thickness is 2 nm. For ED-TFET and ED-MS-TFET length of the drain (L_{D1}) is 50 nm and work function for the drain (ϕ_{D1}), source (ϕ_{S1}) and the gate electrode (ϕ_{GE}) is 4.5 eV with spacer lengths L_{DG} and L_{GS} equal to 5 nm. Lengths of the gate electrode (L_{GE}) and source L_{S1} are both equal to 50 nm. The WF of the additional MS (ϕ_m) is 3.9 eV. For DMG-ED-MS-TFET, L_{D1} is 35 nm as the technique of drain underlapping is used. Its gate electrode is made of two metals. ϕ_{GE2} is equal to 5.2 eV and ϕ_{GE1} is equal to 4.5 eV with spacer length L_{DG} equal to 20 nm, L_{GE1} and L_{GE2} equal to 25 nm. The device has been simulated using a two-dimensional ATLAS device simulator [24]. The models employed to carry out the simulation process are – Shockley Read Hall recombination model, Auger recombination model, Fermi–Dirac statistical model, Universal Schottky model and non-local band to band tunnelling model.

3. Results and discussion

3.1. DC characteristics: As reported in [25, 26], for a physically doped conventional TFET, the OFF state current is in femto amperes and ON state current is in nano amperes when the applied V_{GS} and V_{DS} are 2 V. In this Letter, the ED-TFET is calibrated at the same dimensions and biasing values and similar carrier concentration is achieved by electrical doping in source and drain regions presented in Fig. 2*a* as reported in [26]. Furthermore, the transfer characteristics of the calibrated device are shown in Fig. 2*b*, which reflects almost the same ON but lower OFF current due to the electrical doping. These results validate the used models and simulating parameters.

Fig. 3*a* shows an almost similar electric field for all the three devices near the source/channel junction. This is supported by the ON state energy band diagram as shown in Fig. 3*b*; where tunnelling width at source/channel junction is approximately the same which means the tunnelling probability is the same for all. As

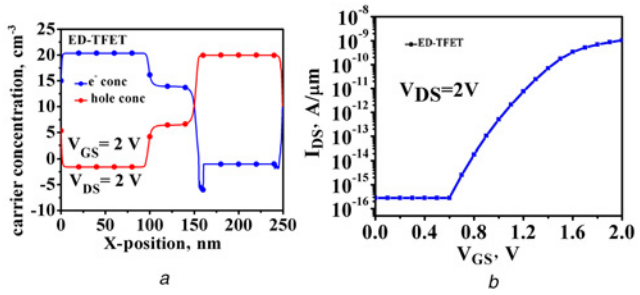

Fig. 2 *Variation in*
a Carrier concentration as a function of the length
b Transfer characteristics of the calibrated device with gate voltage

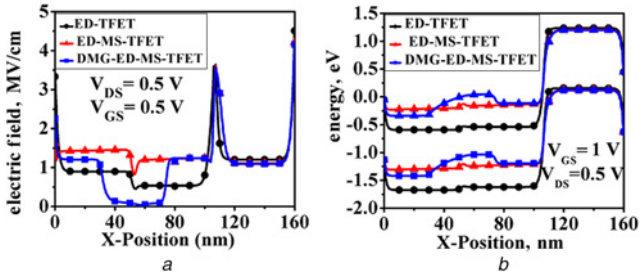

Fig. 3 *Variation of*
a Electric field in the ON state
b Energy band diagram as a function of length in the ON state

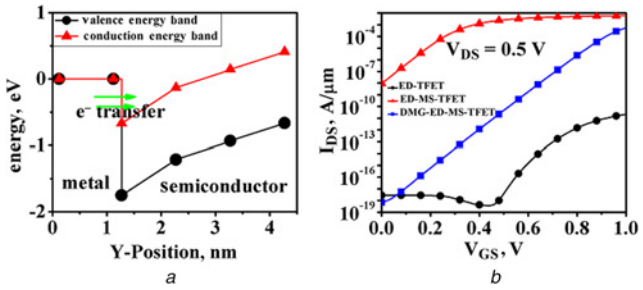

Fig. 4 *Variation in*
a Energy band diagram of ED-MS-TFET along cutline-2
b Drain current of all three devices in ON state

depicted in Fig. 4*a*, there is a transfer of excess electrons from the MS into the silicon body in the vertical direction. The ohmic junction formed by MS by choosing a proper WF metal, which supplies additional carriers in the channel and leads to increment in the ON state current as shown in Fig. 4*b*, while the ON state current of both the devices is significantly higher than ED-TFET. Ambipolar current in the TFET is suppressed by employing the concept of drain underlapping; Fig. 5*a* shows the energy band diagram of the three devices in the ambipolar state. The tunnelling width of DMG-ED-MS-TFET is higher than the other two, indicating a decreased probability of tunnelling at the drain/channel region and thus helps in suppressing the negative conductance. Fig. 5*c* shows the variation in drain current for negative V_{GS} and suppressed ambipolar current is found for DMG-ED-MS-TFET. Fig. 5*b* shows the energy band distribution (EBD) under OFF state; a quantum well structure of EBD is formed due to the dual WF gate electrode; this creates an obstacle for leaky carriers coming from the p+ source and MS in OFF state. This becomes a clear reason for the reduction of leakage in DMG-ED-MS-TFET as shown in Fig. 5*c*. Furthermore, V_{th} and SS of the devices have been numerically calculated by the transconductance derivate approach [27] and

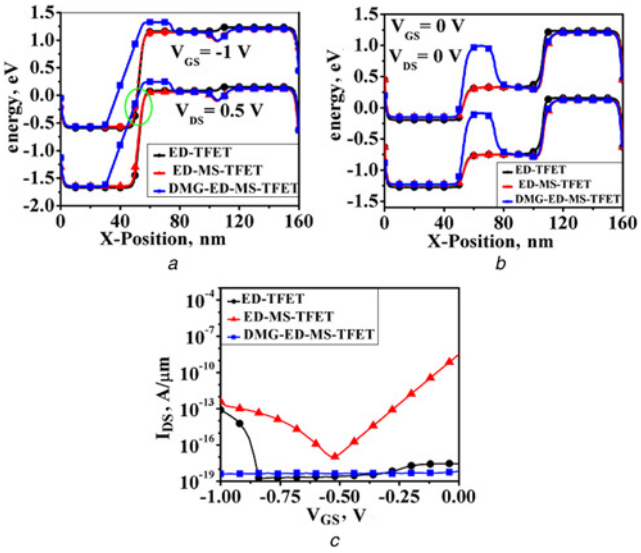

Fig. 5 *Distribution of*
a Energy bands in ambipolar state
b Energy bands in OFF state
c Drain current in the ambipolar state

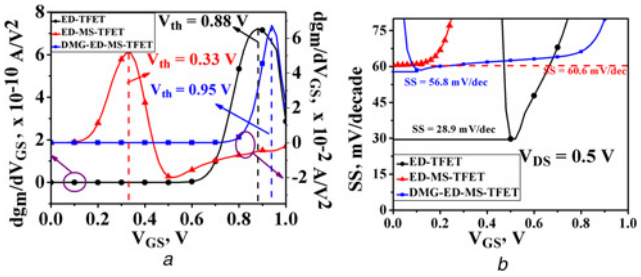

Fig. 6 *Variation in*
a First derivative of g_m
b SS with V_{GS}

Table 1 DC characteristics of devices

Parameters name/ unit	ED-TFET	ED-MS-TFET	DMG-ED-MS-TFET
ON current, A/μm	7.3×10^{-11}	1.7×10^{-3}	7.4×10^{-4}
OFF current, A/μm	3.1×10^{-18}	2.7×10^{-9}	1.5×10^{-18}
V_{th}, V	0.88	0.33	0.95
SS, mV/dec	28.9	60.6	56.8
ambipolar current, A/μm	9.3×10^{-14}	1.8×10^{-13}	4.6×10^{-19}

reported method [28], respectively. Fig. 6*a* shows the variation of the transconductance derivative of ED-TFET, ED-MS-TFET, and DMG-ED-MS-TFET, respectively. Fig. 6*b* depicts a minimum point SS of all three structures in which ED-MS-TFET and DMG-ED-MS-TFET have higher SS because of thermionic emission. Now the values of V_{th} and SS given in Table 1 can be validated from the same figure.

3.2. RF/analogue analysis: RF analysis is crucial in the current scenario due to the need for devices to operate at high frequency and low power. The parameters for interpreting RF FOMs are transconductance (g_m), gate-to-drain capacitance (C_{gd}), gate-to-source

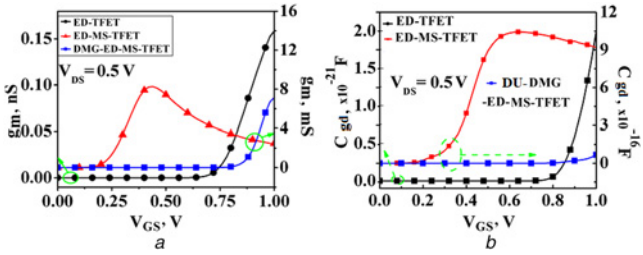

Fig. 7 *Variation in*
a g_m with V_{GS}
b C_{gd} with V_{GS}

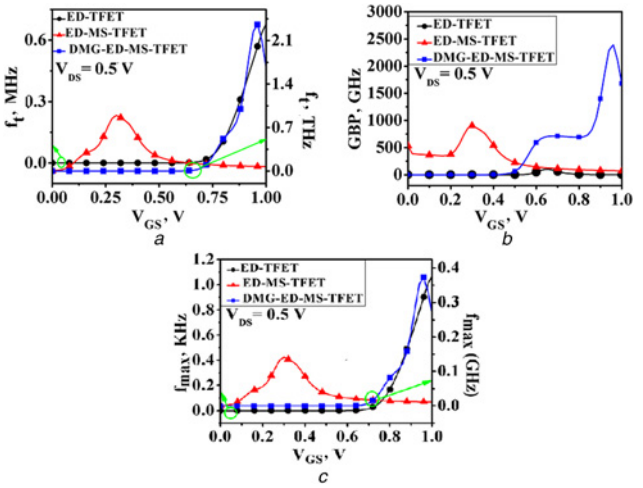

Fig. 8 *Variation of*
a f_t
b GBP
c f_{max} with V_{GS}

capacitance (C_{gs}), cut-off frequency (f_t), gain bandwidth product (GBP), intrinsic gain (IG), maximum oscillating frequency (f_{max}) and transconductance generation factor (TGF). Transconductance is the ability to transform V_{GS} into the drain current (I_{DS}). The transconductance is higher for both ED-MS-TFET and DMG-ED-MS-TFET as compared to ED-TFET as shown in Fig. 7*a* due to the presence of an additional MS in these devices. The accurate analysis of C_{gd} or Miller capacitance is very important for designing high-frequency circuits because C_{gd} behaves as a parasitic capacitance for lower values of V_{GS}, but for higher values of V_{GS}, it behaves as inversion capacitance ($C_{gd,inv}$) [29]. The switching speed of TFET is improved when both of these values are low. The C_{gd} of the devices is plotted as shown in Fig. 7*b*, here, DMG-ED-MS-TFET has C_{gd} in the order of fF. However, it comparatively has a greater C_{gd} than ED-TFET due to the MS and lower capacitance as compared to ED-MS-TFET caused by a dual metal gate and drain underlapping. Cut-off frequency (f_t) is defined as the frequency at which the short circuit current gain in the common source configuration becomes unity [24]. Fig. 8*a* shows the variation of cut-off frequency with V_{GS}. f_t increases with an increase in g_m and then decreases due to the increase in C_{gd}. DMG-ED-MS-TFET and ED-MS-TFET both have a higher cut-off frequency than ED-TFET. Also, DMG-ED-MS-TFET has more cut-off frequency than ED-MS-TFET indicating that the device is suitable for low-power applications over a wide range of frequencies. Fig. 8*b* shows the GBP of the three devices. GBP is an indication of the trade-off between gain and bandwidth of a device and follows the same trend as f_t. The proposed device has a high GBP showing that

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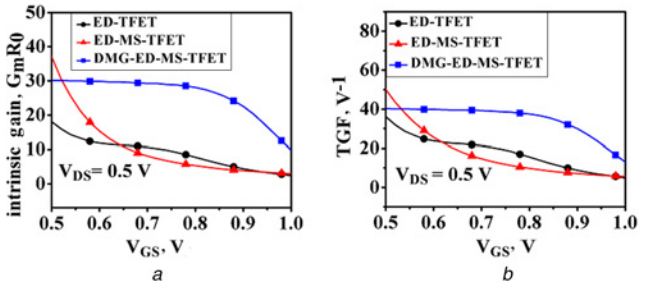

Fig. 9 *Variation of*
a IG
b TGF with V_{GS}

the device can maintain an optimum gain as well as bandwidth. f_{max} is the frequency at which the power gain of the device is unity. It is influenced by g_m, C_{gd} and C_{gs}. It rises with V_{GS} and after attaining a peak, it falls. The f_{max} of DMG-ED-MS-TFET is higher than the other two devices as shown in Fig. 8*c*. IG is the product of transconductance and output resistance R_o. R_o is very high in the subthreshold region and drops under the influence of BTBT after exceeding V_{th}. Since R_o is the dominating factor, IG falls with V_{GS} as depicted in Fig. 9*a*. TGF is a measure of the device efficiency in converting a DC parameter into an AC parameter. It shows how effectively a device optimises drain current for efficient amplification with low power dissipation [30]. Drain current is negligible under the subthreshold region so the TGF is plotted for values over 0.5 V. Both ED-MS-TFET and DMG-ED-MS-TFET have higher TGF values as compared to conventional ED-TFET near the threshold voltage as shown in Fig. 9*b*. Further increase in voltage causes a drop in TGF due to the drain current acting as the dominating factor.

4. Optimisation: The proposed device uses the concepts of drain underlapping, dual metal gate engineering and the introduction of additional MS for improved performance. Hence, the optimised values for drain length (L_{D1}), WF of controlgate2 (ϕ_{GE2}) and position of MS are needed to be analysed. Fig. 10*a* shows the variation of I_{DS} for different drain lengths, when drain length goes below 45 nm it is significant for suppression of ambipolarity without degradation in ON current. The shorter length of the drain electrode is also beneficial for high-frequency applications as can be seen in Fig. 10*b*; shorter the L_{D1} better the RF performance. Moreover, WF variation of CG2 also affects the ON-, OFF-state and RF performance of the proposed device.

Fig. 11*a* shows the WF of CG2 goes below 5.2 eV OFF state current starts increasing and the same trend is followed by ON current also. Similarly lower WF of CG2 causes an increment in RF performance as can be visualised from Fig. 11*b* in terms of cut-off frequency. The position of the MS needs to be optimised for better electronic characteristics. As depicted in Fig. 12*a* and *b*, I_{DS} and f_t are high when the metal is placed near the source/

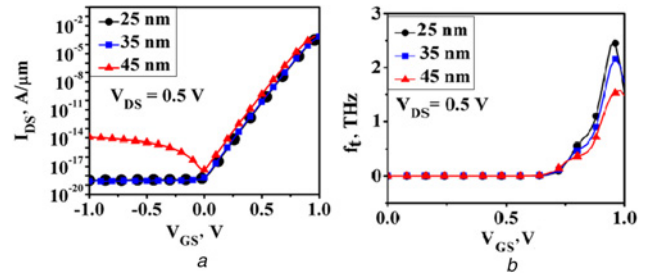

Fig. 10 *Variation of*
a I_{DS}
b f_t for different drain length

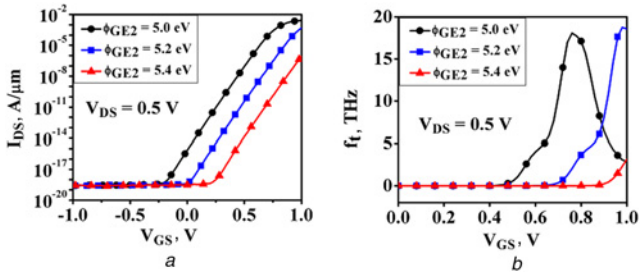

Fig. 11 *Variation of*
a I_{DS}
b f_t with various f_{GE2}

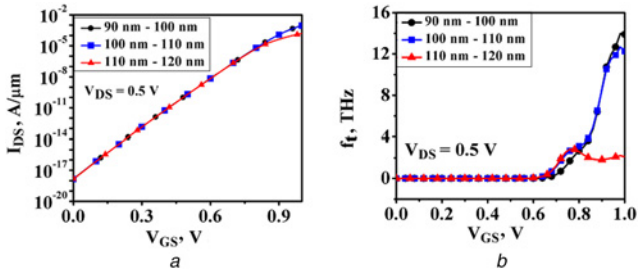

Fig. 12 *Variation of*
a I_{DS}
b f_t with the position of MS

channel junction, but as it moves away from the source/channel junction both of them starts degrading, in which RF performance is more affected.

5. Conclusion: Conventional ED-TFET suffers from the disadvantages of poor DC and RF parameters and ambipolarity. To resolve these issues, the Letter proposes a new device, ED-MS-TFET, which combines thermionic emission and band-to-band tunnelling by using a MS near the source/channel junction. ED-MS-TFET has better DC and high-frequency analysis due to the injection of excess electrons from the MS. However, the device possess OFF state current near to MOSFET and the issue of negative conductance remains untouched. In this concern, DMG-ED-MS-TFET possesses drain underlapping and DMG, where drain underlapping is used to suppress the ambipolarity by widening the tunnelling width at the drain channel junction. DMG is incorporated to reduce leakage current by using higher WF at the drain/channel junction side. This forms a quantum well for the leaky electrons and prevents the movement of electrons coming from ohmic junction in OFF state. Finally, DC and RF analysis of the devices show that the performance of DMG-ED-MS-TFET in terms of GBP, C_{gd}, f_t, f_{max} and TGF is much better than ED-TFET.

6 References

[1] Mohankumar N., Syamal B., Sarkar C.K.: 'Influence of channel and gate engineering on the analog and RF performance of DG MOSFETs', *IEEE Trans. Electron Devices*, 2010, **57**, (4), pp. 820–826

[2] Dennard R.H., Gaensslen F.H., Yu H.-N., *ET AL.*: 'Design of ion-implanted MOSFET's with very small physical dimensions', *IEEE Solid-State Circuits Soc. Newsl.*, 2007, **12**, (1), pp. 38–50

[3] Bangsaruntip S., Cohen G.M., Majumdar A., *ET AL.*: 'Universality of short-channel effects in undoped-body silicon nanowire MOSFETs', *IEEE Electron Device Lett.*, 2010, **31**, (9), pp. 903–905, doi: 10.1109/LED.2010.2052231

[4] Chopra S., Subramaniam S.: 'A review on challenges for MOSFET scaling', *Int. J. Innov. Sci., Eng. Technol.*, 2015, **2**, (4), pp. 1055–1057

[5] Kumar M.: 'Effects of scaling on MOS device performance', *IOSR J. VLSI Signal Process.*, 2015, **5**, (1), pp. 25–28, doi: 10.9790/4200-05132528
[6] 'International Technology Roadmap for semiconductors (ITRS)'. Available at http://www.itrs2.net
[7] Ionescu A.M., Riel H.: 'Tunnel field-effect transistors as energy-efficient electronic switches', *Nature*, 2011, **479**, (7373), pp. 329–337, doi: 10.1038/nature10679
[8] Yadav S., Sharma D., Soni D., *ET AL.*: 'Controlling of ambipolarity with improved RF performance by drain/gate workfunction engineering and using high-k dielectric material in electrically doped TFET: proposal and optimization', *J. Comput. Electron.*, 2017, **16**, pp. 721–731
[9] Raad B.R., Nigam K., Sharma D., *ET AL.*: 'Performance investigation of bandgap, gate material work function and gate dielectric engineered TFET with device reliability improvement', *Superlattices Microstruct.*, 2016, **94**, (138), pp. 138–146
[10] Min J., Wu J., Taur Y.: 'Analysis of source doping effect in tunnel FETs with staggered bandgap', *IEEE Electron Device Lett.*, 2015, **36**, (10), pp. 1094–1096
[11] Boucart K., Riess W., Ionescu A.M.: 'Lateral strain profile as key technology booster for all-silicon tunnel FETs', *IEEE Electron Device Lett.*, 2009, **30**, (6), pp. 656–658
[12] Raad B.R., Tirkey S., Sharma D., *ET AL.*: 'A New design approach of dopingless tunnel FET for enhancement of device characteristics', *IEEE Trans. Electron Devices*, 2017, **64**, (4), pp. 1830–1836
[13] Salehi M.R., Abiri E., Hosseini S.E., *ET AL.*: 'Analysis and optimization of tunnel FET with band gap engineering'. 21 Iranian Conf. on Electrical Engineering (ICEE), Mashhad, 2013, pp. 1–4
[14] Abdi D.B., Kumar M.J.: 'In-built N+ pocket p-n-p-n tunnel field-effect transistor', *IEEE Electron Device Lett.*, 2014, **35**, (12), pp. 1170–1172
[15] Damrongplasit N., Shin C., Kim S.H., *ET AL.*: 'Study of random dopant fluctuation effects in germanium-source tunnel FETs', *IEEE Trans. Electron Devices*, 2011, **58**, (10), pp. 3541–3548
[16] Jang J.-S., Lee H.K., Choi W.Y.: 'Random dopant fluctuation effects of tunneling field-effect transistors (TFETs)', *J. Inst. Electron. Inf. Eng.*, 2012, **49**, (12), pp. 179–183
[17] Lahgere A., Sahu C., Singh J.: 'Electrically doped dynamically configurable field-effect transistor for low-power and high-performance applications', *Electron. Lett.*, 2015, **51**, (16), pp. 1284–1286
[18] Kumar M., Jit S.: 'Effects of electrostatically doped source/drain and ferroelectric gate oxide on subthreshold swing and impact ionization rate of strained-Si-on-insulator tunnel field-effect transistors', *IEEE Trans. Nanotechnol.*, 2015, **14**, (4), pp. 597–599
[19] Ghosh B., Akram M.W.: 'Junctionless tunnel field effect transistor', *IEEE Electron Device Lett.*, 2013, **34**, (5), pp. 584–586
[20] Nigam K., Kondekar P., Sharma D., *ET AL.*: 'A new approach for design and investigation of junction-less tunnel FET using electrically doped mechanism', *Superlattices Microstruct.*, 2016, **98**, pp. 1–7
[21] Putkonen M., Bosund B., Oili M.E., *ET AL.*: 'Thermal and plasma enhanced atomic layer deposition of SiO2 using commercial silicon precursors', *Thin Solid Films*, 2014, **558**, pp. 93–98
[22] Niinistö J., Putkonen M., Niinistö L., *ET AL.*: 'Atomic layer deposition of HfO_2 thin films exploiting novel cyclopentadienyl precursors at high temperatures', *Chem. Mater.*, 2007, **19**, (13), pp. 3319–3324
[23] Ranade P., Takeuchi H., King T.-K., *ET AL.*: 'Work function engineering of molybdenum gate electrodes by nitrogen implantation', *Electrochem. Solid-State Lett.*, 2001, **4**, (11), pp. G85–D87
[24] 'ATLAS device simulation software', Silvaco Inc., Santa Clara, CA, USA, 2014
[25] Boucart K., Ionescu A.M.: 'Double-gate tunnel FET with high-k gate dielectric', *IEEE Trans. Electron Devices*, 2007, **54**, (7), pp. 1725–1733, doi: 10.1109/TED.2007.899389
[26] Wang P.F., Hilsenbeck K., Nirschl T., *ET AL.*: 'Complementary tunneling transistor for low power application', *Solid State Electron.*, 2004, **48**, (12), pp. 2281–2286, doi: 10.1016/j.sse.2004.04.006
[27] Siebel O.F., Schneider M.C., Galup-Montoro C.: 'MOSFET threshold voltage: definition, extraction, and some applications', *Microelectron. J.*, vol. **43**, no. 5, pp. 329–336, 2012
[28] Pahwa G., Dutta T., Agarwal A., *ET AL.*: 'Analysis and compact modeling of negative capacitance transistor with high ON-current and negative output differential resistance part II: model validation', *IEEE Trans. Electron Devices*, 2017, **63**, (12), pp. 4986–4992
[29] Yang Y., Tong X., Yang L.-T., *ET AL.*: 'Tunneling field-effect transistor: capacitance components and modeling', *IEEE Electron Device Lett.*, 2010, **31**, (7), pp. 752–754
[30] Madan J., Chaujar R.: 'Interfacial charge analysis of heterogeneous gate dielectric-gate all around-tunnel FET for improved device reliability', *IEEE Trans. Device Mater. Reliab.*, 2016, **16**, (2), pp. 227–234