Deep insights into electrical parameters due to metal gate WFV for different gate oxide thickness in Si step FinFET

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Published in Micro & Nano Letters; Received on 24th May 2018; Revised on 28th October 2018; Accepted on 7th December 2018

A systematic investigation of the impact of Ti metal gate work function variability (WFV) on various electrical parameters against variation in gate oxide thickness in both step-FinFET and conventional FinFET (C-FinFET) using technology computer-aided design simulation is reported. It is seen that WFV of Ti metal gate has a significant influence on electrical parameters such as threshold voltage (σV_T), subthreshold swing (σSS), on current (σI_{on}), and off current (σI_{off}) with variation in gate oxide thickness. It is also perceived that the impact of WFV of Ti gate material in step-FinFET is lesser than C-FinFET. Histograms of various electrical parameters are presented for better understanding of the statistical impact of WFV of Ti metal gate in both the structures.

1. Introduction: It is well-established that FinFET is a suitable alternative device architecture for metal–oxide–semiconductor field-effect transistor (MOSFET) due to its improved short channel effects (SCEs) and higher transconductance [1]. The most important and salient feature of FinFET is that it is more capable to control the channel than traditional MOSFET [2]. However, in sub-20 nm technology, the process variability such as random dopant fluctuation [3] and line edge roughness [4] have posed serious issues in FinFET architecture. On the other hand, to improve the performance of FinFET, a stack of high-*k*/metal gate is used instead of gate polysilicon. In this regard, high-*k* gate dielectrics such as crystallised HfO_2 [5], ZrO_2 [6], and doped dielectric [7] have been found to be more appropriate. Moreover, metal gate has large number of grains within the gate area and each grain has orientation-dependent work function value, which introduces a random fluctuation in threshold voltage within the gate area, resulting in variation in electrical parameters [8]. Dadgour *et al.* [8] reported the analytical model for work function variability (WFV) of metal gate for square-shaped grains and the distribution of the electrical parameters due to WFV is found to be nearly Gaussian for large number of grains. Increased grain number with increased aspect ratio (height-to-width ratio) and/or reduced grain size within the gate area reduce the fluctuation in threshold voltage due to the impact of WFV of metal gate [9]. Similarly, improvement in threshold voltage variation can be achieved with increased device dimensions and the distribution becomes Gaussian for small size of grain [10, 11] as well.

Again depending on channel and/or gate material, the amount of variation in electrical parameter varies. Higher value of dielectric constant of Ge results in larger capacitance, and hence, the Ge FinFET has lower and higher fluctuations in threshold voltage and subthreshold swing, respectively, than Si FinFET due to WFV of metal gate [12]. Furthermore, due to less difference in WF of Ti metal grain in two different grain orientations, it is less affected by WFV than other materials such as Ta, Mo, and W [13].

Alternatively, optimisation/modification of device architecture may also provide improvement in the variability of electrical parameters. According to ratio of average grain size to gate area concept [14], the conventional FinFET (C-FinFET) has more effective gate area than junctionless FinFET, which results in reduced deviation in V_T in C-FinFET [15]. Similarly, due to reduced corner effect, the threshold voltage deviation of gate all around (GAA) nanowire (NW) FET is less affected because of the impact of WFV of metal gate [16]. Dubey and Kondekar [17] reported that triangular shape fin has more variation in threshold voltage and off current than rectangular FinFET, while on current fluctuation is more in rectangular fin. A detailed investigation on the fluctuation in various electrical parameters in Si-step-FinFET with Ti metal gate for varying device dimensions and grain size was reported [18]. As fin width and/or channel length of step-FinFET increases, variation in V_T reduces and when grain size becomes comparable with channel length, fluctuation in V_T gets saturated [18]. Such variability analysis of Ti metal gate in Si-step-FinFET, with varying gate dielectric materials, shows insignificant impact on V_T with increased gate dielectric constant [19]. In line with this, a study on the effect of WFV on various electrical parameters against variation in oxide thickness in Si-step-FinFET should also be an interesting one.

In this work, we analysed the impact of WFV on various electrical parameters for varying gate oxide thickness. Various electrical parameters investigated are: threshold voltage (σV_T), subthreshold swing (σSS), on current (σI_{on}), and off current (σI_{off}) in the presence of WFV of Ti metal gate for Si-step-FinFET. Furthermore, comparative study of electrical parameters of step-FinFET and C-FinFET in the presence of metal gate WFV is also presented.

2. Device descriptions and calibration of technology computer-aided design (TCAD) model: Figs. 1*a* and *b* show the three-dimensional (3D) and 2D schematic of Si-step-FinFET and C- FinFET, respectively. Fig. 1*c* gives the 2D schematic of C-FinFET. As observed, step-FinFET has two different fin widths and gate oxide thicknesses, but same fin height for both the devices. Therefore, the fin height is equal for both step-FinFET and C-FinFET, whereas fin width and gate oxide thickness are different. The advantages of the Si-step-FinFET over the C-FinFET is pointed out in our previous work [18].

Simulations were carried out through 3D TCAD numerical device simulator [20], and in the simulator the calibrated TCAD physics model with the fabricated results [21] was considered. The various physics models considered in simulator were: the Fermi Dirac Statistics because of the high doping source and drain regions, the Slotboom Bandgap narrowing, to activate recombination and generation the Shockley Read Hall model, and to consider the mobility of the carriers, doping-dependent Masetti models

doi: 10.1049/mnl.2018.5220

were activated [20]. To match the experimental data with simulation results, the mobility parameters are modified and such adjusted parameters are mentioned in [18]. High field saturation model was activated to consider the velocity saturation model. For small dimension device, quantum effect is expected to be present and to account this quantum density gradient model was enabled in TCAD simulator. A good matching between the simulated and experimental results [21] in terms of input and output characteristics are portrayed in Figs. 2*a* and *b*, respectively.

We have reported a comparative study of electrical parameters between the C-FinFET and step-FinFET at 10 nm technology node [18]. It is observed that the Step-FinFET provides improved International Technology Roadmap for Semi-conductors (ITRS) requirements in terms of on and off currents [18]. Step-FinFET has a very low value of off current without any significant degradation of the on current because a smaller fin width increases the source/drain resistances, leading to a decrease in the drain current [22]. The decrease in on current is not significant as the on-state saturation resistance is less affected by reduction in the fin width. The step device has lower horizontal electric field, leading to an improved SCEs.

The various device dimensions considered for C-FinFET and step-FinFET were: gate/channel length ($L_g = 12$ nm), fin height of the bottom cross-section ($H_{fin1} = 8$ nm), fin height of the top cross-section ($H_{fin2} = 2$ nm), fin width of the bottom cross-section ($W_{fin1} = 4$ nm), fin width of the top section ($W_{fin2} = 2$ nm), fin height of C-FinFET ($H_{fin} = 10$ nm), fin width of C-FinFET ($W_{fin} = 4$ nm), buried oxide height ($C = 15$ nm), doping concentration of the source/drain region ($N_S/N_D = 10^{19}$ cm^{-3}), and channel is uniformly doped with concentration of ($N_A = 10^{16}$ cm^{-3}). HfO_2 with dielectric constant ($k = 22$) is considered as gate dielectric material. The gate oxide thicknesses of step-FinFET are: oxide thickness of the lower cross-section (t_{ox1}) = 1, 1.5, 1.8, 2 nm, oxide thickness of the upper cross-section (t_{ox2}) = 2, 2.5, 2.8, 3 nm, and correspondingly, C-FinFET gate oxide thickness (t_{ox}) = 1, 1.5, 1.8, 2 nm.

In this work, the impact of WFV of Ti metal gate on electrical parameters is studied through TCAD simulator. The WF values of Ti metal gates are 4.6 and 4.4 eV in orientations <200> and <111> with probabilities 60 and 40%, respectively [8]. In this regard, we enabled the random algorithm ingrained in TCAD simulator, in which we have considered distribution of the grain is non-uniform having average grain size $(\overline{\varphi})$ of 5 and 7 nm within the gate area. The randomness of metal grains distribution with their WFs and probability of happening within the gate area is shown in Fig. 3. To estimate the fluctuation in electrical parameters, 200 different simulations are performed for each structural combination and each device has a unique random grain pattern. For 200 different simulations, we have extracted the reading for V_T, SS, I_{on}, and I_{off} from the TCAD simulator and then we determined the standard deviation of each electrical parameter among these 200 data. The standard deviation was calculated to estimate the fluctuation in electrical parameters.

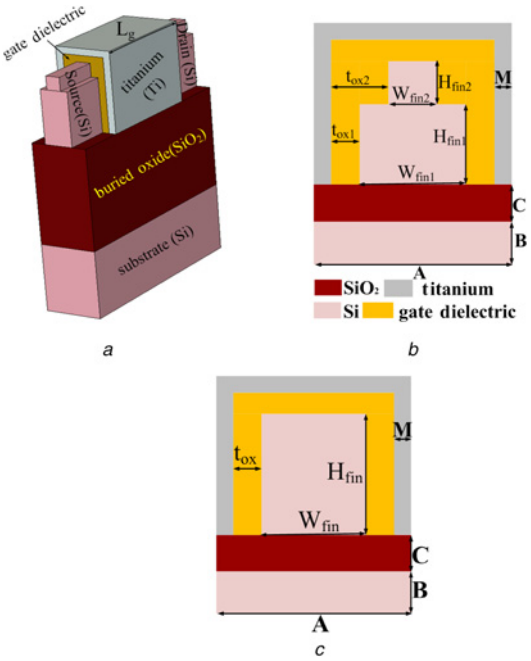

Fig. 1 *Device architectures*
a 3D schematic of Si-step-FinFET [18]
b 2D schematic of Si-step-FinFET [18]
c 2D schematic of C-FinFET [18]

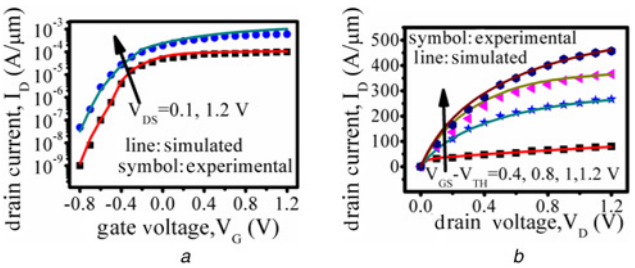

Fig. 2 *Physics of TCAD model calibration with experimental data*
a I_D–V_G plot for different drain bias [21]
b I_D–V_D plot for different gate bias [21]

3. Results and discussion: In this section, before discussing the impact of oxide thickness due to WFV, the I_D–V_G characteristics of step-FinFET, with oxide thickness as a parameter, as shown in Figs. 4*a* and *b*, respectively. With reduced oxide thickness, gate control over the channel region increases resulting in improvement of both the on and off currents.

The different electrical parameters of σV_T, σSS, σI_{on}, and σI_{off} are measured at drain-to-source bias (V_{DS}) of 0.5 V. The extraction of

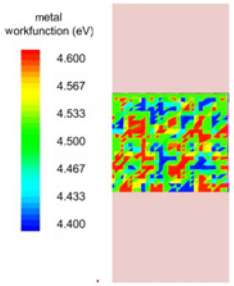

Fig. 3 *Distribution of WF within the top metal gate area [23]*

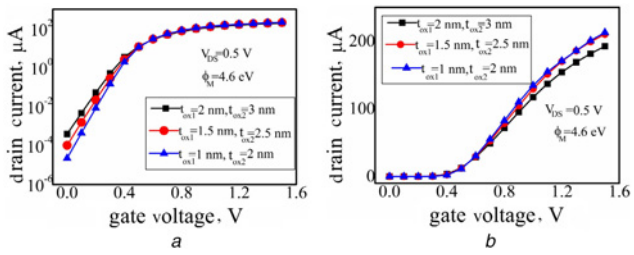

Fig. 4 *Impact of oxide thickness on I_D–V_G characteristics for step-FinFET in*
a Log scale
b Linear scale

threshold voltage is done by using $I_D = 10^{-7}$ A method. The values of on current (I_{on}) and off current (I_{off}) are extracted at $V_G = 1.5$ and 0 V, respectively, at fixed $V_{DS} = 0.5$ V.

The variation in σV_T versus oxide thickness at two different grain sizes for both Si-step-FinFET and C-FinFET is shown in Fig. 5*a*. It is observed that σV_T is lesser in step-FinFET compared with C-FinFET and this is due to the presence of smaller fin width for the top section, more gate control is achieved in step-FinFET, which leads to a smaller V_T variation. While the higher oxide thickness decreases the gate control, the increase in gate control due to smaller fin width is more dominant. It is also visualised from Fig. 5*a* that σV_T decreases significantly as oxide thickness increases and the root cause of this behaviour can be explained from Figs. 5*b* and *c*. The fluctuation in surface potential for 200 different samples at t_{ox1}, $t_{ox2} = 1$, 2 nm and t_{ox1}, $t_{ox2} = 2$, 3 nm are plotted in Figs. 5*b* and *c*, respectively. The cut line to extract the potential was at the middle of the fin cross-section, that is, $x = W_{fin1}/2$ and $y = (H_{fin1} + H_{fin2})/2$. It is visualised that the fluctuation in channel potential decreases with increasing oxide thickness, which leads to decrease in fluctuation of σV_T.

As our device has better gate control, which results in a lesser variation of σSS in Si-step-FinFET than C-FinFET at different $\bar{\varphi}$ is shown in Fig. 6*a*. Again, SS is directly proportional to oxide thickness [24], and therefore degradation in σSS is achieved with rise up in oxide thickness for both the structures.

With decrease in fin width source/drain resistance increases [22], and hence results in decreased drain current. As expected both σI_{on} and σI_{off} are more in C-FinFET compared with Si-step-FinFET as summarised in Figs. 6*b* and *c*, respectively. The impact of oxide thickness on σI_{on} and σI_{off} can summarise from Fig. 7. In this regard, we have plotted the surface potential- for 200 different samples on and off condition of the device at different oxide thicknesses. It is seen from Figs. 7*a* and *b* that the fluctuation in surface potential decreases as the oxide thickness is increased at on state of the device. However, such variation in surface potential is more with increased oxide thickness at off state of the device as portrayed in Figs. 7*c* and *d*. At on state, as oxide thickness increases, the fluctuation in surface potential decreases, which results in improvement in σI_{on} as shown in Fig. 6*b*. On the other hand, at off condition, the variation in surface potential increases with increasing oxide thickness, which is accountable for increase in σI_{off} as portrayed in Fig. 6*c*.

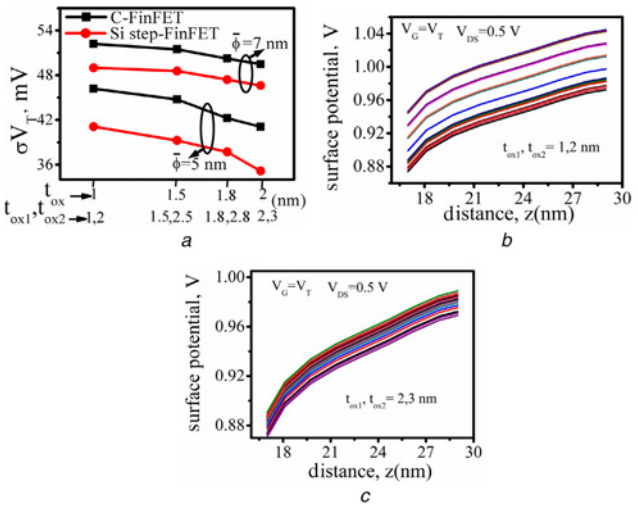

Fig. 5 *Fluctuation in V_T and physics behind it*
a σV_T of Si-step and C-FinFETs
b Fluctuation in surface potential for 200 samples data in the proposed device at $V_{GS} = V_T$, $V_{DS} = 0.5$ V, and t_{ox1}, $t_{ox2} = 1$, 2 nm
c Fluctuation in surface potential for 200 samples data in the proposed device at $V_{GS} = V_T$, $V_{DS} = 0.5$ V, and t_{ox1}, $t_{ox2} = 2$, 3 nm

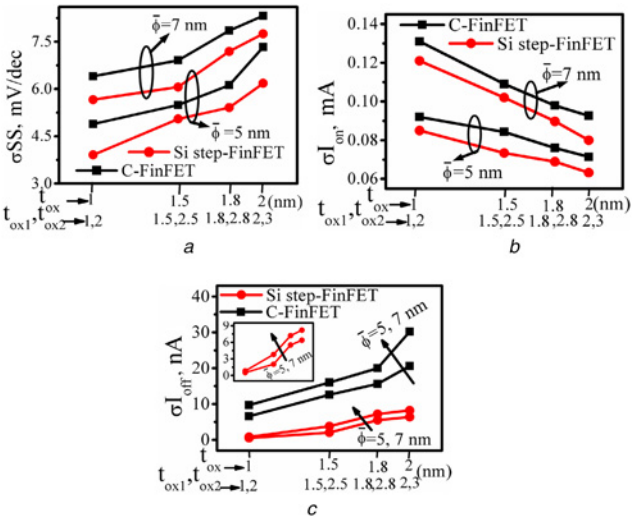

Fig. 6 *Fluctuation of electrical parameters at different φ*
a σSS of Si-step and C-FinFETs
b σI_{on} of Si-step and C-FinFETs
c σI_{off} of Si-step and C-FinFETs

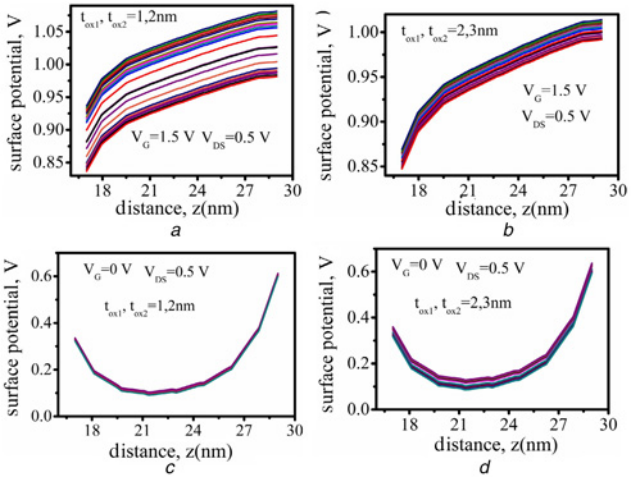

Fig. 7 *Fluctuation in surface potential in Si-step-FinFET for 200 different samples under different conditions*
a At $V_{GS} = 1.5$ V, $V_{DS} = 0.5$ V, and t_{ox1}, $t_{ox2} = 1$, 2 nm
b At $V_{GS} = 1.5$ V, $V_{DS} = 0.5$ V, and t_{ox1}, $t_{ox2} = 2$, 3 nm
c At $V_{GS} = 0$ V, $V_{DS} = 0.5$ V, and t_{ox1}, $t_{ox2} = 1$, 2 nm
d At $V_{GS} = 0$ V, $V_{DS} = 0.5$ V, and t_{ox1}, $t_{ox2} = 2$, 3 nm

The variability in various electrical parameters due to oxide thickness variation in step-FinFET for two different grain sizes is presented in Table 1. As oxide thickness increases, the values of σV_T and σI_{on} decrease, whereas σSS and σI_{off} increase. However, with increased grain size, the fluctuation in all electrical parameter values reduces. For the oxide thicknesses $t_{ox1} = 1$ nm and $t_{ox2} = 2$ nm, the σV_T and σI_{on} are more compared with the corresponding values for $t_{ox1} = 2$ nm and $t_{ox2} = 3$ nm. However, σSS and σI_{off} are higher for this set of oxide thicknesses ($t_{ox1} = 2$ nm and $t_{ox2} = 3$ nm). Therefore, optimised values are: $t_{ox1} = 1.5$ nm and $t_{ox2} = 2.5$ nm at which marginal fluctuation in electrical characteristic is obtained.

For better understanding, the effect of WFV, histograms for different electrical parameters is also analysed. It is visualised from

doi: 10.1049/mnl.2018.5220

Table 1 Comparative study of electrical parameters for different oxide thickness at two fixed average grain size in step-FinFET

t_{ox1}, t_{ox2}, nm	σV_T, mV		σSS, mV/dec		σI_{on}, mA		σI_{off}, nA	
	$\bar{\varphi} = 5$ nm	$\bar{\varphi} = 7$ nm	$\bar{\varphi} = 5$ nm	$\bar{\varphi} = 7$ nm	$\bar{\varphi} = 5$ nm	$\bar{\varphi} = 7$ nm	$\bar{\varphi} = 5$ nm	$\bar{\varphi} = 7$ nm
1, 2	41.1	49	3.91	5.66	0.085	0.121	0.525	0.826
1.5, 2.5	39.25	48.56	5.05	6.06	0.0734	0.102	2.04	3.8
1.8, 2.8	37.71	47.41	5.41	7.19	0.0689	0.0897	5.51	7.2
2, 3	35.16	46.61	6.18	7.75	0.0632	0.08	6.38	8.2

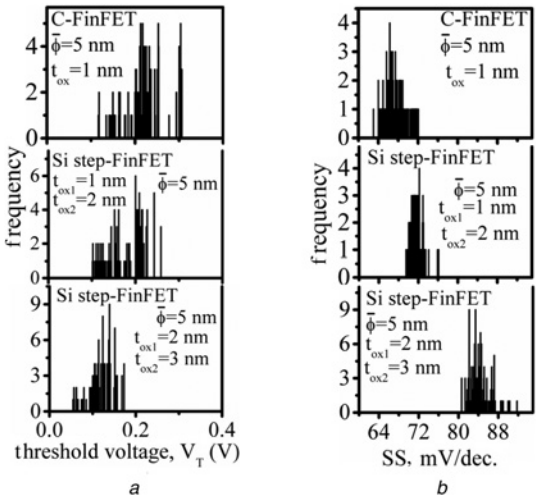

Fig. 8 *Histogram analysis to study the effect of oxide thickness in the proposed device and compared with C-FinFET*
a V_T variation
b SS variation

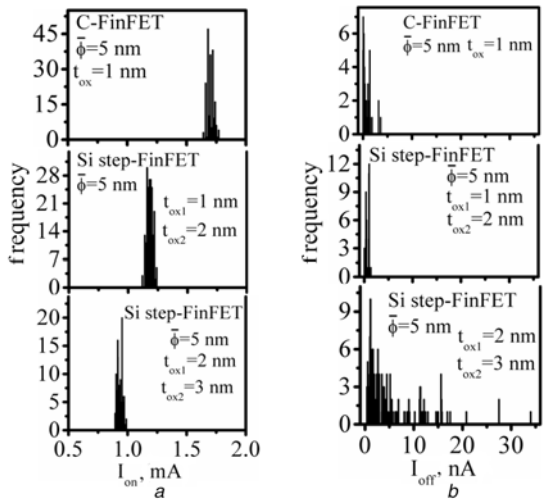

Fig. 9 *Histogram analysis to study the effect of oxide thickness in the proposed device and compared with C-FinFET*
a I_{on} variation
b I_{off} variation

histogram of V_T variation (Fig. 8*a*), the dispersion in V_T is large in C-FinFET compared with step-FinFET. In addition, due to decrease in channel potential with increased in oxide thickness; there is a significant decrease in V_T variation for Si-step-FinFET. The histogram for spreading in SS is shown in Fig. 8*b* and it is perceived that SS dispersion is lesser in step-FinFET than C-FinFET, due to having enhanced gate control for our device. As already mentioned, SS is directly proportional to oxide thickness, which leads to more spreading in SS as portrayed in Fig. 8*b* with increased oxide thickness in step-FinFET. Owing to smaller fin width, gate area decreases resulting in a reduction of the number of grains within the area. This gives rise to more fluctuation in V_T and SS and the distribution becomes non-Gaussian.

Histograms for spreading of on current and off current are plotted in Figs. 9*a* and *b*, respectively. It is observed that both the spreading of I_{on} and I_{off} are lesser in the step-FinFET compared with C-FinFET, due to having less fin width in step-FinFET. As oxide thickness increases, the fluctuation in channel potential decreases in super-threshold region while it increases in subthreshold region as shown in Fig. 7. As estimated, with increase in oxide thickness spreading of I_{on} and I_{off} decreases and increases as summarised in Figs. 9*a* and *b*, respectively.

The value of relative variation (standard deviation/average) in step-FinFET for various gate oxide thickness at $\bar{\varphi} = 5$ nm is shown in Table 2. The relative variation in V_T decreases, whereas SS increases with increase in oxide thickness. On the other hand, with increased oxide thickness, the relative variation in I_{on} decreases while I_{off} increases as summarised in Table 2.

4. Conclusion: In this work, we have investigated the impact of WFV of metal gate on electrical parameters in step and C-FinFETs by considering the WFV of the Ti metal gate. Our investigation reported that with an increase in oxide thickness σV_T decreases, σSS increases, σI_{on} decreases, and σI_{off} increases for both the architectures. Furthermore, the comparative study demonstrated that all the electrical parameters of step-FinFET are more resistant to WFV of metal gate than C-FinFET. The histogram plot shows that the distribution of electrical parameters is neither Gaussian nor symmetric.

5. Acknowledgments: The authors thank the Council of Scientific and Industrial Research, Government of India, Project [Sanction no. 22(0737)/17/EMR-II], for providing required facilities for carrying out the work.

Table 2 Relative variation in electrical parameters for different oxide thickness at $\bar{\varphi} = 5$ nm in step-FinFET

t_{ox1}, t_{ox2}, nm	σV_T, mV	$\sigma V_T/\langle V_T\rangle$, %	σSS, mV/dec	σSS/<SS>, %	σI_{on}, mA	$\sigma I_{on}/\langle I_{on}\rangle$, %	σI_{off}, nA	$\sigma I_{off}/\langle I_{off}\rangle$, %
1, 2	41.1	8.85	3.91	3.54	0.085	5.7	0.525	7.51
1.5, 2.5	39.25	7.25	5.05	5.41	0.0734	5.21	2.04	10.25
1.8, 2.8	37.71	6.40	5.41	5.82	0.0689	4.85	5.51	14.24
2, 3	35.16	5.92	6.18	6.05	0.0632	4.57	6.38	17.85

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