

Linearity improvement in E-mode ferroelectric GaN MOS-HEMT using dual gate technology

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In this work, an enhancement mode dual gate ferroelectric gallium nitride metal oxide semiconductor-high electron mobility transistor (GaN MOS-HEMT) is proposed with enhanced linearity characteristics. The different DC characteristics of the device are analysed and compared with available experimental data of single gate un-recessed ferroelectric GaN MOS-HEMT. In order to analyse the linearity performance of the devices, a look up table-based large signal model is developed directly from technology computer-aided device simulation results built by feeding different small signal parameters. The different linearity characteristics such as input third-order intercept point (IIP3), the input gain compression point (P1dB), third-order intermodulation (IM3) and the carrier to intermodulation power ratio of both the devices are compared by harmonic balance simulation of the developed large signal models. The interlink between IIP3 and IM3 with transconductance indicates that the broader the transconductance distribution with respect to different gate voltage generates higher IIP3 and lower IM3, which results in an improved linearity performance. The dual gate device shows improved linearity performance resulting in applicability in radiofrequency front end receiver.

1. Introduction: Gallium nitride (GaN)-based metal oxide semiconductor-high electron mobility transistors (MOS-HEMTs) have emerged as a potential candidate for future generation radio-frequency (RF) power applications, which not only suppresses the gate leakage current and current collapse but also helps in enhancing the breakdown voltage [1–3]. However, most of the proposed GaN MOS-HEMTs are depletion type due to the strong polarisation effects of GaN material. Enhancement mode (E-mode) device has added the advantage of having low power consumption, simpler circuit design and fail safe operation [4, 5]. In order to obtain E-mode MOS-HEMT, different techniques are available in the literature, which uses different gate insulators beneath the gate [1–3]. Recently ferroelectric materials have been used beneath the gate to obtain E-mode operation due to its strong polarisation effects, which results in polarisation engineering of two-dimensional electron gas (2DEG) and shifts the threshold voltage towards the positive direction. Furthermore, it is also observed that these ferroelectric-based GaN MOS-HEMTs have improved linearity and higher gate voltage swing (GVS) [6–8]. However, a little attention was paid on improving the linearity of ferroelectric gate MOS-HEMT through structural engineering. In this Letter, the authors propose a dual gate ferroelectric GaN MOS-HEMT, which shows improved linearity performance.

Device non-linearity is one of the primary reasons, which causes non-linear behaviour in RF circuits. The intermodulation products and gain compression, which are generated from devices second- and third-order non-linearity, are solely responsible for distortion in signal performance through the communication channel. The non-linear transconductance, capacitance, and output conductance are the main sources of non-linearity in GaN MOS-HEMT [7].

In order to evaluate the linearity performance of devices for circuit applications, an accurate large signal model is required for the device. There are different empirical large signal models such as Angelov, Curtice, and EEHEMT models, which are available in the literature [9, 10]. Instead of using these pre-existing large signal models, a self-defined large signal model is developed in this work, which can predict the device behaviour at the intrinsic

level. The large signal models are developed for both the devices by using Atlas device simulation results [11] and considering the ideal behaviour of trapping and self-heating effect. The different linearity characteristics used for evaluating the performance of RF power amplifier are input gain compression point (P1dB), third-order intermodulation (IM3) distortion, input third-order intercept point (IIP3) and carrier to intermodulation power ratio (C/I) [9]. Therefore, in this Letter, these linearity characteristics of both the devices are analysed and compared with each other through harmonic balance simulation results of their respective large signal models.

The organisation of the Letter as follows. In Section 2, the device structures of both single and dual gate ferroelectric GaN MOS-HEMTs along with their operation are presented. A look up table (LUT)-based large signal model is presented in Section 3. In Section 4, different linearity characteristics of both devices are compared and discussed. Finally, a conclusion is drawn in Section 5.

2. Device structure and operation: Figs. 1 and 2 show the cross-sectional views of single and dual gate ferroelectric GaN MOS-HEMTs. The epitaxial layers consist of 30 nm aluminium nitride (AlN) nuclear layer, 1.3 μm undoped GaN buffer layer, 1 nm AlN interlayer, 20 nm $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier layer, and 2 nm GaN cap layer from down to top, which is grown on silicon carbide substrate. A 2 nm interfacial aluminium oxide layer is presented before the 30 nm lead zirconate titanate (PZT) layer to maintain good interface quality. The PZT ($\text{Pb}(\text{ZrTi})\text{O}_3$) layer is used to provide ferroelectric polarisation opposite to that of nitride polarisation, which depletes the 2DEG channel to realise E-mode operation. Gate recess technique is used for both the devices to realise E-mode operation.

For single gate MOS-HEMT, the gate length, gate-to-drain spacing, and gate-to-source spacing are considered as 0.5, 3.5 and 3.5 μm , respectively. Similarly, for the dual gate MOS-HEMT structure, the gate length, gate-to-drain spacing, and gate-to-gate spacing gate-to-source spacing are 0.5, 2.2 μm , 1.6, and 2.2 μm , respectively. A single gate non-recessed depletion mode

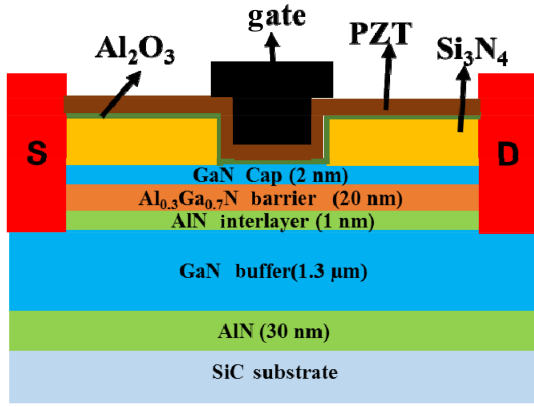


Fig. 1 Cross-sectional view of single gate ferroelectric GaN MOS-HEMT

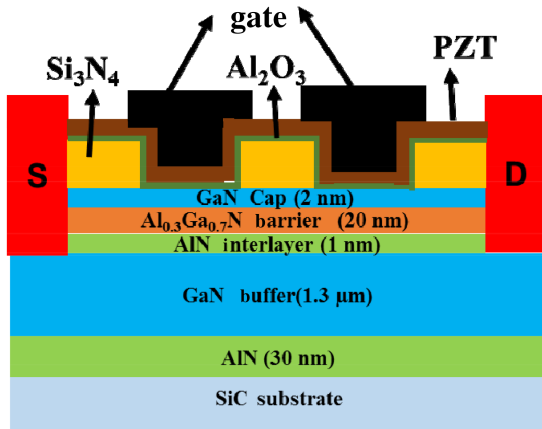


Fig. 2 Cross-sectional view of dual gate ferroelectric GaN MOS-HEMT

ferroelectric MOS-HEMT is also simulated having the same dimensions of the fabricated device from the literature [6] in order to validate the DC transfer characteristics of the proposed device.

3. Large signal model and harmonic balance simulation: Fig. 3 shows the simplified large signal model, which has been used in this work. The model is derived directly from the small signal equivalent circuit whose extraction techniques are described in our previous work [12] expect the non-linear capacitances, which are implemented in the form of charge sources. As shown in Fig. 3, the non-linear capacitances are implemented as quasi-static gate charge sources (Q_{gs} and Q_{gd}). Two bias dependent resistances R_i and R_{gd} are added in the circuit in order to consider the non-quasi-static effect of the channel charge. The different

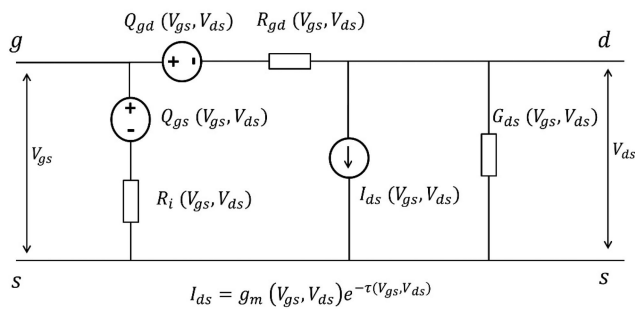


Fig. 3 Simplified large signal model

charges are expressed as follows:

$$Q_{gs}(V_{gs}, V_{ds}) = \int_{V_{gs0}}^{V_{gs}} C_{gs}(V, V_{ds0}) dV + \int_{V_{ds0}}^{V_{ds}} C_{gs}(V_{gs0}, V) dV, \quad (1)$$

$$Q_{gd}(V_{gs}, V_{ds}) = \int_{V_{gs0}}^{V_{gs}} C_{gs}(V, V_{ds0}) dV - \int_{V_{ds0}}^{V_{ds}} [C_{ds}(V_{gs}, V) dV + C_{gd}(V_{gs}, V) dV]. \quad (2)$$

In order to implement the large signal model, a seven-port symbolically-defined device (SDD), which is an equation-based component present in advanced design system (ADS) [13] is used, which helps in quickly and easily defining custom, non-linear components. The SDD is defined by specifying different equations which relate the port voltage, port currents, and their derivatives. Every term has an explicit, implicit or a weighting function expression. The weight of '1' represents inductance or capacitance and weight of '0' denotes voltage or resistance. Ports 1–6 of the SDD represent Q_{gs} , Q_{gd} , R_i , R_{gd} , and I_{ds} , respectively. Port 7 consists of 1 Ω termination and a weighting function that helps us to get a delayed input voltage, referencing to the small signal parameter, τ . The harmonic balance simulation setup for the large signal model with input and output matching circuit is shown in Fig. 4.

The large signal model is implemented in the form of LUT, which is directly derived from technology computer-aided device simulations. The data access component, which is present in ADS, is used to read the LUT-based data from the file.

The large signal model consists of two series capacitances C1 and C3, which are used for DC blocking or AC coupling capacitors. Since the parallel pad capacitances and associated series inductances are useful for constructing a small signal model and these parameters will not affect the large signal models, so these are not presented in the large signal model schematic diagram.

In order to analyse the linearity of both the devices, harmonic balance simulation of the developed large signal models has been carried out. The single tone analysis has been carried out at a frequency of 20 GHz. Similarly, the double tone analysis has been carried out at a frequency of 20 GHz and 100 kHz having the same offset. To consider the non-linearity and power distribution linearity up to the third harmonic frequency, an order of three has been used for simulation. To ensure maximum power transfer and minimum input and output return loss, the input and output matching networks are designed as shown in Fig. 4. The different values of inductor–capacitor matching networks are calculated by optimisation of the large signal scattering parameters having the constraints on input and output return loss as $S_{11} < -15$ dB and $S_{22} < -15$ dB.

4. Results and discussion: The polarisation curve of the device is simulated by applying an AC voltage at a small frequency, which is varied from 0 V to voltages greater than the coercive field. Fig. 5 shows the polarisation curve of the device with respect to the electric field at $V_{max} = 20$ V for different temperatures. It shows a hysteresis curve between polarisation and electric field, which indicates the retention of polarisation in the device. The curve also shows that the polarisation increases with increase in temperature. However, the hysteresis loop is wider with an increase in temperature, which indicates that the PZT at higher temperature cannot be used as gate material as this polarisation may be induced due to leakage current.

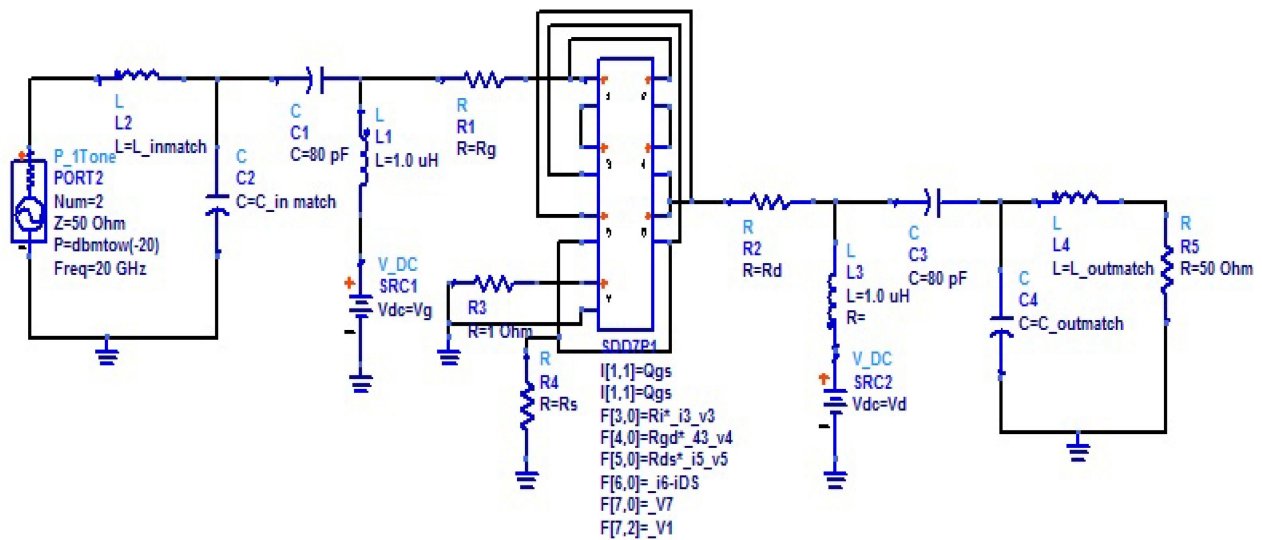


Fig. 4 Harmonic balance simulation setup of the large signal model

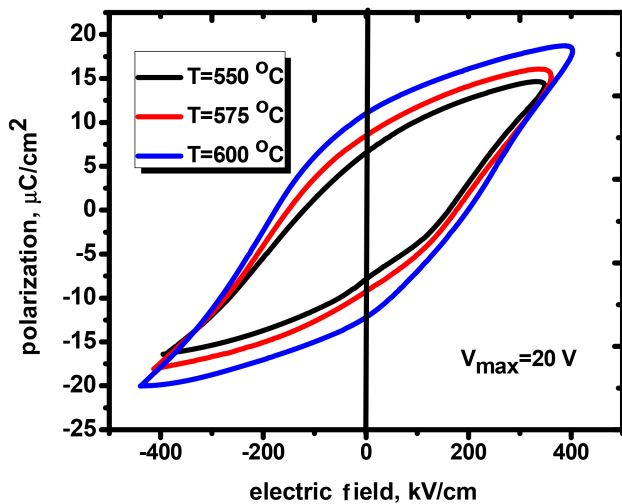


Fig. 5 Polarisation versus electric field of the device for different temperatures

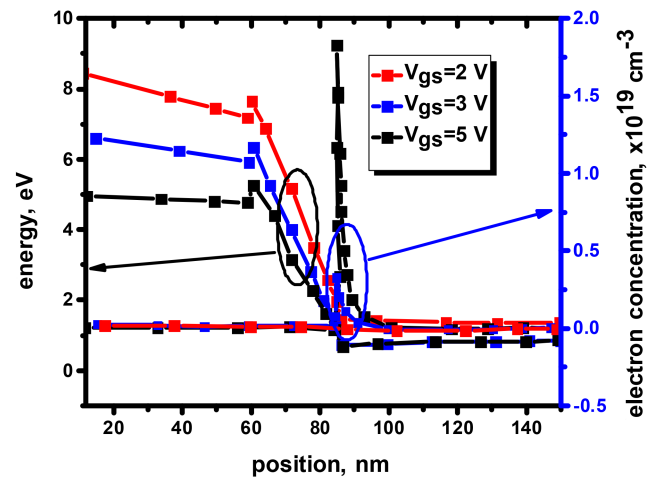


Fig. 6 Energy band diagram and electron concentration of single gate ferroelectric GaN MOS-HEMT for different gate voltages

Fig. 6 shows the electron concentration and energy band diagram of single gate GaN MOS-HEMT for different values of gate voltages (V_{gs}). From the figure, it is clear that with an increase in gate voltage (V_{gs}) across the transition voltage, the electrons are accumulated at the AlGaIn/GaN interface and hence energy band is bending. It is very similar to conventional MOS-HEMT. This leads to efficient modulation of the AlGaIn surface potential near the edge of conduction band which results in good control in 2DEG density even at forward bias. Hence the GVS of ferroelectric GaN MOS-HEMT is increased, which leads to improvement of linearity.

Fig. 7 shows the $I_{ds}-V_{gs}$ and g_m-V_{gs} curves of both the devices. It is observed that the dual gate MOS-HEMT has a more positive threshold voltage of 1.7 V as compared to single gate MOS-HEMT having 0.7 V, which indicates the dependence of the threshold voltage on gate length. The results are also compared with available experimental data [6] of the un-recessed device, which shows negative threshold voltage and larger transconductance. When the gate length is scaled down the effect of electron velocity overshoot is more significant since more number of electrons travel ballistically.

It is also observed that the slope of $I_{ds}-V_{gs}$ curve of single gate device is relatively higher than that of dual gate device at $V_{gs}=2$

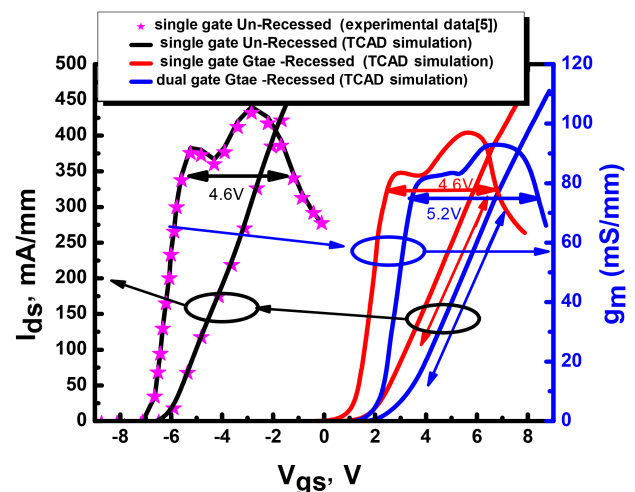


Fig. 7 Input transfer characteristics comparison of single and dual gate ferroelectric MOS-HEMT

to 6 V. The main reason behind this slope is that the higher electric field at the gate edge generates high electron velocity due to which the transit time is reduced and hence gives rise to higher drain current and transconductance.

The maximum transconductance extracted for the single and dual gate MOS-HEMTs is 99 and 91 mS/mm, respectively. Although the effective gate length is doubled for dual gate MOS-HEMT as compared to single gate MOS-HEMT, at the same time the effective gate capacitance is decreased since both are connected in series. Hence, we got the values of G_m very close to each other. The double hump feature of transconductance is observed due to the polarisation in the ferroelectric material. It is also observed that the GVS of dual gate MOS-HEMT is high as compared to a single gate and un-recessed MOS-HEMT, which suggests that the dual gate MOS-HEMT has better linearity behaviour.

The different parameters of single and dual gate MOS-HEMTs extracted from DC and AC device simulations are presented in Table 1. From the table, it is observed that dual gate ferroelectric MOS-HEMT has relatively lower values than single-gate ferroelectric MOS-HEMT.

The relationship between IM3 and IIP3 with G_m and G_{ds} is expressed as [7]

$$IM3 @ \frac{(G_m'')^2}{G_{ds}^2 \cdot R_L} A^6, \quad (3)$$

$$IIP3 @ \frac{(G_m)^3}{G_m'' \cdot G_{ds}^2 \cdot R_L}, \quad (4)$$

where G_m'' is the second derivative of transconductance and A is the single amplitude and R_L is the load impedance. Equations (3) and (4) indicate that IM3 is directly proportional to $(G_m'')^2$, whereas the IIP3 is inversely proportional to G_m'' and directly proportional to $(G_m)^3$. Since the dual gate MOS-HEMT has higher GVS, which generates smaller G_m'' as compared to single gate MOS-HEMT as shown in

Table 1 Parameter comparison between single and dual gate ferroelectric MOS-HEMT at $V_{gs} = 3$ V and $V_{ds} = 10$ V

Parameter	Single-gate ferroelectric MOS-HEMT	Dual-gate ferroelectric MOS-HEMT
g_m , mS/mm	99	91
C_{gs} , pf	30	24
C_{gd} , pf	16	11

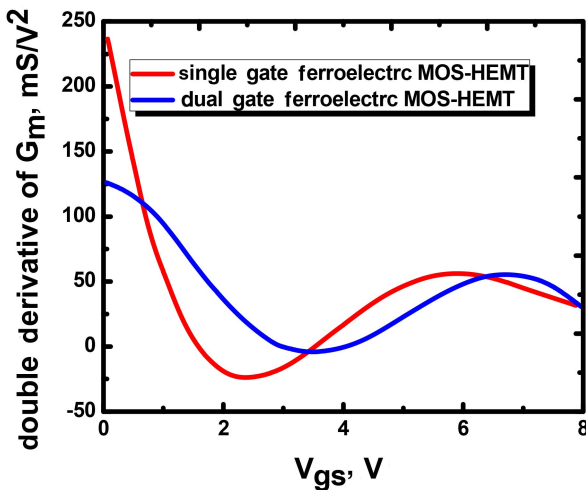


Fig. 8 Second derivative of transconductance comparison of single and dual gate ferroelectric MOS-HEMT

Fig. 8. This results in lower IM3 and higher IIP3 for dual gate MOS-HEMT and hence better linearity.

Figs. 9–11 show the harmonic balance simulation results of the large signal model. The main sources of non-linearity of the

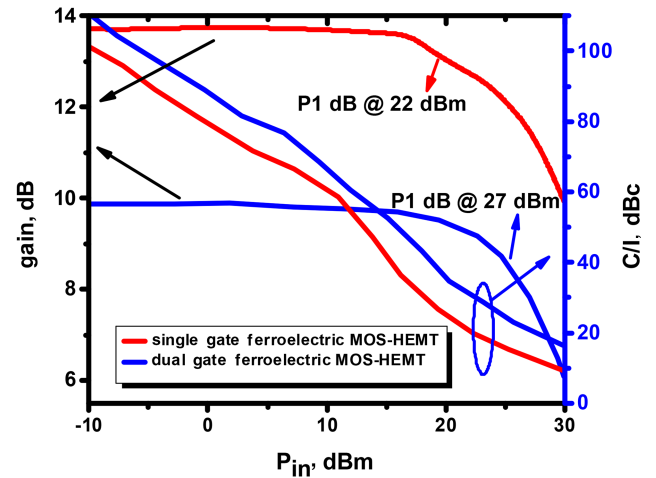


Fig. 9 Gain and C/I ratio comparison of single and dual gate ferroelectric MOS-HEMT with respect to input power

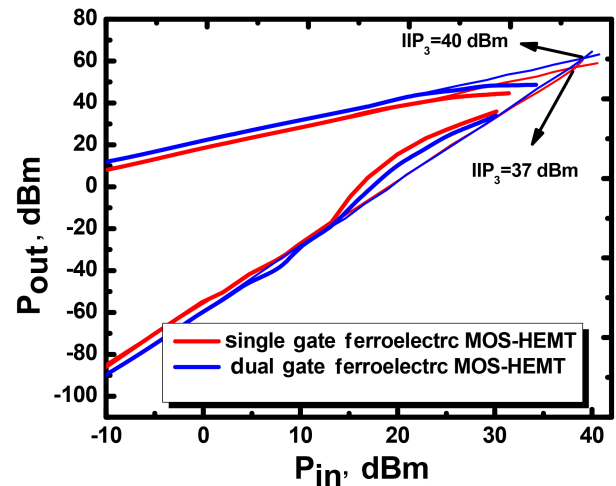


Fig. 10 Fundamental output power and IM3 distortion power with respect to input power

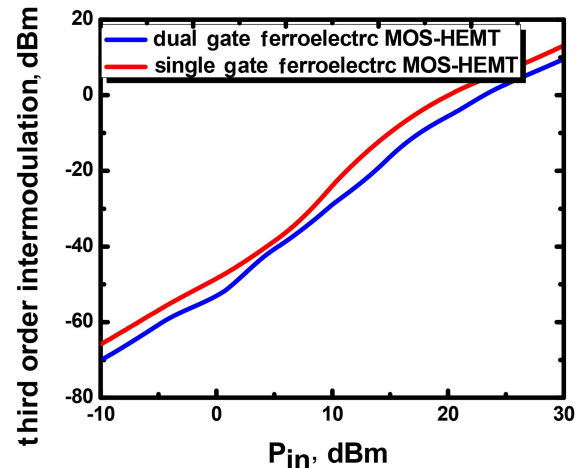


Fig. 11 IM3 comparison of single and dual gate ferroelectric MOS-HEMT

device are g_m , C_{gs} , C_{gd} and g_{ds} . So the bias points for harmonic balance simulation are chosen such that the non-linearities caused by these parameters are minimum thereby increasing the linearity behaviour. In this work, the gate and drain bias chosen is 2 and 12 V, respectively. In order to avoid the ambiguity between Class A and Class AB mode of power amplifier operation in this work, the quiescent current is explicitly set as 2% of the maximum current.

Fig. 9 shows gain versus input power and the P1dB compression point of single and dual gate MOS-HEMT are extracted as 22 and 27 dBm, respectively. It shows that the gain of single gate MOS-HEMT is higher than the dual gate MOS-HEMT by 3.7 dB due to the higher transconductance of the single gate MOS-HEMT. The 1 dB compression point is also high nearly up to 1 dB for the dual gate case, which shows a slight improvement in the linear behaviour of dual gate MOS-HEMT. Fig. 9 also shows the C/I ratio comparison of both the devices with respect to input power. It shows that the C/I ratio is relatively higher for dual gate MOS-HEMT. The suppression of IM3 at higher input power, in this case, is the main reason behind this.

Similarly, Fig. 10 presents the fundamental output power and IM3 distortion power for both the devices as a function of input power. From this curve, the IIP3 of single and dual gate MOS-HEMT are extracted as 37 and 40 dBm, respectively, which are 13 and 14 dBm higher than their respective P1dB compression point. It also shows that the IM3 distortion power deviates from the ideal curve at an input power higher than 0 dBm, which is the indication of non-linearity at these values.

Fig. 11 shows the comparison of IM3 distortion of single and dual gate MOS-HEMTs. Although the IIP3 and P1dB compression point of dual gate MOS-HEMT show a very small deviation from single gate MOS-HEMT, the average IM3 of dual gate MOS-HEMT shows nearly 7 dB lower than single gate MOS-HEMT and also the intermodulation power is closer to the ideal line. This can be mainly attributed due to the flat g_m (higher GVS) and the antisymmetric behaviour of C_{gs} about the gate bias point. Lower distortion and higher output power in case of dual gate MOS-HEMT gives rise to suppression of IM3 around 10 dB higher than single gate MOS-HEMT.

5. Conclusion: In this Letter, a dual gate ferroelectric GaN MOS-HEMT is proposed. The DC and linearity performances of the device are compared with a single gate ferroelectric GaN MOS-HEMT. In order to further analyse the linearity of the devices, a LUT-based large signal equivalent circuit is built by feeding different small signal parameters. The output power and linearity characteristics of both the devices are analysed by performing harmonic balance simulation of their respective large signal models at a frequency of 20 GHz. It is concluded that although the single gate device shows higher ON current and transconductance, the

dual gate device has comparatively large device linearity having higher IIP3, lower IM3 and higher C/I ratio. These results indicate that the dual-gate ferroelectric GaN MOS-HEMT is a potential candidate to be applicable for future RF front end receiver.

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