


# PSJ LDMOS with a VK dielectric layer

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Published in Micro & Nano Letters; Received on 14th August 2018; Revised on 26th December 2018; Accepted on 11th February 2019

A partial super junction lateral double-diffused metal–oxide–semiconductor field-effect transistor with a variable- $k$  dielectric layer (PSJ VK LDMOS) is proposed in this Letter. Low- $k$  material and PSJ are introduced into the device. PSJ provides a low-resistance channel to reduce the specific on-resistance ( $R_{\text{on,sp}}$ ). Furthermore, according to an enhanced dielectric layer field, low- $k$  buried layer can sustain the high breakdown voltage (BV). To eliminate substrate-assisted depletion effect and improve the lateral BV of the proposed structure, the charge compensation layer in the device adopts a variation of lateral doping technique and is combined with the  $N$  pillar in PSJ. Ultimately, the simulation results show that BV of 795.5 V and the figure of merit (FOM) of  $6.1 \text{ MW cm}^{-2}$  are achieved for PSJ VK LDMOS. BV and FOM are enhanced by 71.4 and 81.1%, respectively, compared with con. PSJ SOI LDMOS with the drift region length of  $46.5 \mu\text{m}$ . Furthermore,  $R_{\text{on,sp}}$  of  $103.4 \text{ m}\Omega \text{ cm}^2$  is reduced by 31.2% compared with the ‘silicon limit’ at the same BV class, which breaks the ‘silicon limit’.

**1. Introduction:** Lateral double-diffused metal–oxide–semiconductor field-effect transistor (LDMOS) has been widely used in different high-voltage fields such as switching power supplies and power amplifiers [1]. However, due to the limitation of length and concentration of drift region,  $R_{\text{on,sp}}$  and breakdown voltage (BV) of LDMOS exist the relationship of ‘silicon limit’ [2], which greatly limits its application in the high-voltage fields. The invention of super junction (SJ) breaks the ‘silicon limit’ of conventional power MOSFET devices and then the important  $R_{\text{on,sp}}$ –BV relationship of the power MOSFET devices is reduced from  $R_{\text{on,sp}} \propto \text{BV}^{2.5}$  to  $\text{BV}^{1.32}$  [3]. However, the conventional SJ LDMOS exists the substrate-assisted depletion (SAD) which will reduce the BV of the device. To solve this problem, scientists have proposed many new structures [4–8]. SOI technology is introduced into SJ LDMOS with its advantages of ideal dielectric isolation and relatively simple dielectric isolation process [9–13]. However, SOI has a low vertical BV, which hinders its development. According to the enhanced dielectric layer field (ENDIF) principle [14], the electric field of the buried layer in the device can be increased when the dielectric constant  $k$  of the buried layer is reduced. The dielectric constant of low- $k$  material is  $<3.9$  which is that of silicon dioxide ( $\text{SiO}_2$ ), so the low- $k$  material can dramatically improve the electric field in the buried layer of the device.

According to what has been mentioned, a partial SJ LDMOS with a variable- $k$  dielectric layer (PSJ VK LDMOS) has been put forward and investigated theoretically in this Letter. Confirmed by SENTAURUS 2013, SAD is eliminated. Moreover, PSJ not only improves the lateral BV, but also reduces  $R_{\text{on,sp}}$ . Furthermore, the low- $k$  dielectric buried layer greatly improves the vertical BV. Finally, PSJ VK LDMOS accomplishes the high BV and low  $R_{\text{on,sp}}$  of SJ and it achieves a good compromise between BV and  $R_{\text{on,sp}}$ .

**2. Structure and mechanism:** The structure of PSJ VK LDMOS is shown in Fig. 1a. The buried oxide (BOX) and low- $k$  dielectric buried layer constitute a VK dielectric layer.  $L_{\text{OX}}$ ,  $L_{\text{Lk}}$  and  $L_{\text{SJ}}$  represent the length of BOX, low- $k$  dielectric layer and PSJ, respectively. Here,  $t_{\text{SJ}}$  and  $W_{\text{SJ}}$  denote the thickness and width of the PSJ.  $N_{\text{n}}$  and  $N_{\text{p}}$ , respectively, are the concentrations of N and P pillars in the PSJ, and  $N_{\text{b}}$  means the initial doping concentration in the charge compensation layer (CCL).

As shown in Fig. 1a, PSJ VK LDMOS includes PSJ at the source and a low- $k$  dielectric buried layer under the drain. The PSJ increases the lateral electric field to enhance the lateral BV at the off-state. In addition, it provides a low-resistance path when the device is on, which reduces  $R_{\text{on,sp}}$ . To suppress the SAD, PSJ includes a CCL whose concentration increases linearly from source to drain. Moreover, the doping concentration satisfies the relationship  $N = N_{\text{b}} + Gx$ , ( $0 < x < L_{\text{SJ}}$ ), where  $N_{\text{b}}$  and  $G$  are the initial concentration and slope of the linearly variable doping in CCL, respectively. The change curve is roughly shown in Fig. 1b.

As Fig. 2 shows, according to ENDIF, the vertical BV is expressed as

$$\text{BV} = 0.5E_{\text{S}}t_{\text{S}} + E_{\text{I}}t_{\text{I}} \quad (1)$$

where  $E_{\text{S}}$  is the electric field of the Si layer, and  $t_{\text{S}}$  and  $t_{\text{I}}$  are the thicknesses of the Si and dielectric layers, respectively. By the continuity of electric displacement,  $E_{\text{I}}$  is shown as

$$E_{\text{I}} = \frac{\epsilon_{\text{S}}E_{\text{S}}}{\epsilon_{\text{I}}} + \frac{q\sigma_{\text{in}}}{\epsilon_{\text{I}}} \quad (2)$$

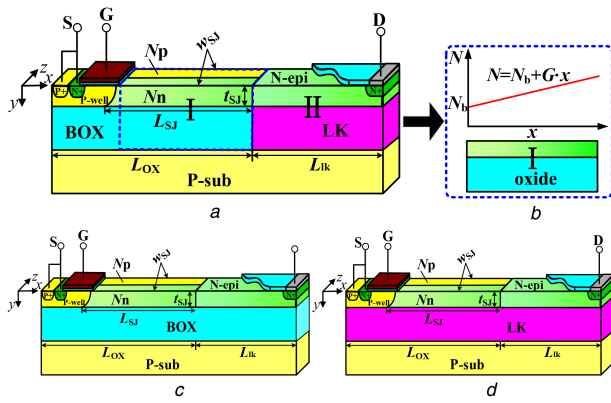
where  $\sigma_{\text{in}}$  is the interface charge density, and  $\epsilon_{\text{S}}$  and  $\epsilon_{\text{I}}$  are the permittivities of the Si and dielectric layers, respectively. Thereby the vertical BV is

$$\text{BV} = 0.5E_{\text{S}}t_{\text{S}} + \frac{\epsilon_{\text{S}}}{\epsilon_{\text{I}}}t_{\text{I}}E_{\text{S}} + \frac{qt_{\text{I}}\sigma_{\text{in}}}{\epsilon_{\text{I}}} \quad (3)$$

When  $k$  is only reduced, the vertical BV is increased. Therefore, the introduction of low- $k$  dielectric buried layer increases the vertical BV of PSJ VK LDMOS.

The simulation parameters of the PSJ VK LDMOS are shown in Table 1.

**3. Simulation results and discussion:** Fig. 3 shows the distributions of equipotential lines for PSJ VK LDMOS and con. PSJ SOI LDMOS at the breakdown. It can be seen from Fig. 3a that in PSJ VK LDMOS, the distributions of equipotential lines in N-type drift region and PSJ are relatively uniform and dense, whereas in con. PSJ SOI LDMOS the equipotential lines



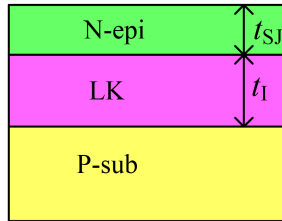
**Fig. 1** Structures and concentration of CCL

a PSJ VK LDMOS

b Concentration doping diagram in CCL,  $N = N_b + Gx$ ,  $N_b$  and  $G$  denote the initial concentration and slope of linear variation doping in CCL, respectively

c Con. PSJ SOI LDMOS

d Con. PSJ LK LDMOS



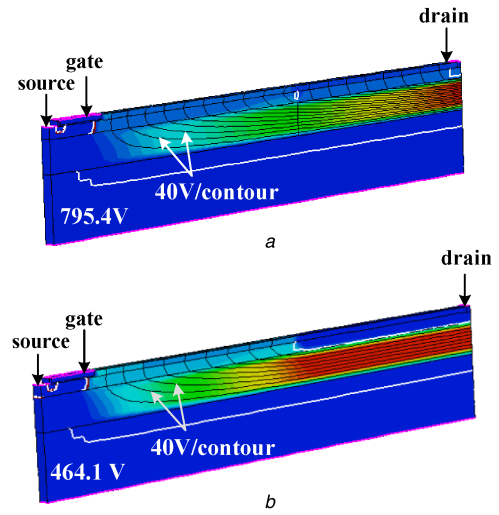
**Fig. 2** Partial structure diagram of PSJ VK LDMOS

**Table 1** Device parameters of the PSJ VK LDMOS

Symbol	Description	Value
$L_{SJ}$	length of SJ, $\mu\text{m}$	30
$L_{OX}$	length of BOX layer, $\mu\text{m}$	5
$L_{LK}$	length of low- $k$ dielectric buried layer, $\mu\text{m}$	optimised
$N_n(10^{16})$	N pillar of SJ concentration, $\text{cm}^{-3}$	1.0
$N_p(10^{16})$	P pillar of SJ concentration, $\text{cm}^{-3}$	1.0
$N_b(10^{15})$	initial concentration of CCL, $\text{cm}^{-3}$	4.5–6.5
$t_{SJ}$	thickness of SJ, $\mu\text{m}$	1
$t_I$	thickness of low- $k$ dielectric buried layer, $\mu\text{m}$	3
$W_{SJ}$	width of SJ, $\mu\text{m}$	1

distribution is only even and dense in PSJ. There is no distribution of equipotential lines in the N-type drift region of the previous structure. The reason is that in order to increase BV, PSJ VK LDMOS introduces a low- $k$  dielectric layer under the drain to increase the electric field of the buried layer, which enhances vertical BV of the device. Therefore, BV of PSJ VK LDMOS reaches 795.4 V, whereas con. PSJ SOI LDMOS is only 464.1 V.

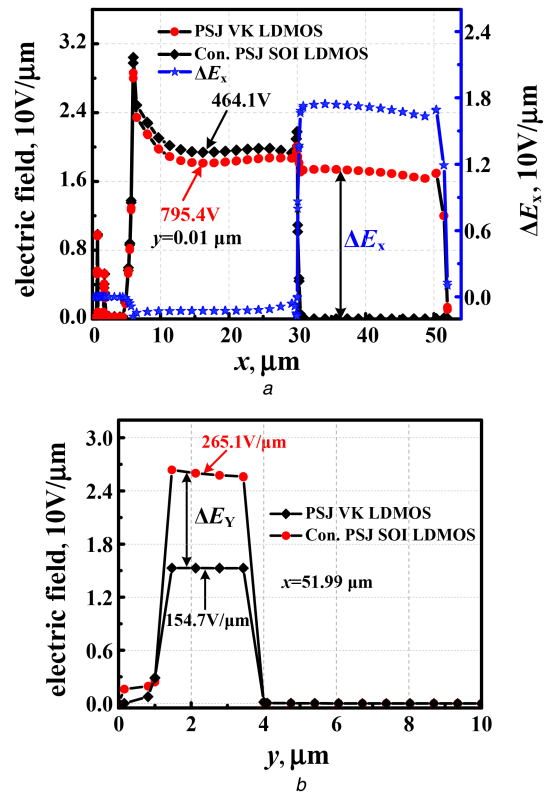
Fig. 4 illustrates the lateral and vertical electric field distributions for PSJ VK LDMOS and con. PSJ SOI LDMOS. As Fig. 4a shows that electric field of the conventional structure at PSJ reaches about 20 V/ $\mu\text{m}$ , but at N-type drift region is zero. The average electric field of the proposed structure at PSJ is around 20 V/ $\mu\text{m}$  and N-type drift region is  $\sim 17$  V/ $\mu\text{m}$ . We can calculate from Fig. 4a that N-type drift region of the proposed structure sustains about 43% of the lateral BV. Fig. 4b shows that PSJ VK LDMOS has a buried layer electric field of 270 V/ $\mu\text{m}$ , whereas that of con. PSJ SOI LDMOS is only 150 V/ $\mu\text{m}$ .  $\Delta E_y$  is about 120 V/ $\mu\text{m}$ . On the basis of the ENDIF principle, the low- $k$  buried layer of PSJ VK LDMOS enhances the vertical electric field to increase the vertical BV.



**Fig. 3** Equipotential lines distributions at the breakdown (40 V/contour)

a For PSJ VK LDMOS

b For con. PSJ SOI LDMOS



**Fig. 4** Lateral and vertical electric field distributions for PSJ VK LDMOS and con. PSJ SOI LDMOS

a Lateral electric field distributions, where  $\Delta E_x$  represents the electric field difference between the proposed and conventional structures

b Vertical electric field distributions under the drain, and  $\Delta E_y$  means the electric field difference in the buried layer of the proposed and conventional structures

It can be clearly seen from Fig. 5 that at the off-state, when the voltages of the proposed and the conventional structures reach 795.4 and 464.1 V, respectively, the current sharply increases to cause a breakdown.

Fig. 6 reveals the relationship of  $R_{on,sp}$  and BV versus  $L_{OX}$ . We can see that  $R_{on,sp}$  does not change much as  $L_{OX}$  changes, but BV varies a lot and obtains the optimum when  $L_{OX}$  is 30  $\mu\text{m}$ . That is because when the concentration of CCL is certain if  $L_{OX}$  is

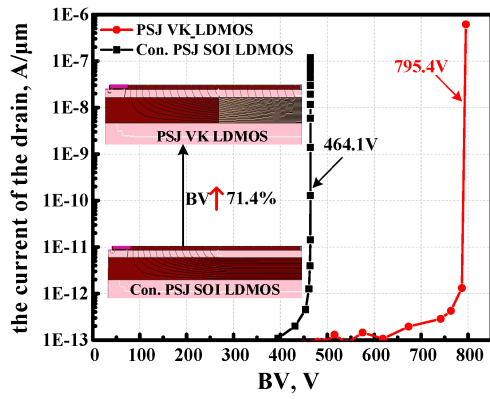


Fig. 5 Transfer characteristics of PSJ VK LDMOS and con. PSJ SOI LDMOS at the off-state

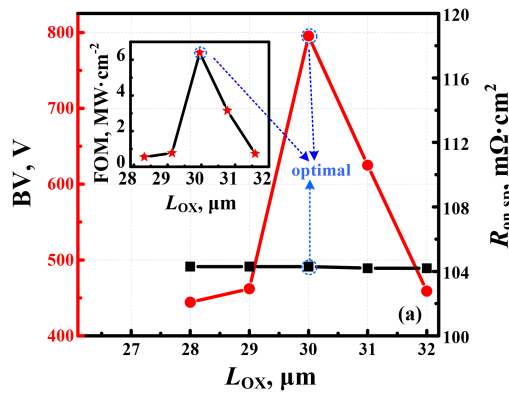


Fig. 6 Dependence of BV and  $R_{on,sp}$  on  $L_{OX}$

longer or shorter than  $L_{SJ}$ , PSJ or N-type drift region will straddle between the BOX and low- $k$  dielectric layer. Then, the different dielectric constants of both  $SiO_2$  and low- $k$  dielectric will break the charge balance of PSJ, which will lower BV of the device.

Fig. 7 displays the relationship among  $k$ , BV and  $R_{on,sp}$ . According to ENDIF principle, when  $k$  is reduced, the electric field of the buried layer will be improved. However, the low- $k$  buried layer also reduces the auxiliary depletion effect of substrate on the drift region. Furthermore, when  $k$  is high, the assisted depletion effect of substrate on the drift region is strengthened and the power lines directed to substrate from the drift region are increased, which results in a drop of the surface electric field and BV for the device. When  $k$  is low, the auxiliary depletion effect of substrate on the drift region is weakened, which causes the drift region not to be completely depleted. Therefore,  $k$  of 1.1 is optimal.

Fig. 8 indicates the relationship between BV and  $R_{on,sp}$  versus  $N_b$  and  $G$ . As Fig. 8 shows when  $N_b$  or  $G$  is certain, BV will increase with the improvement of the other first and then declines, but  $R_{on,sp}$  drops continuously. The reason for this is that when we increase  $N$  by fixing  $N_b$  or  $G$  and improving the other,  $R_{on,sp}$  will fall as the concentration of drift region increases. Moreover, when  $N$  does not reach the critical value, the increase of the concentration of CCL will enhance the charge compensation of PSJ and then improve the BV of the device. However, when this critical value is exceeded, the excessive concentration of the drift region will cause premature breakdown of the device surface, which lowers BV.

Fig. 9 provides with many data about BV and  $R_{on,sp}$  of SJ LDMOS. Compared with other structures, the figure of merit (FOM) of PSJ VK LDMOS is optimal. We can see from this figure that BV and  $R_{on,sp}$  of PSJ VK LDMOS are 795.4 V and 104.3  $m\Omega \cdot cm^2$ , which has broken the 'silicon limit'.

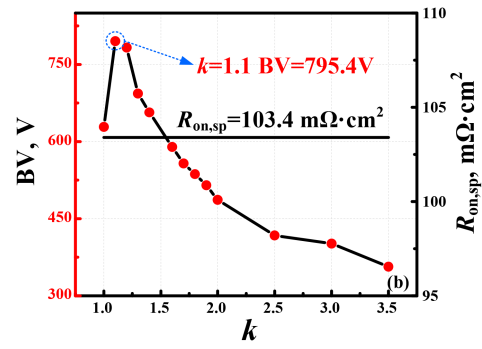


Fig. 7 Relationship among  $k$ , BV and  $R_{on,sp}$

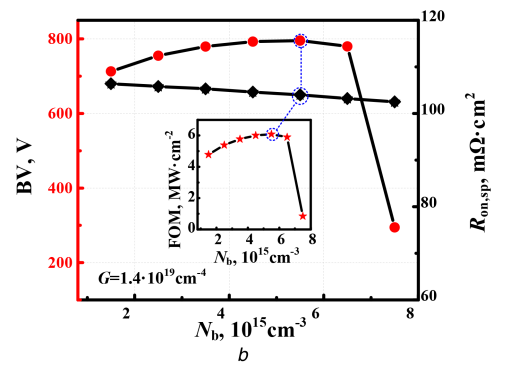
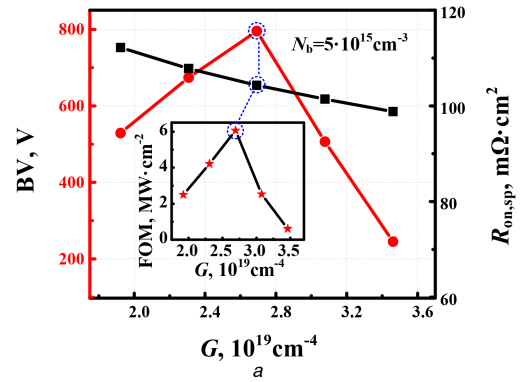


Fig. 8 Relationship between BV and  $R_{on,sp}$  versus  $G$  and  $N_b$   
a Relationship between BV and  $R_{on,sp}$  versus  $G$   
b Relationship between BV and  $R_{on,sp}$  versus  $N_b$

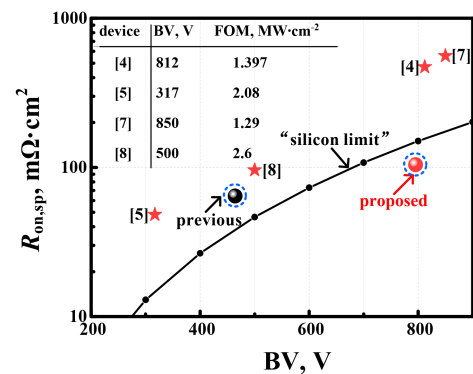
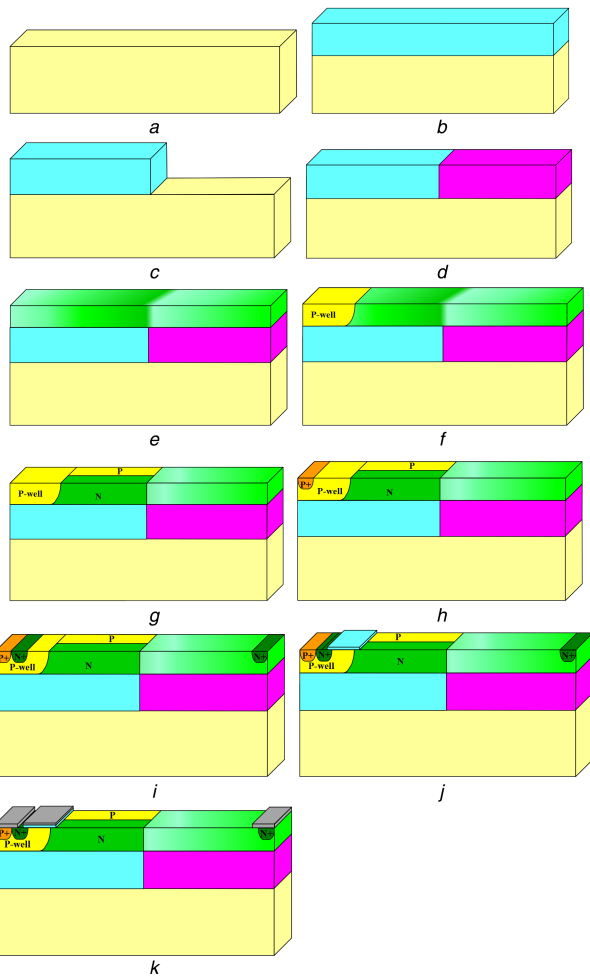


Fig. 9 Comparison of BV and  $R_{on,sp}$  for different SJ LDMOS devices

The key process steps of PSJ VK LDMOS are showed in Fig. 10. Thermally grow  $SiO_2$  in Fig. 10b; etch the  $SiO_2$  region to form the deep trench by the method of reactive ion etch in Fig. 10c; deposit



**Fig. 10** Key process steps of PSJ VK LDMOS

- a prepare P-type substrate  
b thermally grow SiO<sub>2</sub>  
c etch the SiO<sub>2</sub> region  
d deposit the low-k materials  
e epitaxially grow a N-type doped silicon region and ion implantation in the different regions  
f ion implantation  
g ion implantation  
h ion implantation  
i ion implantation  
j thermally grow SiO<sub>2</sub>  
k electron beam evaporation to form the electrodes

**Table 2** Parameters for three devices

	BV, V	$R_{on,sp}$ , mΩ cm <sup>2</sup>	$BV^2/R_{on,sp}$ , MW cm <sup>-2</sup>
<b>PSJ VK LDMOS</b>	<b>795.4</b>	<b>104.3</b>	<b>6.066</b>
con. PSJ SOI LDMOS	464.1	64.3	3.349
con. PSJ LK LDMOS	773.3	172.5	3.467

Bold values shows excellent features compared with the conventional structures

the low-k materials by the method of chemical vapour deposition in Fig. 10d; epitaxially grow an N-type-doped Si region and ion implantation in the different regions in Fig. 10e; ion implantation to form the P-well region in Fig. 10f; ion implantation to form the N pillar and P pillar in Fig. 10g; ion implantation to form the P+ region in Fig. 10h; ion implantation to form the N+ region in

Fig. 10i; thermally grow SiO<sub>2</sub> in Fig. 10j; electron beam evaporation to form the electrodes of the source, gate and drain in Fig. 10k. Therefore, the production processes of PSJ VK LDMOS are compatible with conventional processes.

The device parameters by simulation of the three devices are shown in Table 2. As can be seen from Table 2, the PSJ VK LDMOS has the highest BV. The FOM is the largest among them. Therefore, the PSJ VK LDMOS achieves a good compromise between the BV and  $R_{on,sp}$ .

**4. Conclusion:** PSJ VK LDMOS proposed in this Letter perfectly combines PSJ and VK materials. Furthermore, PSJ can optimise the surface electric field distribution of the device and enhance the lateral BV. The introduction of low-k dielectric buried layer increases the vertical BV, which improves the vertical BV. According to SENTAURUS 2013 simulation data, compared with con. PSJ SOI LDMOS, BV and FOM of PSJ VK LDMOS reach 795.4 V and 6.1 MW cm<sup>-2</sup>, which are improved by 71.4 and 81.1%, respectively.

**5. Acknowledgments:** This work was supported by the National Natural Science Foundation of China (grant no. 61306094), the Scientific Research Fund of Hunan Provincial Education Department (grant no. 15C0034) and the introduction of talents project of Changsha University of Science & Technology (grant no. 1198023).

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